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Impact of temperature on analog/RF, linearity and reliability performance metrics of tunnel FET with ultra-thin source region

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Abstract
In this script, authors affirm a novel structure of tunnel FET in which a lightly doped channel region completely bounds the ultra-thin finger-like source region to enhance the tunneling probability with an increased tunneling interface area. TFETs have become common in power-constrained applications due to the minimal subthreshold swing (SS) and low OFF current (I_{off}) with low ON-state driving current (I_{on}) and ambipolar conduction concerns. Decreasing device dimensions is becoming more crucial for protecting device linearity and reliability under varying manufacturing and environmental conditions. However, changes in ambient temperature (T) imply its efficiencies, such as linearity distortion, analogue, and high-frequency performance, which must be thoroughly investigated. The impactful analysis was carried out for manuscript for assuring analog/RF performance, linearity distortion, and reliability of F-shaped TFET. Extensive investigations have been performed to check device susceptibility towards temperature ranging from 250 to 400 K by using the 2D-TCAD tool. For this, various critical parameters like I_{on}, I_{ambi}, SS, parasitic capacitances, threshold voltage (V_{th}), I_{on}/I_{off} ratio, transconductance (g_m), output transconductance (g_{ds}), higher-order g_m (g_{m2} and g_{m3}), intrinsic gain (IG), cut-off frequency (f_t), gain bandwidth product (GBP), transconductance generation factor (TGF), transit time (TT), transconductance frequency product (TFP), VIP_2, VIP_3, IIP_3, IMD_3 and 1-dB compression point have been investigated for temperature sensitivity analysis for the proposed device. Furthermore, reliability analysis is also performed, which shows that with a significant change in second harmonics, rising temperature is seen to be unfavorable for the SS, I_{ambi} and I_{on}/I_{off} ratio.

Keywords Ultra-thin source · Band-to-band tunneling (B2BT) · Linearity · Reliability · Source/channel interface (S–C-I) · Drain/channel interface (D–C-I) · Ambipolar current

1 Introduction

Downscaling of metal oxide semiconductor field-effect transistors (MOSFETs) has been performed over the years and years to improve device efficiency in terms of I_{on}, high-frequency parameters, and reliability of the device, to satisfy semiconductor industries demands and continue to realize Moore's vision [1]. On the other hand, continuous downscaling leads to several critical problems like hot carrier effect, high leakage current, short channel effects, and drain-induced barrier lowering (DIBL), and those are causative for high power consumption [2]. These limitations are labeled as a significant barrier to device reliability. Apart from this, the SS value of MOSFET (switching speed) is limited by thermal factor kT/q. In an ideal case, the minimum SS value of MOSFET is 60 mV/decade, but it may be worst in practical case [3]. To overcome the limitation of MOSFET, an extensive study is carried out on the forthcoming device named tunnel FET (TFET) for its substitute. TFET devices offer very low SS without any limitation with very low leakage current in the range of femto (10^{-15}) ampere [4, 5]. Along with these substantial advantages, high I_{ambi}, lower I_{on}, and poor high-frequency performance are considerable problems of TFET devices. To improve the TFET performance for real-world application (like biosensor, memories, logic gates), many researchers have been working to enhance the I_{on} with suppress ambipolar conduction by using different concepts, and engineering techniques [6–8]. We need better electrically characteristics for analog/RF applications along

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with better linearity and reliability performance under the various environmental conditions like impact of temperature variation, power supply fluctuation, etc. Theses variations are responsible for intermodulation, and harmonic distortions [9]. Thus, these effects must be carefully investigated for the device reliability and linearity performance check. Therefore, this proposed work is devoted to a detailed analysis of temperature effect on analog/RF, linearity, and reliability performance, which can be benchmark/solution for real-time application.

To overcome the limitation of conventional TFET like low I_{on}, high I_{ambi}, high V_{th} etc., we proposed a new structure with an ultra-thin finger-like source with increased S–C-I for better B2BT probability at source/channel junction. The proposed device is named as single gate F-TFET (SG-F-TFET) because of ultra-thin finger-like source which is wholly inserted in the channel region [10]. As we know, the basic working principle of TFET mainly depended on the B2BT at S–C-I (for I_{on}) and D–C-I (for ambipolar conduction). So, in this proposed device, the S–C-I junction area is increased to enhance I_{on} by increasing the B2BT rate of the carrier at S–C-I, and D–C-I boundary is reduced to limit the ambipolar behavior by widening the width of potential barrier present at D–C-I junction. As we know, the performance of nano-devices is empathetic towards temperature variation [11], and an extensive study is carried to analyze the impact of temperature variation on SG-F-TFET for future replacement in the high-frequency application. The linearity and reliability analysis also performed because adjacent channel signals interface with the original signal and crumble data quality in the high-frequency application. Maintaining linearity metrics within a healthy range is essential.

This script is drafted as follows. First, the DC performance of SG-L-TFET has been investigated with OFF-state sensitivity analysis with variation in temperature and different device models. The impact of temperature variation on analog and high-frequency performance parameters is explained in the "Impact on Analog/RF Parameters" section. In Sect. 5, the device linearity's sensitivity towards various temperature ranges was investigated. In the end, in the "Reliability Analysis" section, the effects of temperature variations on system reliability are discussed with various pie charts.

2 Device Schematic and Parameters

The 2D cross-sectional view of the proposed SG-F-TFET device schematic is illustrated in Fig. 1, and Table 1 showcases the complete device dimension parameters used during the simulation process. In these, silicon (Si) thin film is considered for device. The Si-based doped source region is highly doped (p+), and Si-based drain region (n+) is

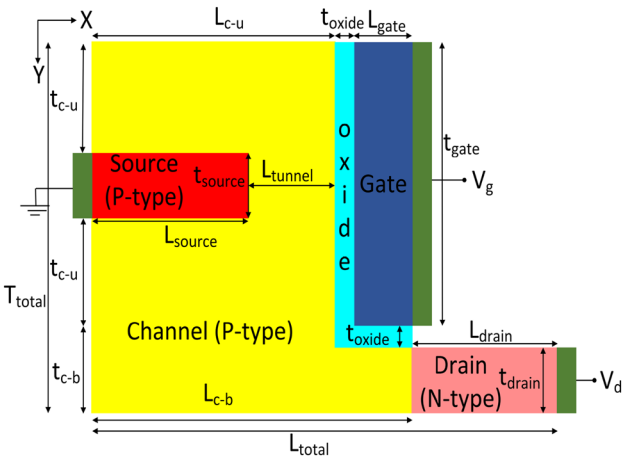
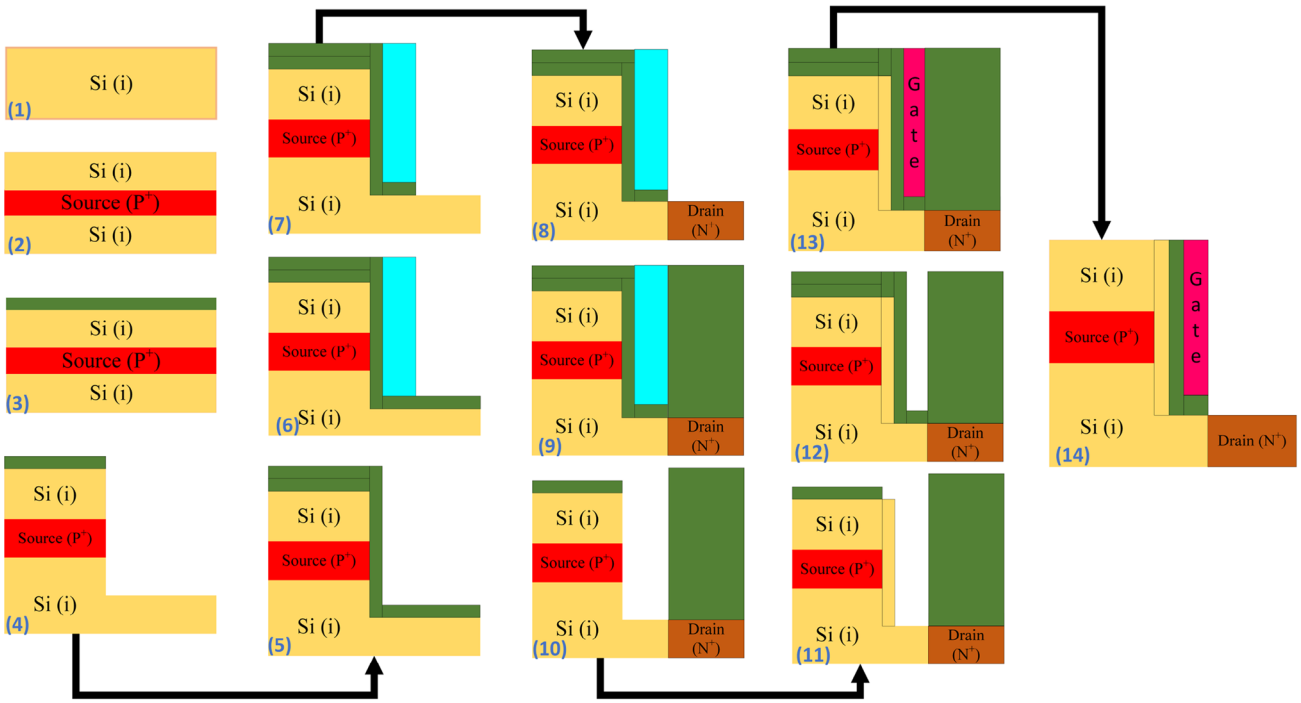


Fig. 1 2D cross-sectional view of SG-F-TFET

lightly doped. Molybdenum with 4×10^{15} atom/cm^2 nitrogen implant dose is used to achieve gate electrode work function (WF_G) 4.5 eV with SiO_2 as gate oxide. The proposed device consists of a single gate with an ultra-thin, highly doped source region that is entirely bounded by the intrinsic channel region. On the other hand, drain region of device is attached to the outside of the channel, due to this D–C-I is reduced and device looks like an L-shaped. For an extensive study of temperature impact on the various performance parameters of the proposed device, some crucial models are also used during the simulation process. Some used important models are standard band-to-band tunneling model (BTBT), band gap narrowing model (BGN), Auger recombination model (Auger), field-dependent mobility model (FLDMOB), concentration-dependent mobility model (CONMOB), Shockley–Read–Hall model (SRH), trap-assisted tunneling model (TAT), etc. Along with these models, Newton's numerical method was used to provide strong coupling between the resultant equations for better convergence of current. Excluding this, to analyze RF functioning, the frequency is set to 1 MHz. The physic parameters of device used in models equation are listed in Table2 with corresponding values used during simulation process.

In the table, MUN and MUP are the mobility of electron and hole carriers, respectively. BGN.E, BGN.N and BGN.C parameters are material dependent, and it can be defined with the material properties. ϵ_{si} is permittivity of silicon, and ϵ_{sio_2} stands for permittivity of gate oxide. m_e^* and m_h^* are effective mass of electron and holes, m_0^* stands for rest mass (9.11×10^{-31} kg).

From a fabrication point of view, the possible fabrication process flow to fabricate the device is depicted in Fig. 2 step by step. For this, self-align process would be used to fabricate the proposed device. In brief, the key steps for self-align



(1) Si bulk wafer **(2)** Growing ip+i epitaxial layers with in-situ doping **(3)** SiO_2 hard mask deposition **(4)** Mesa patterning **(5)** Deposition of SiO_2 sacrificial layer **(6)** Dummy gate deposition **(7)** Etch back process and SiO_2 remove to form drain region **(8)** Ion-implantation and rapid thermal annealing process (RTA) (Arsenic (As) impurity added) **(9)** SiO_2 deposition and planarization **(10)** Dummy gate removal **(11)** Selective epitaxial layer growth for intrinsic silicon **(12)** High-k oxide deposition **(13)** Metal gate stack deposition and at last **(14)** Etch back process and final device.

Fig. 2 Basic steps for fabrication of SG-F-TFET device

Table 1 Description of the basic design variables used for simulation

Parameters	Abbreviations	SG-F-TFET
Gate oxide thickness	t_{oxide}	1 nm
Thickness above and below source	t_{c-u}	16 nm
Channel thickness at bottom of device	$t_{c-b} = t_{drain} + t_{oxide}$	6 nm
Lateral tunneling length	L_{tunnel}	4 nm
Source thickness	t_{source}	3 nm
Source length	L_{source}	37 nm
Gate length	L_{gate}	20 nm
Gate thickness	$t_{gate} = 2t_{c-u} + t_{source}$	35 nm
Channel thickness	$2t_{c-u} + t_{c-b} + t_{source}$	41 nm
Channel length (upper)	L_{c-u}	41 nm
Channel length (bottom)	L_{c-b}	62 nm
Drain length	L_{drain}	38 nm
Drain thickness	t_{drain}	5 nm
Gate work-function	WF_G	4.5 eV
Drain doping concentration	N_D	10^{18} cm^{-3}
Channel doping concentration	N_C	10^{15} cm^{-3}
Source doping concentration	N_S	10^{20} cm^{-3}
Total device length	L_{total}	100 nm
Total device thickness	T_{total}	41 nm

process flow are as follows: (1) epitaxial layer grown for P+ type silicon layer, active region patterning, and SiO_2 hard-mask deposition; (2) Mesa patterning is followed by SiO_2 buffer layer deposition; (3) dummy gate deposition and etch-back process with drain region formation with the help of ion implantation and annealing process; (4) for exposure of dummy gate, chemical mechanical polishing can be used; (5) after that for lateral tunneling region epitaxial layer is grown, and at the last (6) oxide/metal gate formed by atomic layer deposition [10, 12–15].

3 DC performance analysis

This section is edifying the impact of T variation (from 250 to 400 K, with a 50 K gap) on DC performance of SG-F-TFET. At the initial stage of sensitivity analysis of device w.r.t. any external fluctuations under different working conditions, variation in energy band diagram (EBD), transfer characteristics ($I_{ds} - V_{gs}$ curve), V_{th} and SS is the best medium to observe.

When T increases above the room temperature, the covalent bond inside the lattice of body material starts to break, and many electron and hole pairs (EHPs) are generated. The generation rate of EHPs is directly propositional to intrinsic

Table 2 Physic parameters of device structure

Parameters	E_{g300} (eV)	MUN (cm^2/Vs)	MUP (cm^2/Vs)	ϵ_{si}	ϵ_{sio_2}	m_e^*	m_h^*	BGN.E (V)	BGN.N (cm^{-3})	BGN.C
Values	1.08	1000	500	11.7	3.9	$0.26m_0$	$0.36m_0$	6.93×10^{-3}	1.3×10^{17}	0.5

carrier concentration of semiconductor (n_i) [16, 17]. The n_i is exponentially increased with T as per Eq. 1. Along with this, the variation in T also affects the band profile of device at both interfaces (S–C-I and D–C-I). The relation between energy band (E_g) and T is given in Eq. 2.

$$n_i = N_a \exp\left(\frac{E_g}{2kT}\right) \tag{1}$$

$$E_g(T) = E_g(300) - \frac{\alpha T^2}{T+\beta} \tag{2}$$

where N_a is the impurity (donor/acceptor) concentration, kT is the energy term (product of T and Boltzmann constant), $E_g(300)$ (1.08 eV for Si material) is the band gap at room temperature, α (4.73×10^{-4} for Si) and β (636 K for Si) are the fitting parameters of body material.

The effect of T fluctuation on EBD at S–C-I and D–C-I is depicted in Fig. 3. The change in EBD at D–C-I is high (Fig. 3b) as compared to EBD at S–C-I for ON-state condition (Fig. 3a). The overall impact of T on band bending of energy bands in ON-state condition is not considerable, and we can say that band bending of energy bands is less sensitive towards T variations. On the other hand, the percentage change in majority charge carriers (charge carriers of source region) is very less for changes in T because the generated EHPs are significantly less as compared to the carrier present in the highly doped source region. Consequently, we have not seen any significant impact of T on I_{on} of SG-F-TFET, as depicted in Fig. 4a. The minority charge carrier is inversely proportional to the doping concentration, and it will increase with a rise in T because more numbers of EHPs are generated. Thus, the percentage deviation in minority charge carrier concentration (charge carrier of drain region) is very high [16, 19]. Due to this, the ambipolar conduction increases as well as T increases from 250 to 400 K with interval of 50 K, as shown in Fig. 4b.

To ensure the model accuracy used during simulation, the proposed device is calibrated with experimental results of doped L-shaped tunnel FET (L-TFET) (Ref. [18]). The calibration is done with the same material and physical dimensions as of doped L-TFET. The simulation results authenticate with experimental data as depicted in Fig. 4c. From Fig. 4c, we can see that the simulated results are well matched with the experimental results, which proves the accuracy of the models used in during simulation work.

When ramp V_{gs} is applied, the $I_{ds} - V_{gs}$ curve on semi-log scale is divided into three region. The first region is known as OFF-state region ($V_{gs} < V_{off}$), the second region known as subthreshold region ($0\ \ V_{gs} < V_{th}$), and the third region is super-threshold region ($V_{gs} > V_{th}$). The device switching speed is examined with the help of the 2_{nd} region of $I_{ds} - V_{gs}$ curve because this region describes how fast device conditions change OFF-state to ON-state. In other words, the steepness of the $I_{ds} - V_{gs}$ curve decides the switching speed of device

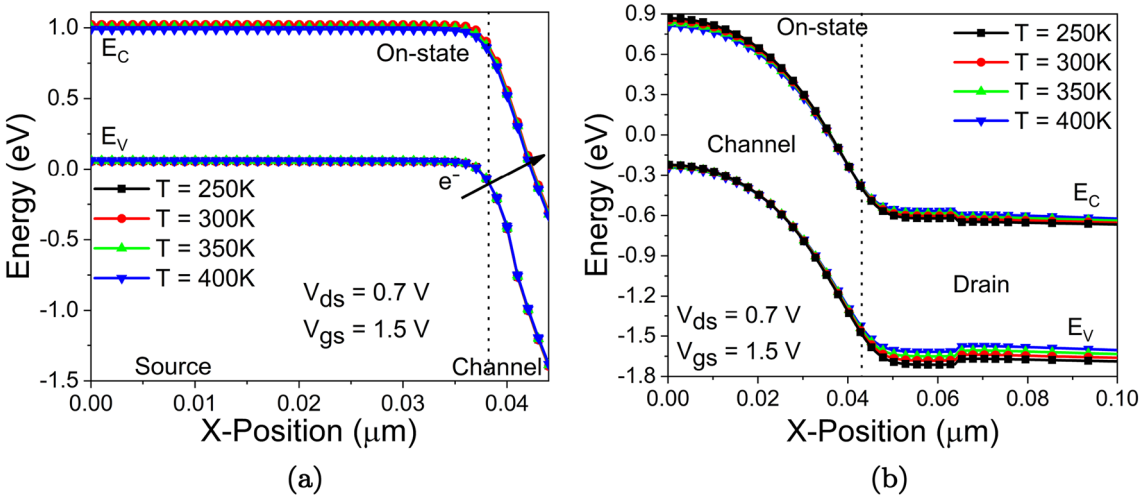


Fig. 3 ON-state EBD of proposed device **a** at S–C-I and **b** at D–C-I junction

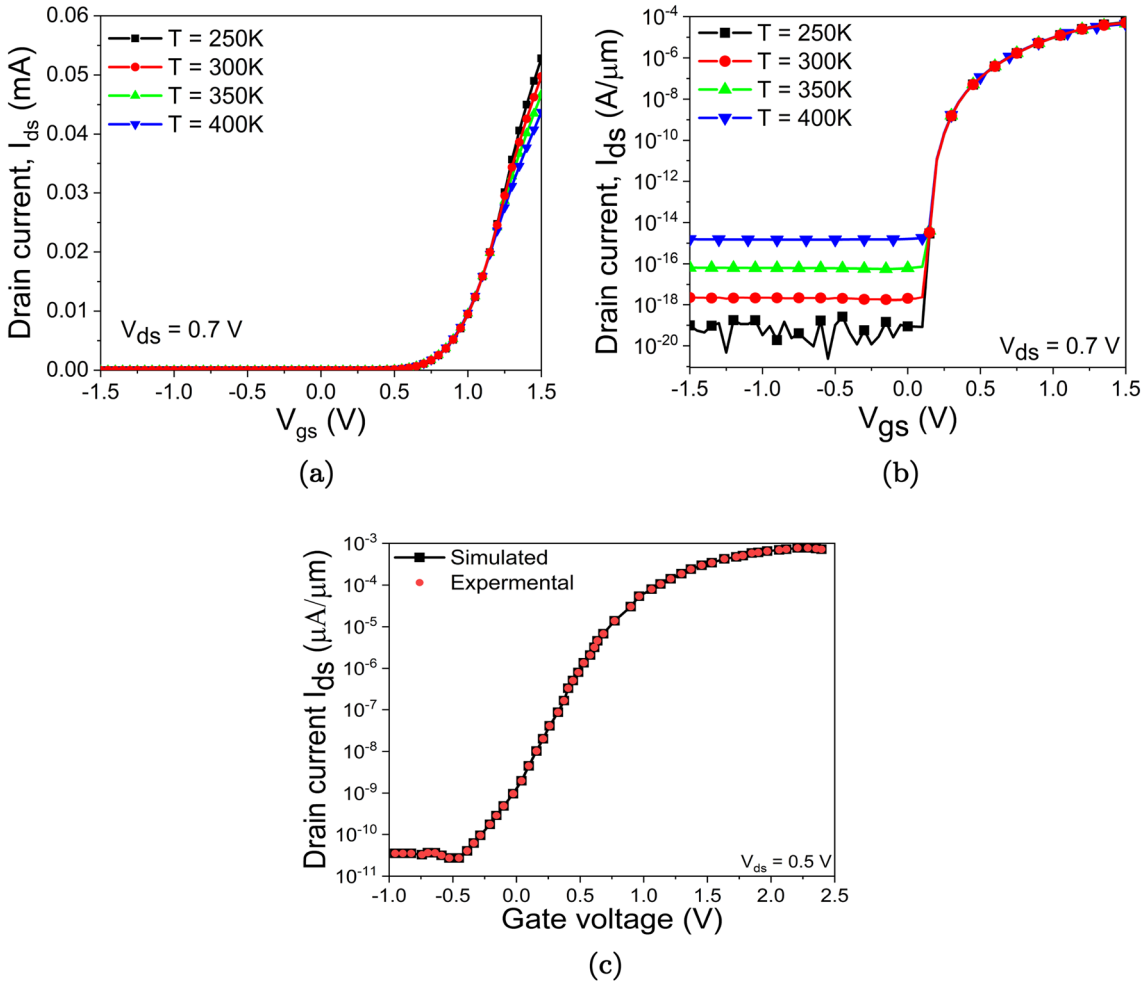


Fig. 4 I_{ds}-V_{gs} data plot for various T on **a** linear and **b** semi-log scale to visualize the variations in I_{on} and I_{ambi} **c** calibration curve of the simulated device with the experimental data as presented in Ref. [18]

[20, 21]. The steepness of the curve defines the SS, and its mathematical expression is illustrated in Eq. 3.

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log\left(\frac{I_{th}}{I_{off}}\right)} \tag{3}$$

The SS value is inversely proportional to the steepness of $I_{ds} - V_{gs}$ curve in the subthreshold region. Figure 5a demonstrates that as T increases, the SS value increases (red lines), which is not a good sign for the switching speed of proposed device. On the other hand, V_{th} of the proposed device reduces (black lines, Fig. 5a) with a rise in T, and it is beneficial for ultra-low-power application. In addition, an intensive analysis is performed for I_{on}/I_{off} ratio and I_{ambi}. As we earlier see that I_{on} is not significantly affected by T variation, but I_{off} shows the opposite behavior (Fig. 4b). The I_{on}/I_{off} ratio of proposed device decreases as T increases (Fig. 5b) because I_{on} slightly decreases but I_{off} significantly increases with an increment in T. Similarly, the impact of T on I_{ambi} is portrayed in Fig. 5c.

3.1 OFF-current analysis

The OFF-state conditions of proposed device are much affected by T variation. T plays a critical role in the reliability of SG-F-TFET for circuit-level applications because the I_{on}/I_{off} ratio is highly affected. The higher I_{on}/I_{off} ratio leads to better switching speed [22–24]. Therefore, an extensive study is performed on SG-F-TFET for OFF-state conditions. For this, the impact of models and T both are carefully investigated to extract the optimum T range and models for improved performance of the proposed device. During the simulation process, we opted for BTBT, TAT (trap-assisted tunneling), and SRH (Shockley–Read–Hall) to analyze the effect of T on I_{off}.

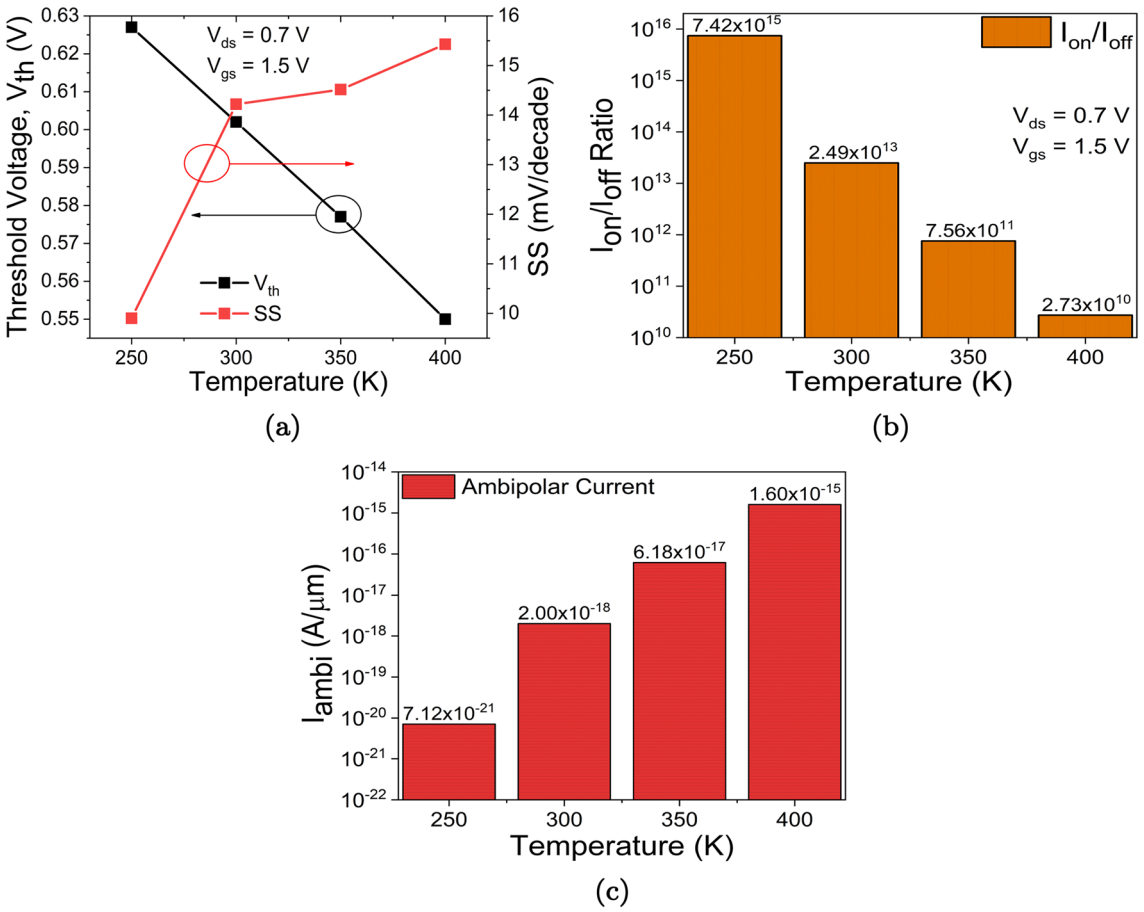


Fig. 5 Variations in **a** V_{th} (left Y-axis) and SS (right Y-axis), **b** I_{on}/I_{off} ratio, **c** I_{ambi} for different T values

$$T(E) \propto \exp\left[-\frac{4\sqrt{2m^*}E_g^{*3/2}}{3h|e|(E_g^* + \Delta\varphi)}\sqrt{\frac{\epsilon_{si}t_{ox}t_{si}}{\epsilon_{ox}}}\right]\Delta\varphi \tag{4}$$

high E-field and show less sensitivity towards the T variations [25].

By using Eq. 5, we investigate the impact of the SRH model on proposed devices at various T values. Constant

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUP0\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUN0\left[p + n_{ie}exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{5}$$

$$R_{TAT} = \frac{pn - n_{ie}^2}{\frac{TAUP0}{1+\Gamma_p^{DIRAC}}\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \frac{TAUN0}{1+\Gamma_n^{DIRAC}}\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{6}$$

The consequence of BTBT model on I_{off} is examined with the help of Eq. 4. From Eq. 4, the BTBT mainly depends on electric field ($E = E_g^* + \Delta\varphi$), body thickness ($t_{si}$), dielectric constant of material and oxide (ϵ_{si} and ϵ_{ox}) and band gap of material (E_g^*). The BTBT models control the I_{on} under the carrier lifetimes (TAUP0 (for hole) and TAUN0 (for electron)) are used in SRH recombination model with dependency on temperature (T_L term in Eq. 5) and trap energy level (E_{TRAP}). So, we can easily conclude that T variation significantly affects the OFF-state conduction with the SRH model. Similarly, from Eq. 6, we can say that

the TAT model also shows considerable impact on I_{off} because it depends on field-dependent functions (Γ_n^{DIRAC} and Γ_p^{DIRAC}) and all that factor influences SRH model [26].

As we know, due to high T, more number of covalent bond breaks inside the semiconductor lattice and EHPs generated with high thermal energy. Hence, the mobility of carrier gets reduced, and the movement of charge carriers turns in the vibration at a particular coordinate within the lattice. The amount of energy that charge carriers have between two point gets reduced. Consequently, the potential at D–C-I starts decreasing as T increases from 250 to 400 K, shown in Fig. 6a. The E-field is measure of electrostatic force between two charge carriers (either repulsive or attractive). The E-field at D–C-I junction increases with T (Fig. 6b) because generated EHPs significantly increase the minority charge carrier at D–C-I and due to this the electrostatic force between charge carriers increases. But we can see the opposite impact of T at S–C-I junction because carrier concentration is not much affected by generated EHPs and E-field starts decreasing with a rise in T. At thermal equilibrium, the generation and recombination rates balance the net charge carrier density, i.e., total carrier density is constant. As T increases, the generation of carriers is increasing because more covalent bonds are broken at high T [27]. On the other hand, due to mobility saturation, the recombination rate is decreased, as shown in Fig. 6c.

The variation in potential, E-field and recombination rate at D–C-I affects the OFF-state behavior of the proposed device for different models and variations in T. As V_{gs} reduces, TAT and SRH models start showing their existence. For very low V_{gs}, the potential barrier is getting reduced and enables the BTBT mechanism, which helps the carrier to start tunneling across the present barrier. The BTBT, BTBT+SRH, and BTBT+SRH+TAT current components have their region of confinement depending upon E-field at both interfaces (S–C-I and D–C-I) [25]. The BTBT model component is domineering the I_{ds} value under high E-field and shows less sensitivity towards T variation, as mentioned

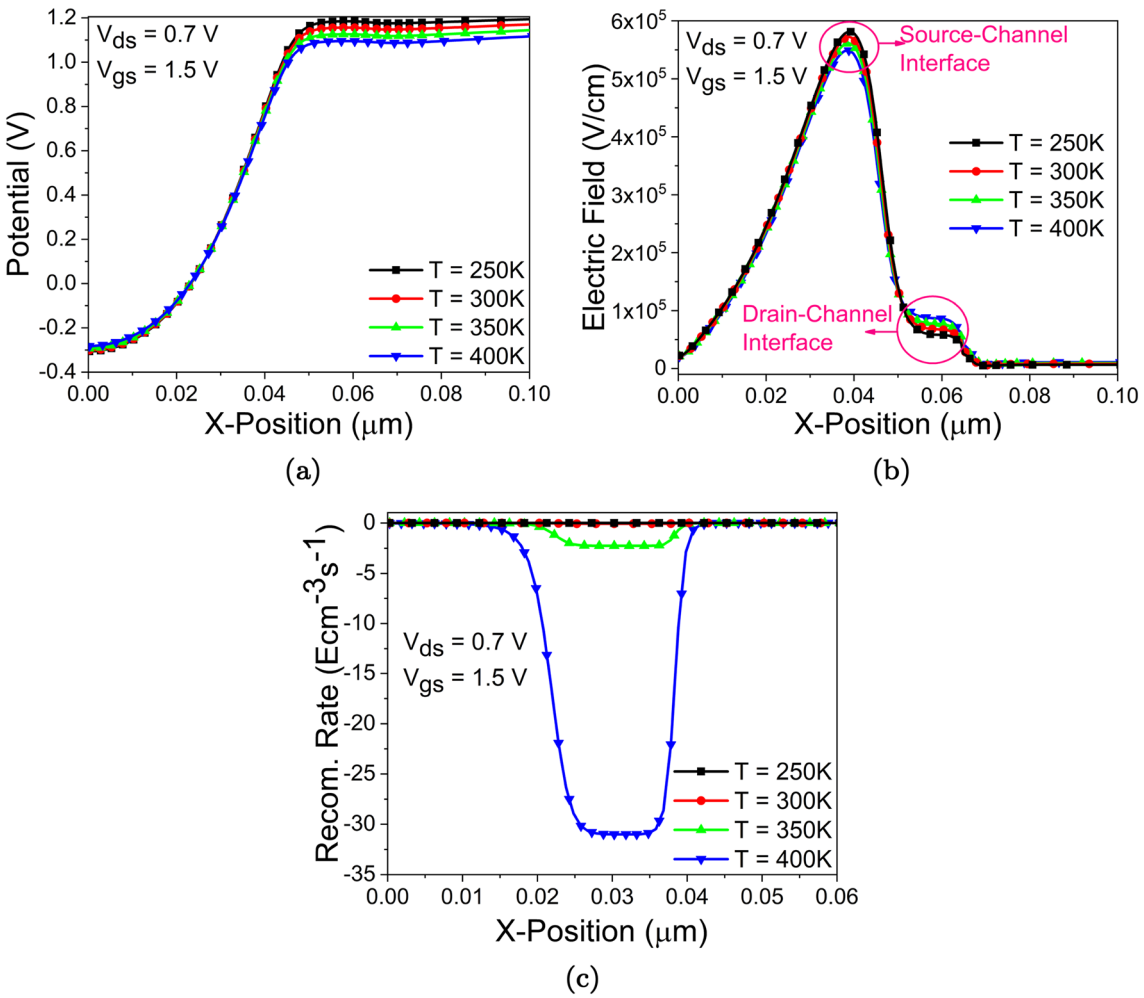


Fig. 6 The impact of T on **a** potential at D–C interface, **b** electric field at both interfaces and **c** variation in recombination rate at D–C-I

in Eq. 4. On the other hand, SRH and TAT models show their presence at low E-field and dominate the I_{ds} range, showing high sensitivity towards changes in T. From Fig. 7, we can examine that due to BTBT model consideration, the change in I_{ambi} is from 10^{-20} to 10^{-16} A/μm (10^4 time) and at T= 300K, I_{ambi} is in the range of 10^{-18} A/μm, which is acceptable for digital circuit application. But, for the SRH and TAT models, $I_{ambi} \approx 10^{-17}$ and 10^{-13} A/μm, respectively, increase when T increases above the $T = 250$ K, as depicted in Fig. 7. So, we can easily conclude that for lower T, SRH and TAT consequences are weak, and the BTBT again becomes a major and effective tunneling mechanism with less sensitivity towards T variation.

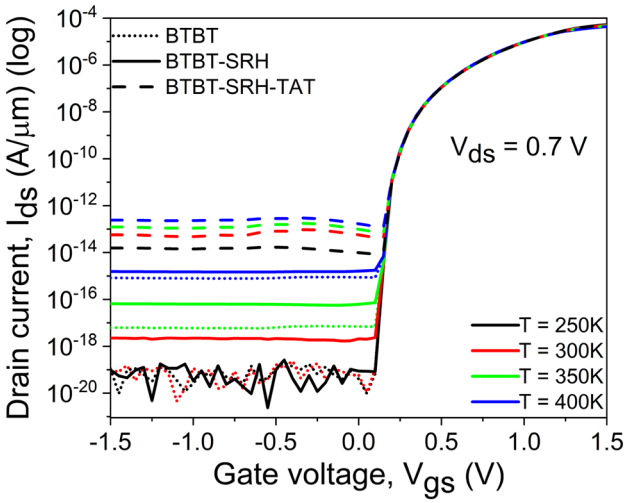


Fig. 7 I_{ds}-V_{gs} graph to analyze the impact of model under different T values

4 Impact on analog/RF parameter

In this section, the consequence of T variations is analyzed w.r.t. different FOMs (figure of merits) associated with high-frequency performance of the proposed device. For RF performance analysis, the first important parameter to be analyzed is parasitic capacitances (gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) capacitance) associated with the device. The C_{gd} and C_{gs} play a crucial role in examining the device performance at high frequency because both are responsible for parasitic oscillation at various frequency ranges [28]. From Fig. 8a, the significant increment can be seen in C_{gd} data plot because the thermally generated charge carriers in channel region help to increase the inversion layer across the channel. Thus, the potential barrier present between the D–C-I gets reduced when T increases from 250 to 400 K. Due to this, a considerable increment is visualized in C_{gd} plot. On the other hand, C_{gs} is reduced as T increases (Fig. 8b) because the potential barrier at S–C-I decreases with an increment in T.

To analyze amplification or current driving capability of SG-F-TFET, the g_m and g_{ds} graph is depicted in Fig. 9 for different T values. The reciprocal of output resistance is known as g_{ds}. For the high amplification ability of a device, g_{ds} should be low. The mathematical expression of g_m and g_{ds} is given in Eqs. 7 and 8.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{7}$$

$$g_{ds} = \frac{\partial I_d}{\partial V_{ds}} \tag{8}$$

From Eq. 7, g_m depends on the slope of $I_{ds} - V_{gs}$ curve, i.e., it can be used to determine the switching speed of the device.

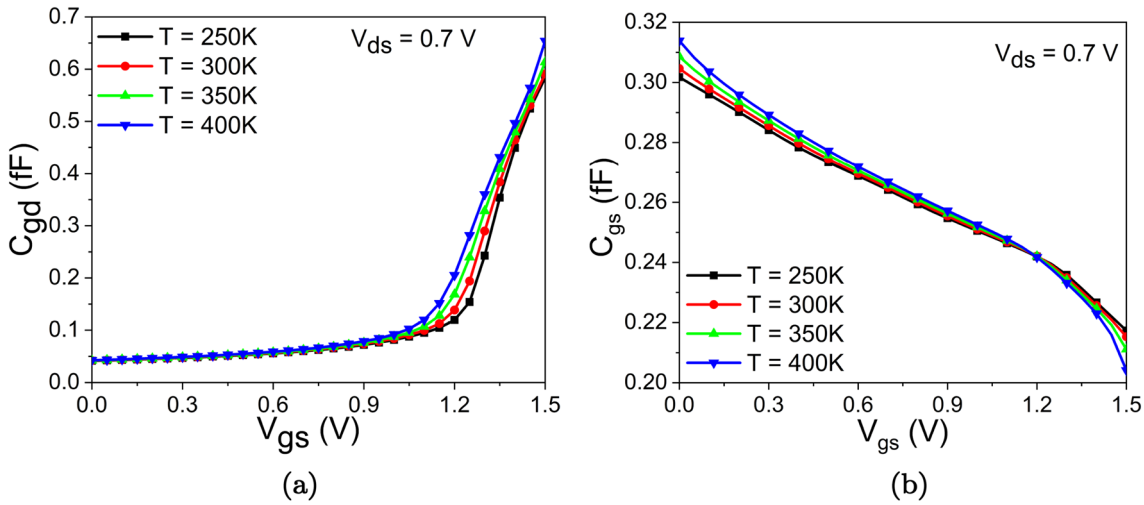


Fig. 8 The variation of parasitic capacitance **a** C_{gd} and **b** C_{gs} for T range from 250 to 400 K

Higher g_m is required for high switching speed. From Fig. 9a we can see that g_m is reduced as T increases because the I_{on} decreases at elevated temperature. On the other hand, g_{ds} shows opposite behavior towards T, i.e., it is increased when T rises from 250 to 400 K with 50 K interval (Fig. 9b), which is not a good sign for amplification ability of the device. Along with this, to analyze the impact of T variation on DC and analog parameters, a comparison of parametric deviations is listed in Table 3.

From Eq. 9, the ratio of g_m and g_{ds} is known as intrinsic gain (IG), which is the maximum voltage gain [29, 30]. In this relation, g_m is dominating factor because g_{ds} is very low as compared to the g_m. Therefore, the impact of T on IG plot is similar to g_m and curve of IG started decreasing as T increases. Similarly, we need to analyze the variation in f_t at which voltage gain and current gain are equal to unity. The f_t is directly proportional to g_m and inversely proportional to total gate capacitance ($C_{gg} = C_{gd} + C_{gs}$), as mentioned in Eq. 10. For the lower V_{gs}, g_m is dominating but as well as V_{gs} increases, C_{gg} become dominating parameter. Thus, f_t curve starts decreasing after attaining peak because of high C_{gg} at higher V_{gs}. From Fig. 10b, the f_t curve shifted downward as T increases above the room temperature because variation in g_m is very high as compared to C_{gd} and C_{gs} when T increases.

$$Intrinsic\ gain = \frac{g_m}{g_{ds}} \tag{9}$$

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{10}$$

Another crucial parameter for RF analysis is TT depicted in Eq. 11. It is inversely proportional to f_t. The TT increases

Table 3 Observation of physical parameters for different temperatures

Physical parameters	Temperature			
	250K	300K	350 K	400 K
E-Field (V/cm)	5.8×10^{5}	5.4×10^{5}	5.4×10^{5}	5.1×10^{5}
Potential (V)	1.2	1.15	1.1	1.09
I_{on} A/μm	1.61×10^{-5}	7.719×10^{-5}	4.67×10^{-5}	3.84×10^{-5}
I_{off} A/μm	2.17×10^{-20}	3.10×10^{-18}	6.17×10^{-17}	1.41×10^{-15}
I_{on}/I_{off}	7.45×10^{15}	2.49×10^{13}	7.56×10^{11}	2.73×10^{10}
I_{ambi} A/μm	7.12×10^{-21}	2.01×10^{-18}	6.18×10^{-17}	1.601×10^{-15}
SS (mV/decade)	9.8	14.1	14.6	15.5
$V_{th}(V)$	0.45	0.49	0.51	0.52
C_{gd} (fF)	0.57	0.59	0.61	0.65
C_{gs} (fF)	0.219	0.214	0.210	0.204
g_m (mS)	0.19	0.094	0.088	0.078

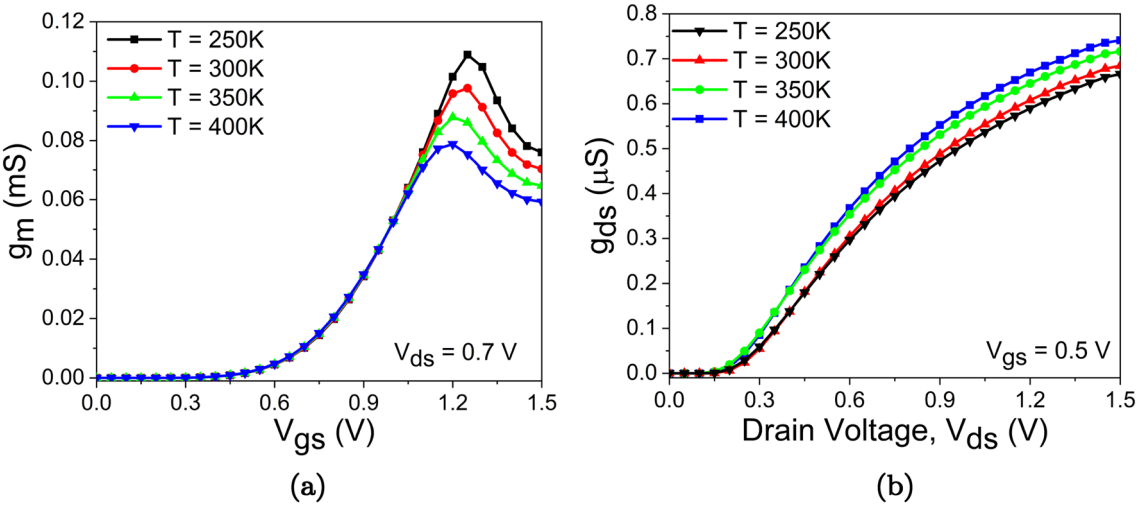


Fig. 9 The data plot of **a** g_m and **b** g_{ds} for different T values

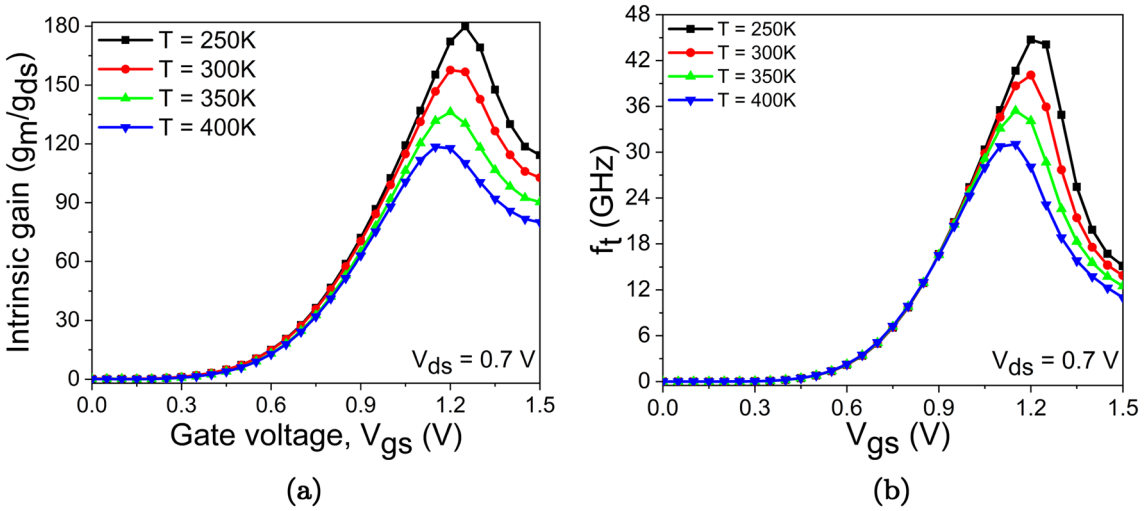


Fig. 10 The data plot of **a** intrinsic gain and **b** f_t for different T values

for reducing f_t values, and the speed of SG-F-TFET increases because of reduced delay [17, 31]. But for higher T values, TT has reduced because f_t decreases when T increases from 250 to 400 K, as illustrated in Fig. 11b. Furthermore, the mathematical equation for GBP is given in Eq. 12, which shows the dependency of GBP on g_m and C_{gd}. The GBP data plot of SG-F-TFET is illustrated in Fig. 11a for various T values. From this, we examine that the GBP decreases with T and attains its extreme point earlier, and after that, it starts decreasing because g_m decreases and C_{gd} increases.

$$TT = \frac{1}{2\pi f_T} \tag{11}$$

$$GBP = \frac{g_m}{2\pi C_{gd}} \tag{12}$$

The mathematical expression of TFP and TGF is given in Eqs. 13 and 14. TFP and TGF are key parameters to consider when calculating device efficiency and the trade-off between operating bandwidth and power dissipation [32, 33]. The TFP and TGF data plot with T variation is depicted in Fig. 12a, b, respectively. From Fig. 12b, the TFP deteriorates at high T, and the maximum peak of TFP is shifted towards lower V_{gs} because the mobility of charge carrier at high T decreases. Similarly, the impact of T variation on TGF plot is portrayed in Fig. 12a. From Eq. 14, it inversely depends on I_{ds} and directly proportional to g_m. Therefore,

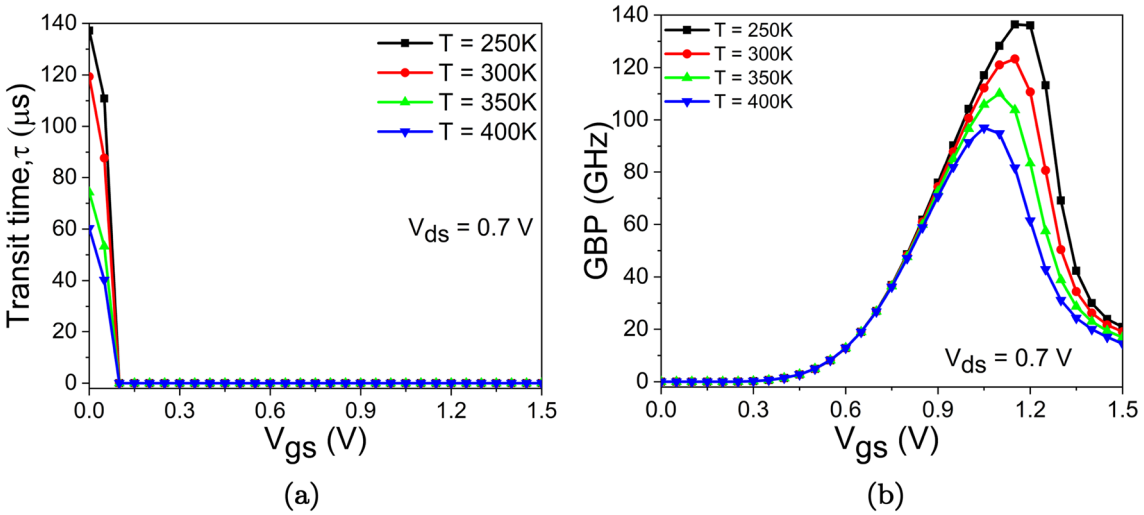


Fig. 11 The graph of **a** transit time and **b** GBP to examine the impact of T variation

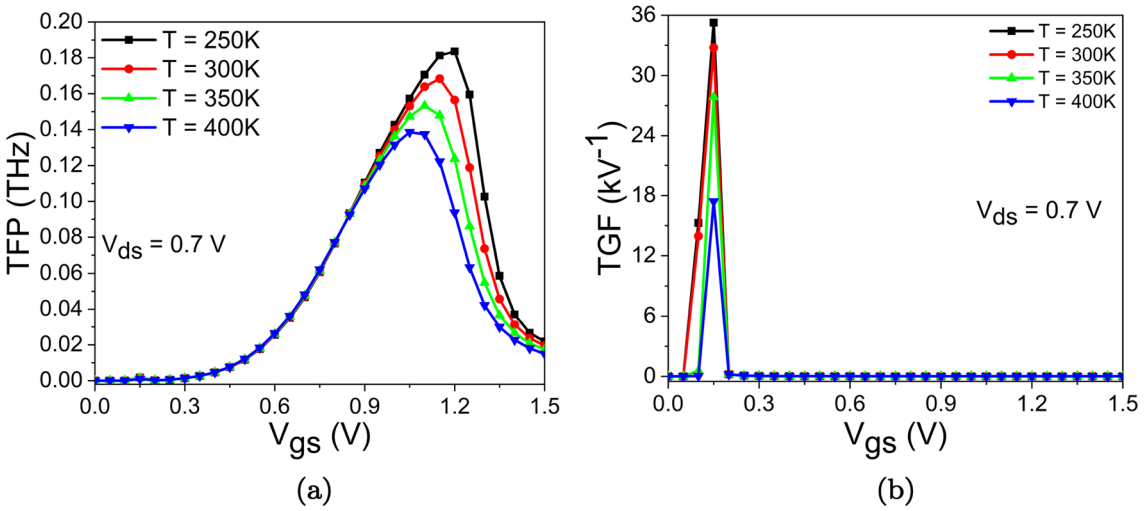


Fig. 12 The variation of **a** TFP and **b** TGF with respect to V_{gs} for different T values

TGF is reduced with a rise in T because of decrement in g_m and I_{ds} values.

$$TFP = \frac{g_m f_T}{I_d} \tag{13}$$

$$TGF = \frac{g_m}{I_d} \tag{14}$$

5 Impact on linearity performance

In the recent trend of device and circuit applications, high I_{on}, high I_{on}/I_{off} ratio, low V_{th} and lower values of SS with suppressed I_{ambi} ($10^{-18}\, A/\mu m$) are not only essential parameters to analyze the device behavior. Linearity analysis of the device is an additional quality checking stage, at which the device is used in the circuit and checks the linear relation between input and output. Any nonlinear power series can be written in the following form by using the Volterra series:

$$V_{out} = a1V_{in} + a2V_{in}^2 + a3V_{in}^3 + \cdots \tag{15}$$

In Table 4, different frequency components of desirable inter-modulated (IMS) and harmonics signal are listed. The desired frequency is f_1 and f_2 with the second- and third-order components. As integral multiples of fundamental frequency give harmonic distortion that can be filtered, they are very far from the desirable range. The IMS of $f_1 \pm f_2$ is very close to original frequencies and is hard to remove [34]. The small-signal model (SSM) of output current in terms of nonlinear g_m for V_{gs} can be expressed similar to Eq. 15 and given by

Table 4 Nonlinear frequency components

Components	Parameters	Frequencies
Actual Signal	Fundamental	f_1, f_2
Second order	HD2	$2f_1$, $2f_2$
	IM2	$f_1 \pm f_2$
Third order	HD3	$3f_1$, $3f_2$
	IM3	$2f_1 \pm f_2$

$$I_{ds} = g_m V_{gs} + g_{m2} V_{gs}^2 + g_{m3} V_{gs}^3 + \cdots \tag{16}$$

The relation between I_{ds} and V_{gs} should be linear, but when the V_{gs} increases, the I_{ds} is saturated because of the mobility saturation of charge carriers and due to this g_m decreases. As a conclusion of Eq. 16, it is clear that higher-order g_m derivatives (g_{m2} and g_{m3}) should be as minimum as possible for the device to be linear [35]. A detailed investigation of linearity FOMs of SG-F-TFET device under the T variation from 250 to 400 K is performed in this section.

5.1 Harmonic distortions

The mathematical expression of second- and third-order derivatives of g_m is given in Eqs. 17 and 18, respectively, which are responsible for harmonic distortion and affects the device performance when used in circuit application [36]. The g_{m2} and g_{m3} should be low to maintain the linear behavior of SG-F-TFET device. The variation of g_{m2} and g_{m3} with respect to V_{gs} for different T values is depicted in Fig. 13a, b. The zero cross over point is the value of V_{gs} at which g_{m2} and g_{m3} become equal to zero, which are defining the optimal bias point for device linear operation and both increase with V_{gs}. g_{m2} and

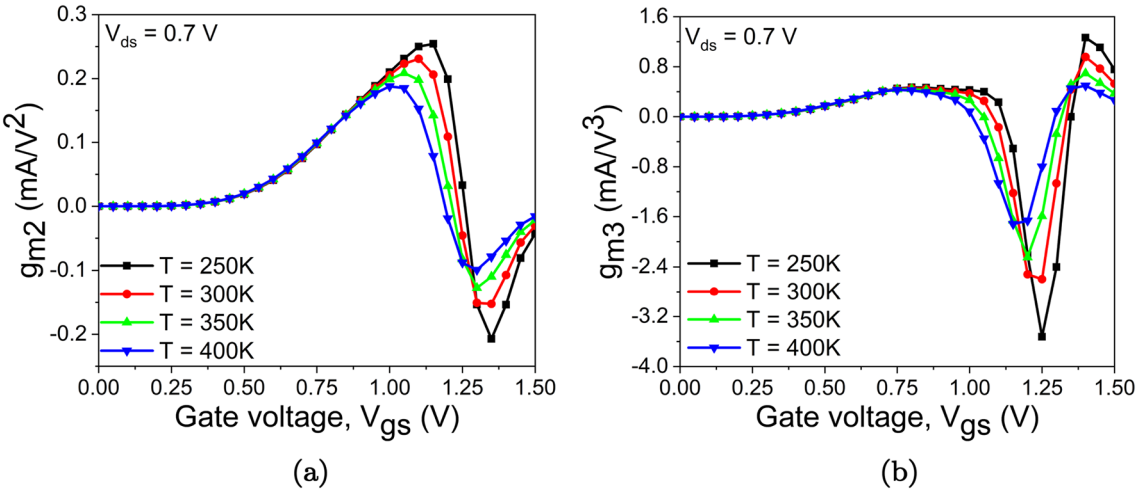


Fig. 13 The graph of **a** g_{m2} and **b** g_{m3} for different T values

g_{m3} values low for lower T, as shown in Fig. 13. Hence, lower T provides improved linearity performance with suppressed second- and third-order harmonics of g_m.

$$g_{m2} = \frac{\partial^2 I_d}{\partial^2 V_{gs}} \tag{17}$$

$$g_{m3} = \frac{\partial^3 I_d}{\partial^3 V_{gs}} \tag{18}$$

5.2 Second- and third-order intercept point

In this section, we examine the effect of T variation on the second-order voltage intercept point (VIP_2), third-order voltage intercept point (VIP_3) and third-order input intercept point (IIP_3). From Eq. 19, VIP_2 is the four times of the ratio of g_m and g_{m2}. As we discussed earlier, for better device performance we need high g_m and low g_{m2}, so larger value of VIP_2 is intended to insure better linearity of SG-F-TFET. The value of VIP_2 decreases, while T increases from 250 to 400 K, shown in Fig. 14a. Therefore, VIP_2 can be obtained for lower T.

$$\mathrm{VIP}_2 = 4\left(\frac{g_m}{g_{m2}}\right) \tag{19}$$

From Eq. 20, VIP_3 directly depends on g_m and inversely on g_{m3}, so higher value of VIP_3 is desired to ensure suppression of the third-order harmonics with lower value of g_{m3}. VIP_3 improves as T increases above the room temperature, as illustrated in Fig. 14b. The peak of VIP_3 is shifted towards lower V_{gs} as T increases, which helps to improve linearity of proposed device and it can be achieved at a lower bias point. This indicates that the proposed device has low power consumption.

$$\mathrm{VIP}_3 = \sqrt{24\left(\frac{g_m}{g_{m3}}\right)} \tag{20}$$

The mathematical expression of IIP_3 is shown in Eq. 21, where $R_s = 50\ \Omega$ for analog and RF application. For better linearity performance, IIP_3 should be high because for this we need low g_{m3} and high g_m with fixed value of R_s. For lower V_{gs} (0 to 0.25 V), IIP_3 is improved when T increases, but for higher values of V_{gs}, it shows asymmetric behavior towards T variation. The 1^{st} and 2^{nd} peaks of IIP_3 occur for $T = 350$ K and $T = 250$ K, respectively. So, better IIP_3 can be achieved at high T.

$$IIP_3 = \frac{2}{3}\left(\frac{g_m}{g_{m3}R_s}\right) \tag{21}$$

5.3 Intermodulation distortion and 1-dBm point

Equations 22 and 23 show the mathematical expressions of third-order intermodulation distortion (IMD_3) and 1-dB compression point (1-CP), respectively. The IMD_3 is directly proportional to the product of $(VIP_3)^4$ and $(g_{m3})^2$, so reduced value of g_{m3} helps to achieve the lower range of IMD_3. Minimum value of IMD_3 indicates better immunity towards the third-order intermodulation harmonics and helps to prevent wastage of usable power. From Fig. 15a, IMD_3 increases with T, leading to degradation of device performance.

$$\mathrm{IMD}_3 = \left[\frac{9}{2}(\mathrm{VIP}_3)^2 g_{m3}\right]^2 R_s \tag{22}$$

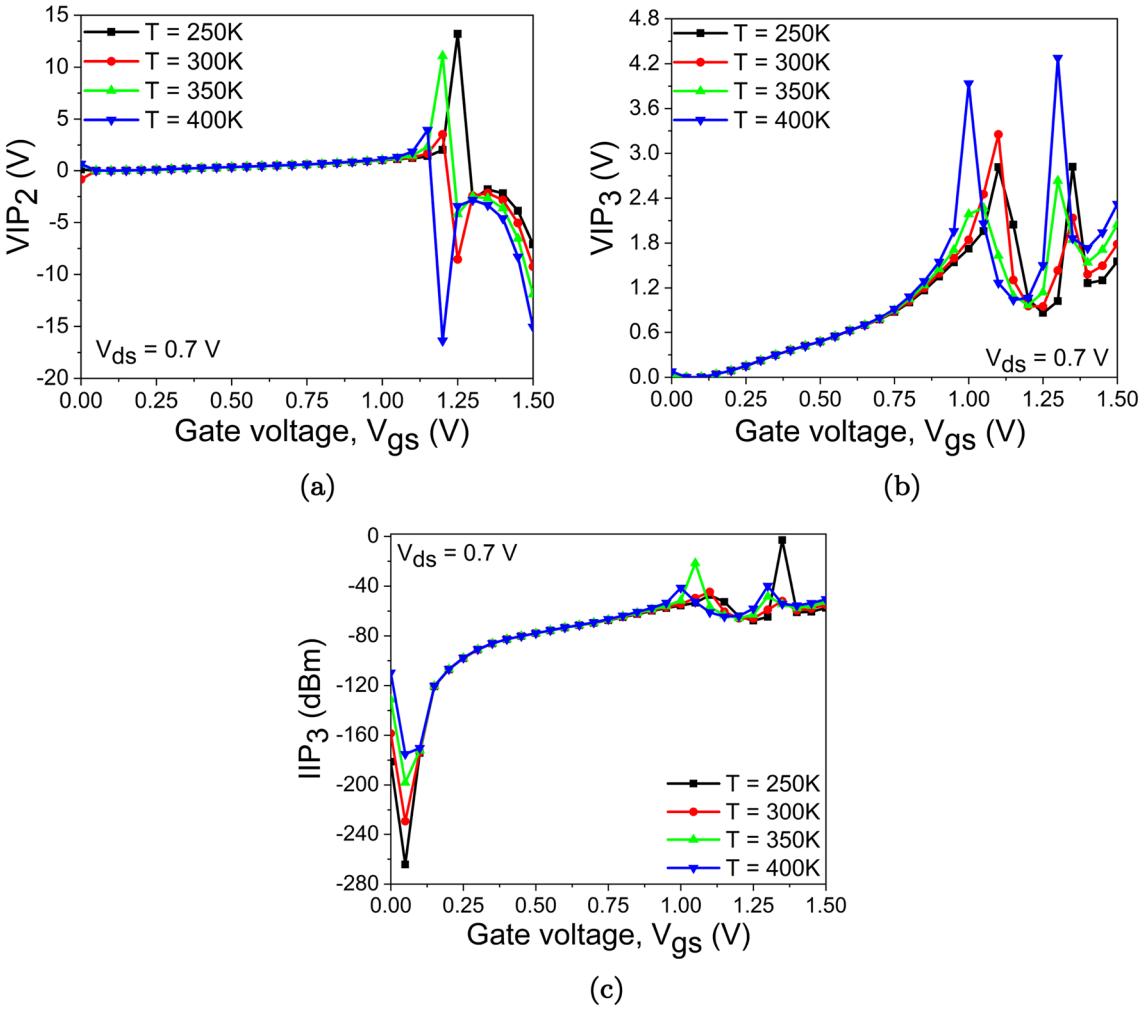


Fig. 14 The data plot of **a** VIP_2, **b** VIP_3 and **c** IIP_3 for different T values

$$1dB\,\text{compression point} = 0.22\sqrt{\frac{g_m}{g_{m3}}} \tag{23}$$

Another vital parameter to consider when determining the device's linearity efficacy is the 1-CP. A high value of 1-CP is desired because it specifies the input power level at which the output power reduces to 1 dB from the linear gain region. It is used to calculate the highest input power, after which the device's gain reduces. 1-CP enhanced as T increases above 250 K, which is a good sign.

6 Reliability analysis

This section highlights the reliability concerns of proposed device over a wide T range of 250 to 400 K. In Sect. 3, we have seen that the impact of T variation on I_{on} is very low and I_{on} and V_{th} reduces as T increases. On the other hand, I_{ambi} and SS value of the proposed device increase with temperature. The I_{on}/I_{off} ratio decreases dramatically with increasing T. Similarly, in Sect. 3.1, study on OFF-state elaborates that ambipolar behavior of the proposed device is increased with T because of strong dependency of SRH and TAT model on temperature. The variation in T also affects the high-frequency performance parameters. The percentage deviation in analog and RF parameters is analyzed and depicted in Fig. 16a with the help of a pie chart. The same way, impact on linearity parameters is illustrated in Fig. 16b. Therefore, after a detailed study of ON- and OFF-state, high frequency, and linearity performance of the proposed device, it can be concluded that SG-F-TFET shows better reliability in the range of 250 to 350 K temperature.

7 Conclusion

In this extensive study, TFET with ultra-thin finger-like source region is introduced and investigated under various T ranges from 250 to 400 K with 50 K interval. This proposed

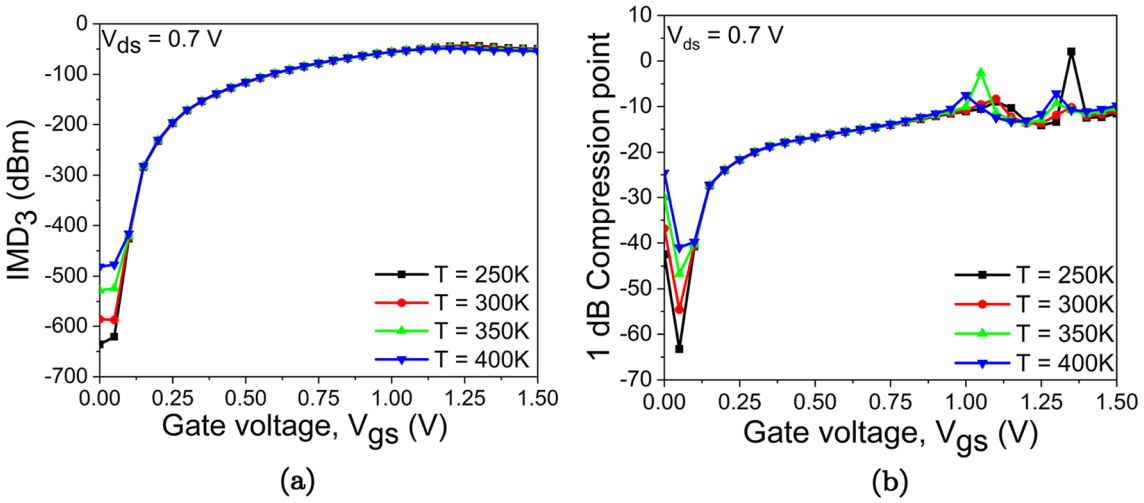


Fig. 15 The data plot of **a** IMD_3 and **b** 1-CP for different T values

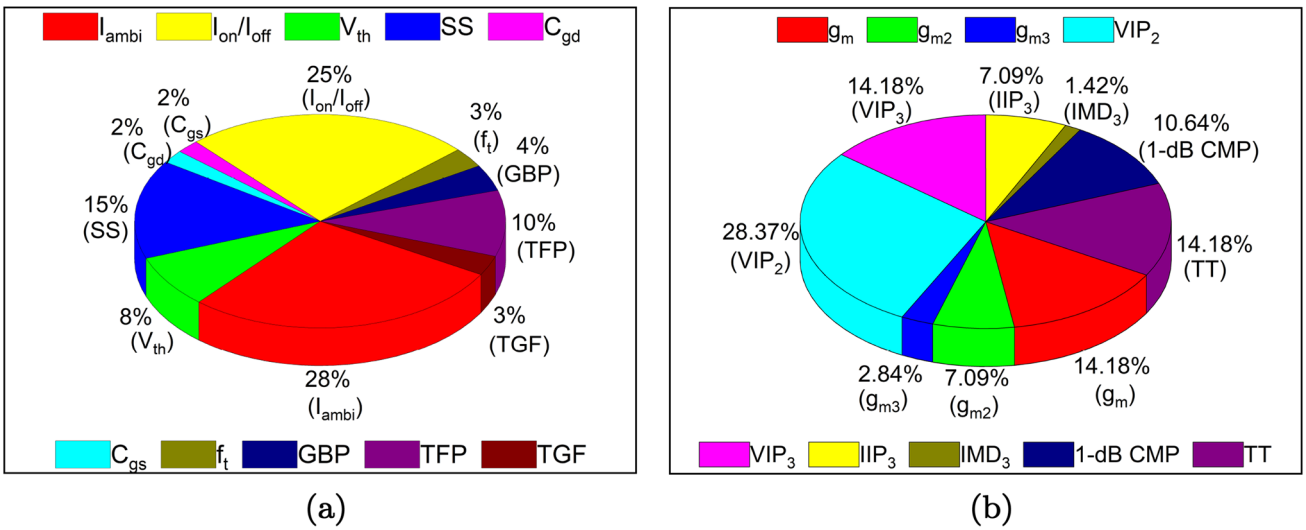


Fig. 16 Deviation in **a** analog/RF parameters and **b** linearity parameters of SG-F-TFET for T fluctuations

device overcomes the limitation of conventional TFET in terms of high I_{on} ($5.45 \times 10^{-4}\ A/\mu m$), lower V_{th} (0.60 V) and optimum SS (10.08 mV/decade) at $T = 300$ K. Further, impact of T is examined in ON-state conditions, OFF-state conditions, RF performance, and linearity performance parameters. It has been analyzed that I_{on} and C_{gg} show less sensitivity towards T variations. Hence, SG-F-TFET can be a promising device for ultra-low power and RF applications. On the other side, the impact of T on off-state current is very high, which deteriorates the device performance for digital circuit application. The increase in T reduces the impact of BTBT current component, and TAT and SRH current components get more superiority in the proposed device's OFF-state condition. Due to this effect, the I_{on}/I_{off} ratio drastically reduces because I_{off} increases with the rise in T. Besides, the influence of T variation on RF parameters is also examined, to check the device performance for high-frequency applications, and we find that the sensitivity of RF parameters towards T variation is less. Linearity and reliability analysis is carried out to examine robustness of SG-F-TFET under various environmental conditions. We found that SG-F-TFET shows superior response in the T range of 250 to 350 K.

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