Applied Physics A (2020) 126:935
https://doi.org/10.1007/s00339-020-04086-0

Applied Physics A
Materials Science & Processing

On the electrical characteristics of Al/p-Si diodes with and without (PVP: Sn-TeO_2) interlayer using current–voltage (*I–V*) measurements

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Received: 1 August 2020 / Accepted: 17 October 2020 / Published online: 12 November 2020

Abstract
The present study aims to investigate the effect of (PVP: Sn-TeO_2) interfacial layer on the electrical parameters of the Al/p-Si diode. For this aim, (Sn-TeO_2) nanostructures were developed by the ultrasound-assisted method, and both their electrical and optical characteristics were investigated by XRD, SEM, EDS, and UV–Vis methods. The bandgap of Sn-TeO_2 was found as 4.65 eV from the $(\alpha h\upsilon)^2$ vs $(h\upsilon)$ plot. The main electrical parameters of the Al/p-Si diodes with/ without (PVP: Sn-TeO_2) interlayer, such as ideality factor (n), zero-bias barrier height (Φ_0), and series resistance (R_s), were calculated by applying and comparing two methods of thermionic emission theory and Cheung's functions. These results show that the presence of the (PVP: Sn-TeO_2 interlayer, along with the increase of Φ_0, and the decrease of n and R_s, led to a significant increment in the rectification of MPS when compared to MS diode. The current-transport mechanisms (CTMs) of them were examined through the forward $\mathrm{Ln}I_F - \mathrm{Ln}V_F$ and reverse $\mathrm{Ln}I_R - V_R{}^{0.5}$ bias currents, and then, the Poole–Frenkel and Schottky field-lowering coefficients (β) were calculated and obtained its value from the theoretical and experimental methods showed that the mechanism of the reverse current of MS and MPS diodes is governing by the Schottky emission and Pool-Frenkel mechanism, respectively.

Keywords Interfacial layer · PVP · Tin telluride oxide (Sn-TeO_2) · Schottky diodes · *I–V* characteristics · Poole–Frenkel emission

1 Introduction

Metal–semiconductor (MS) contacts with/without an interfacial layer, which play a key role in the present-day technology, are used in components such as microwave detectors (MDs), solar cells (SCs), field-effect transistors (FETs), and varactor or photodiodes (VDs/PDs). In MS structure, the conductivity or current transport mechanism depends on various factors such as surface preparation, barrier formation at M/S interface and its homogeneity, density of surface states (N_{ss}) at M/S interface which have energies in the bandgap interval of the semiconductor, doping concentration of donor/acceptor atoms (N_D/N_A), temperature, frequency, applied voltage, etc. [1–6]. When a polymer or insulating layer is placed between metal and semiconductors by various techniques, MS diode converts to MIS or MPS type diodes and leads to changes in both the electrical and dielectric properties. Therefore, recently, they were used in a wide range of electronics and optoelectronics applications. Such

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an interfacial layer may be created or passivated many traps or states at M/S interface and changes the current conduction mechanism of the structure by trapping and releasing free charge carriers. Also, these levels/traps, in turn, change the efficiency and rectification of the diode by affecting parameters, e.g., n, R_s, and barrier height (BH) [7, 8].

Tin telluride (SnTe) is an IV–VI semiconductor with a narrow bandgap of 0.18 eV. SnTe belongs to a new class of topological crystalline insulators (TCIs) and has a band degeneracy. SnTe is a thermoelectric material that shows interesting optical and electronic properties. This substance could be used in mid-IR photodetectors and thermoelectric generators when is slightly doped [9, 10]. Tellurium dioxide (TeO_2) has also a wide band-gap semiconductor that can be used in gas sensors, deflectors, optical memories, optical filters, and waveguides owing to its special electro-optical and acoustic-optical properties [11–17]. On the other hand, polymers have long-chain molecules and are used in electronic components, instead of insulators, due to their merits, e.g., easy preparation, low cost, lightness, etc. As they have limited conductivity, some efforts have been recently made to increase their conductivity using metal atoms and metal oxides, as well as doping. Among polymers, polyvinylpyrrolidone (PVP) has unique advantages, including easy thin-film preparation, flexibility, adjustable conductivity and resistivity, relatively high environmental stability, non-toxic properties, low cost, and good conductivity. Thus, it is a potential alternative to traditional layers in diodes and capacitors [18, 19].

The main aim of this study is to investigate the effect of (PVP: Sn-TeO_2) interlayer on the electrical characteristics of the Al/p-Si diode. For this purpose, (Sn-TeO_2) were fabricated by the Microwave-assisted method and both their electrical and optical characteristics were investigated by XRD, SEM, EDS, and UV–Vis methods. After that n, Φ_0, R_s values of them were calculated from the TE emission and Cheung's functions and compared. The CTMs of them were also investigated the forward and reverse bias region. These results show that the existence of the (PVP: Sn-TeO_2 interlayer leads to an increase of Φ_0, and a decrease of n and R_s. The value of RR for the MPS diode was also found significantly higher than the MS diode.

2 Experimental procedure

Sn-TeO_2 nanostructures were prepared using the microwave-assisted method. To do this, the sodium tellurite (Na_2TeO_3) and tin (II) chloride ($SnCl_2$) precursors were purchased from Loba Chemie Co. 20 ml of 0.2 M solution of both precursors were prepared with distilled water and mixed. The pH of the sodium tellurite and tin chloride solutions were 10 and 2, respectively, and reached 8 after being mixed. The resulting mixture was exposed to 180 W microwave irritation for 15 min. After the washing step, the resulting mixture was placed in an oven at 40 °C for 45 h to be dried.

The relevant tests for investigating the structural, optical, electrical, and dielectric characteristics of prepared nanostructures and diodes were performed using an X-ray diffractometer (Philips, X $\lambda = 1.5406$ Å), FESEM (Tescan-Mira III, Czech Republic), ultraviolet–visible spectroscope (UV-1800, Shimadzu, Japan), KEYSIGHT (E4980Al 20 Hz–1 MHz) and KEITHLEY 2450 source-meter, respectively. The PVP: Sn-TeO_2 interfacial layer was deposited on the p-type silicon using the spin coating technique. 10 mg nanostructures were used for this layer, whereas the concentration of water-soluble PVP was 5%. Before the deposition process, the surface was prepared for deposition and various solutions were used to wash the silicone surface, as described in Ref. [8].

3 Results and discussion

3.1 Structural analysis

The structural and morphological features of prepared nanostructures are shown in Fig. 1a and b, respectively.

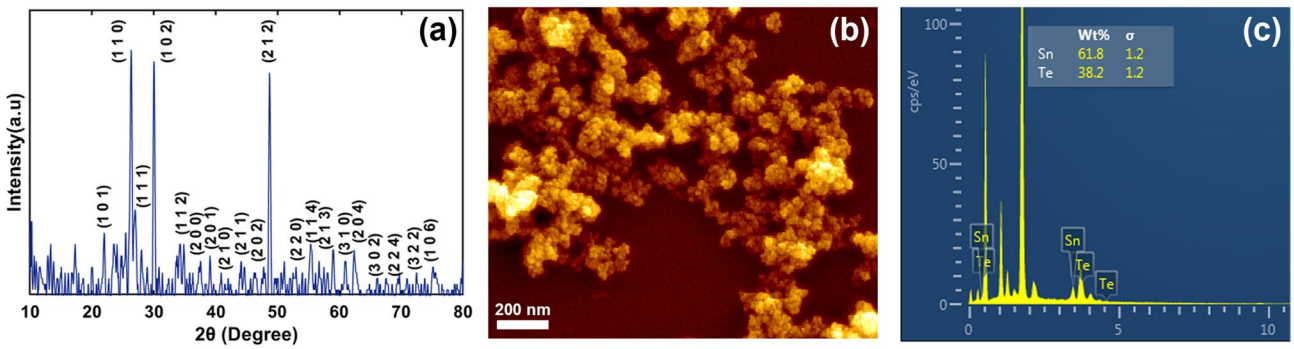

Fig. 1 **a** X-ray diffraction pattern, **b** FESEM image and **c** EDS spectrum of Sn -TeO_2 nanostructures

According to Fig. 1a, the diffraction peaks at $2\theta = 26.3°$ and 48.7° belong to (110) and (212) crystalline planes of the tetragonal structure of TeO_2 [20], which are related to the P41212 space group with parameters of $a = b = 4.8$ Å and $c = 7.6$ Å. This is in agreement with the standard XRD PDF card (ICSD # 01-084-1777). Also, the diffraction peak at $2\theta = 30.1°$ is matched with the standard XRD PDF card (00-046-1210) related to the cubic structure of SnTe, which belongs to the Fm3m space group with lattice parameters of $a = b = c = 6.3$ Å. The average size of nanostructures is calculated by the following equation:

$$D = K\lambda/\beta\cos(\theta) \tag{1}$$

where D is the crystal size (nm) and the rest of the parameters are defined in the previous report. According to Eq. (1), the average sizes of TeO_2 [related to (110) and (212) crystal plates] and SnTe nanoparticles were estimated at 31 nm and 41 nm. Figure 1b presents the FESEM image and EDS spectrum of the sample. As shown, the nano-clusters have dimensions of less than 200 nm and are composed of almost spherical nanoparticles with an average size of 40 nm. Also, the EDS analysis shows that the nanostructures contain only Te and Sn elements (Fig. 2).

The optical characteristics of nanostructures were evaluated using the ultraviolet–visible spectroscopy (UV-1800, Shimadzu, Japan) and their energy gap was calculated by the linear part of $(\alpha h\nu)^2$—photon energy $(h\nu)$ plot:

$$\alpha h\nu = B\left(h\nu - E_g\right)^n \tag{2}$$

where B is a constant, α is the absorption coefficient, and the value of n is 2 and 0.5 for indirect and direct transitions, respectively. According to Eq. (2), the energy gap of Sn-TeO_2 nanostructures for direct transition is 4.65 eV. Figure 2a and b show the absorption spectrum and the energy gap plot of the prepared sample, respectively.

3.2 Electrical characteristics

The electrical characteristics of MS and MPS diodes were investigated by measuring current and voltage using the KEITHLEY 2450 source-meter instrument. Figure 3a and b exhibit the I–V curves of MS and MPS diodes in the voltage range of ± 4.5 V at ambient temperature, respectively. As seen in Fig. 3, both diodes have a Schottky contact behavior, which means that they have a rectifying behavior with a very small leakage current in the reverse bias region. It is also observed that the MPS diode has a much better rectifying behavior rather than the MS one. In the direct bias region of the I–V curve at low voltages, the number of current increases exponentially with voltage, which is due to the depletion layer width in the M/S interface. At higher voltages, the current increases linearly because the depletion layer width is minimized, and as a result, the (PVP: Sn-TeO_2) interfacial layer acts as a series resistance. In the reverse bias region, a small current passes through the diode thanks to the increased depletion layer width, and also, because the whole current is caused by the minority carriers of the interfacial layer.[21] As indicated in Fig. 3b, the leakage current of the MPS diode is much lower than that of the MS one owing to the presence of an interfacial layer. The current–voltage equation of the Schottky junctions ($V > 3kT/q$) is expressed according to the thermionic emission (TE) theory as follows [22]:

$$I = I_0\left[\exp\left(\frac{q\left(V - IR_s\right)}{nkT}\right) - 1\right] \tag{3}$$

where I_0 is the reverse-saturation current, which can be calculated from the intercept of the LnI–V plot at $V = 0$. The

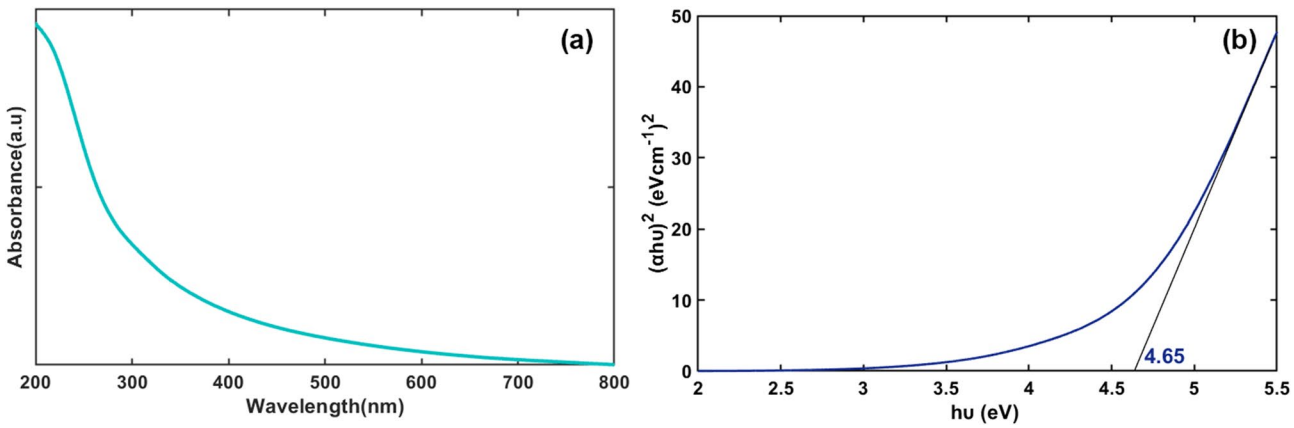

Fig. 2 **a** UV-Vis spectra of the prepared nanostructures and **b** The $(\alpha h\nu)^2$ vs $(h\nu)$ plot

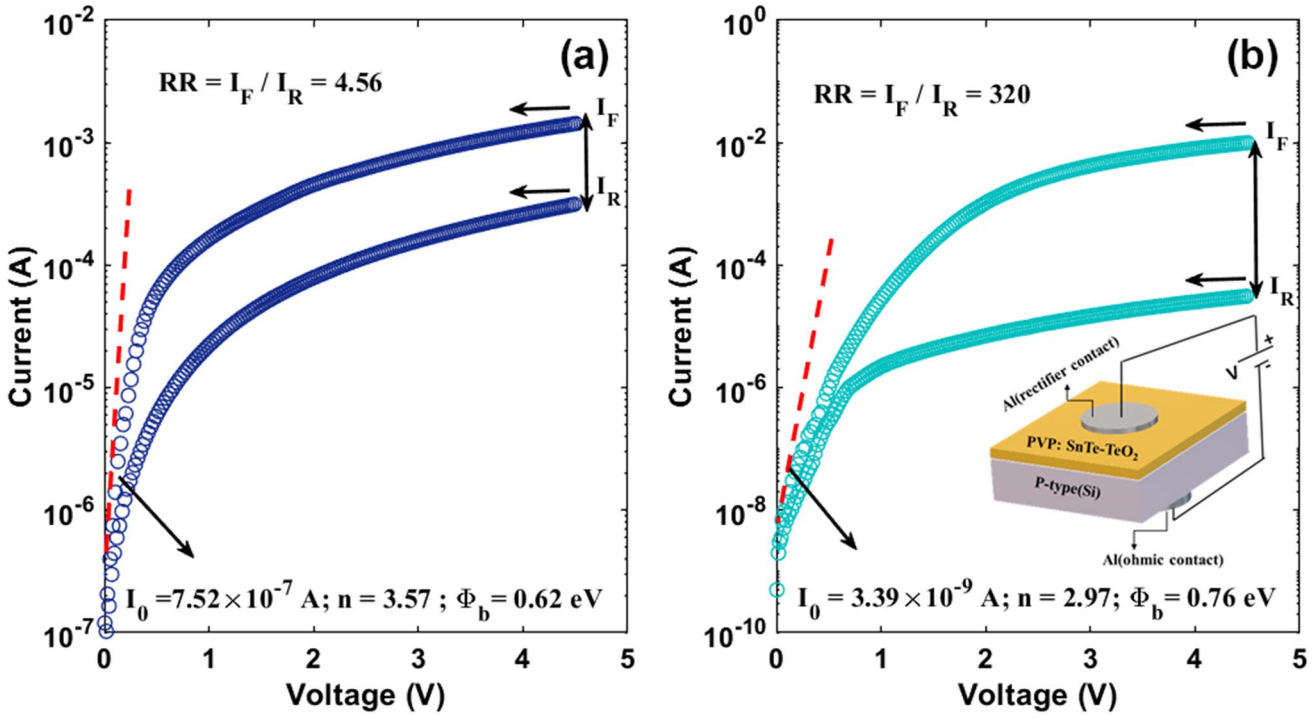

Fig. 3 The *I–V* plot of **a** MS and **b** MPS type SBDs

estimated values of leakage current for MS and MPS diodes were 7.52×10^{-7} A and 3.39×10^{-9} A, respectively. The barrier height and the ideality factor can be calculated through the obtained leakage current and the slope of the Ln*I–V* plot, according to Eq. (4):

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{B0}}{kT}\right) \tag{4a}$$

$$n = \frac{q}{kT}\left(\frac{dV}{d(\mathrm{Ln}I)}\right) \tag{4b}$$

Thus, the value Φ_{B0} was calculated from the Eq. (4a) using the experimental value of I_o and rectifier contact area (A) and the other parameters have been introduced in previous works [8, 23, 24]. The calculated Φ_{B0} of the MS and MPS diodes are 0.62 eV and 0.76 eV, respectively. The ideality factor, which indicates the degree of deviation from the thermionic emission theory, is determined by 3.57 and 2.97 for the MS and MPS diodes, according to Eq. (4b), respectively. As is clear, both of these values are greater than one. In general, the value of n is dependent on interfacial layer thickness (d_i) and its permittivity (ε), depletion layer width (W_d) or doping concentration atoms, and surface states as $n = 1 + d_i/\varepsilon_i d_i[\varepsilon_s/W_d + q\mathrm{Nss}]$. In this case, the applied bias voltage on the diode will be shared by the interfacial layer, R_s, and depletion layer [25, 26]. The existence of barrier inhomogeneity is the other reason for higher ideality factor states [2–4].

To determine the transport mechanism of charge carriers and diode behavior in direct and reverse bias, Ln (I_F) − LnV_F and Ln (I_R) − V_R plots of both MS and MPS diodes are presented in Fig. 4a and b. Figure 4a shows that the plot has two and three linear sections with different slopes for the MS and MPS diodes, which are named I, II, III. The current conduction/transport mechanisms differ from one region to another due to various factors, e.g., BH heterogeneity, R_s, and density of Nss [7, 8].

As seen, the dependence of the current on the voltage has as an exponential relation: $I \sim V^m$, where m is related to the slope of each region. The slopes of regions I, II, III for the MS diode (region I: $0.01 < V < 0.10$ V, region II: $0.21 < V < 0.40$ V, and region III: $0.48 < V < 4.50$ V) are 1.49, 2.79, and 1.45, while the relevant values for the MPS diodes (region I: $0.03 < V < 0.28$ V, region II: $0.38 < V < 2.28$ V, region III: $2.60 < V < 4.50$ V) are 1.35, 5.07, and 2.27, respectively. The slopes of regions I, III of the MS diode, and the slope of the region I of the MPS diode, are close to one, and the current is directly proportional to the applied voltage, indicating the ohmic behavior of the diodes in the aforementioned region. In this region, the current follows $i = qn\mu V/d$, where n, μ, d, are the density of free carriers, mobility, and thickness of the interfacial polymer

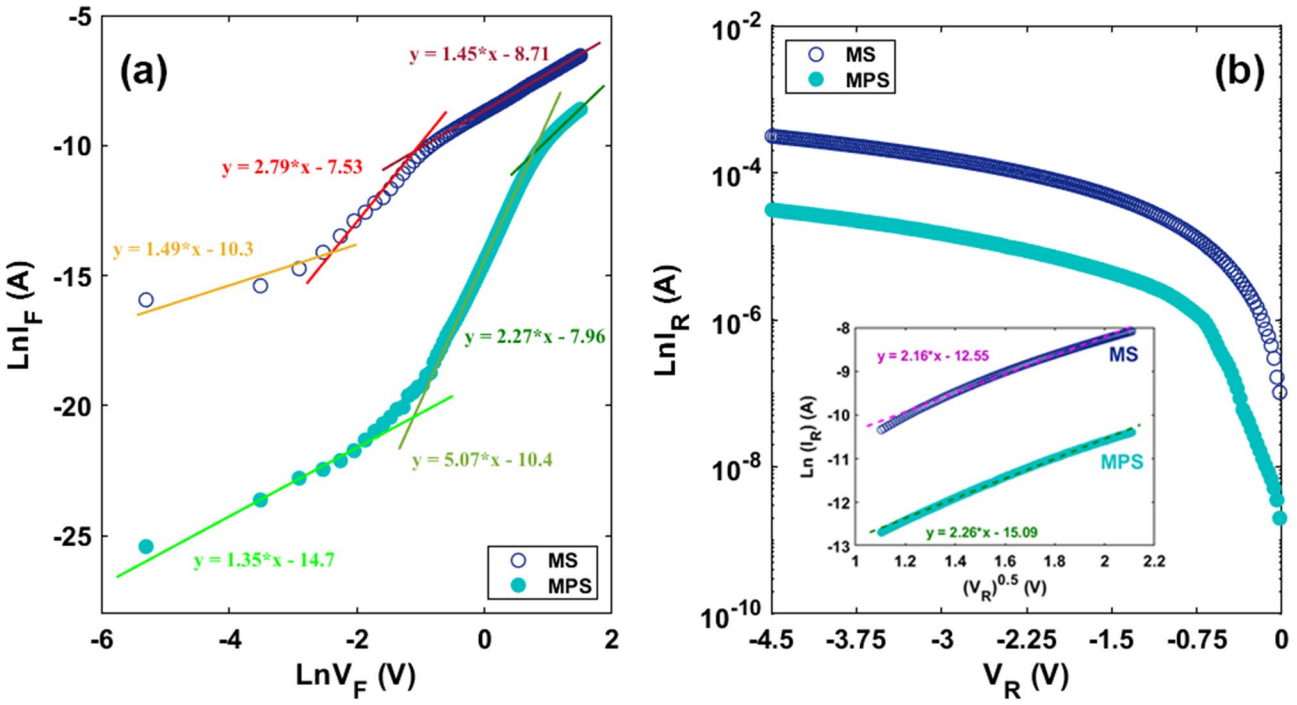

Fig. 4 the plots of **a** $\mathrm{Ln}I_\mathrm{F} - \mathrm{Ln}V$, **b** Ln $(I_\mathrm{R}) - V_\mathrm{R}$ and Ln $(I_\mathrm{R}) - \sqrt{V_\mathrm{R}}$ of MS and MPS diodes

layer, respectively. The slopes of region II of the MS diode and region III of the MPS diode are close to 2, which is explained by space charge-limited current (SCLC) mechanism. The slope of region II of the MPS diode is greater than 2 and can be described by the trap-charge limited current (TCLC) mechanism with an exponential distribution of traps. When the PVP: Sn-TeO_2 interfacial layer is placed in the metal–semiconductor interface, a series of energy states/traps is created due to the interfacial layer. This phenomenon takes place within the semiconductor energy gap below the Fermi level, which changes the conductivity mechanism by storing and releasing electrons. The results of the $\mathrm{Ln}I_\mathrm{F} - \mathrm{Ln}V_\mathrm{F}$ plot specify that at very low applied voltages, the density of the injected carriers is much lower than that of the thermal-generated free charge carriers, and the current increases linearly with voltage (region I). At intermediate voltages, as voltage increases, the injected charges increase and begin to fill the traps, leading to increasing the current exponentially (region II). At higher voltages, the increasing in voltage causes an approach to the trap-filled limit state, and accordingly, an increase in the series resistance and a reduction in the slope of the plot. In this state, space charge-limited current mechanism dominates. The presence of the interfacial layer at the metal–semiconductor interface has induced arising the current of the MPS diode with voltage exponentially in the intermediate voltage region, which is owing to the surface states/traps. Nevertheless, this is not observed for the MS diodes [3, 7, 27].

Two Poole–Frenkel emissions (PFE) and Schottky emission (SE) theories are usually used to study the mechanism governing the current in reverse bias. To do this, the Ln $(I_\mathrm{R}) - V_\mathrm{R}$ and Ln $(I_\mathrm{R}) - \sqrt{V}$ plots are drawn with I–V information and shown in Fig. 4b.

Both mechanisms governing PFE and SE currents are described as follows [28, 29]:

$$I_\mathrm{R} = I_0 \exp\left(\frac{\sqrt{V}\beta_\mathrm{PF}}{\sqrt{d}kT}\right) \tag{5a}$$

$$I_\mathrm{R} = AA^*T^2 \exp\left(\frac{\sqrt{V}\beta_\mathrm{S}}{\sqrt{d}kT}\right) \tag{5b}$$

where β_PF and β_S are the Poole–Frenkel and Schottky field-lowering coefficients, respectively. According to Eq. (5), field-lowering coefficients can be calculated by the slope of the Ln $(I_\mathrm{R}) - \sqrt{V_\mathrm{R}}$ plot. β_PF is twice β_S and their theoretical value is expressed as follows:

$$2\beta_\mathrm{S} = \beta_\mathrm{PF} = \left(\frac{q^3}{\pi\varepsilon}\right)^{1/2} \tag{6}$$

where ε is the permittivity of the interfacial layer. The theoretical values of β_PF and β_S for the MS diode are 4.2×10^{-5} and 2.1×10^{-5} eV $\mathrm{m}^{1/2}$ $\mathrm{V}^{-1/2}$, respectively, while those for the MPS diode are 1.2×10^{-5} and 6.0×10^{-6} eV

$m^{1/2}\ V^{-1/2}$. Also, the value of the field-lowering coefficient is calculated through the slope of the plot in Fig. (4b), which is 6.0×10^{-6} and 1.5×10^{-5} eV $m^{1/2}\ V^{-1/2}$ for MS and MPS diodes, respectively. A comparison of the obtained results shows that the obtained experimental field-lowering coefficients for MS is close to the theoretical Schottky-emission (SE) coefficient (β_{SE}) and for MPS is close to the theoretical Poole–Frenkel emission (FPE) coefficient (β_{PFE}). Therefore, the reverse leakage current in the MS structure is dominated by the SE mechanism, and in MPS structure is dominated by the PFE mechanism. In SE, the carrier transport occurs from the contact interface instead of the bulk material due to the nonuniformity structure of the interlayer. While in FPE, the carrier transport is formed from the metal into conductive dislocations via trap or states [28, 30].

Another parameter affecting the efficiency of Schottky diodes is the rectification ratio (RR), which is defined as $RR = I_F/I_R$. The rectification ratios of MS and MPS diodes for 4.5 V are estimated 4.56 and 320, respectively. A significant increase in the rectification ratio of the MPS diode, compared to the MS diode, is due to the presence of an interfacial layer, which can lead to a growth in direct current or a drop in reverse current. This increase is very important in the rectification of electronic components, especially Schottky junctions. To determine why the value of R is raised, the resistance parameter can be used, which is defined by Ohm's law ($R_i = V_i/I_i$). The constant value of resistance at high direct bias voltages is called series resistance (R_s) and at high reverse bias, voltages are called shunt resistance (R_{sh}). The voltage dependence plots ($R_i - V$) of both diodes are shown in Fig. 5. The series resistance and shunt resistance values of the MS diode are calculated 3.14 kΩ and 14.3 kΩ, respectively, and for MPS diodes, they are estimated 450 Ω and 144 kΩ. The results exhibit that the interfacial layer reduces the series resistance and increases the shunt resistance, and as a result, both increased direct current and reduced reverse current significantly uplift the rectification ratio of the MPS diode, compared to that of MS one.

In the following, the values of barrier height, ideality factor, and series resistance are calculated using Cheung's method and compared to the results obtained from the thermionic emission theory. According to this method, Eq. (3) can be rewritten as follows:

$$\frac{dV}{dLn(I)} = RI + \frac{nkT}{q} \tag{7}$$

In the curvature of the I–V curve, the $dV/dLn(I)$ plot is linear concerning I in the direct bias region, where the values of series resistance and the ideality factor can be calculated through its slope and intercept. The barrier height can also be estimated from the dependence of the

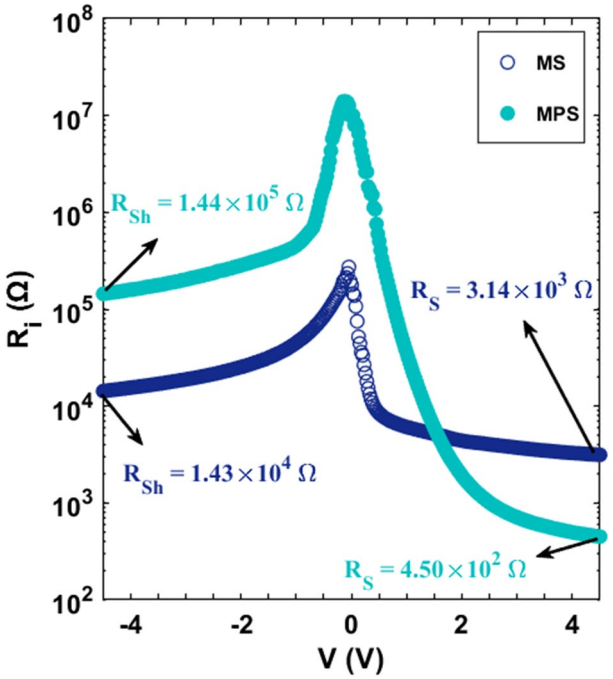

Fig. 5 The semilogarithmic plot of Ri – Vi for the MS and MPS diodes

Cheung's function on the current. The Change's function is defined according to the following equation [5]:

$$H(I) = V - \frac{n}{\beta}Ln\left(\frac{I}{AA^*T^2}\right) = RI + n\Phi_B \tag{8}$$

Based on Eq. (8), the values of series resistance and the barrier height can be calculated from the slope and intercept of the linear part of the $H(I) - I$ plot. The $dV/d(LnI) - I$ and $H(I) - I$ plots of both diodes are shown in Fig. 6.

To calculate the barrier height, it is necessary to determine the value of the ideality factor, which is obtained by Eq. (4). Using Eqs. (7) and (8), the values of R_s, n, and Φ_B are estimated 3.38 KΩ, 5.58, 0.62 eV for MS diodes, and 241 Ω, 5.74, 0.75 eV for MPS diodes, respectively. The results of this method also indicate that the (PVP: Sn-TeO_2) interfacial layer reduces the series resistance and the ideality factor and increases the barrier height, and consequently, improves the efficiency of the metal–semiconductor diode. The main parameters obtained from both methods are presented in Table 1.

All these experimental results show that the use of (PVP: Sn-TeO_2 interlayer between Al and p-Si leads to an increase of Φ_0, and the decrease of n and R_s. The value of RR for the MPS diode was also found significantly higher than the MS diode. In recent years, similar results have been reported by various studies [31–40].

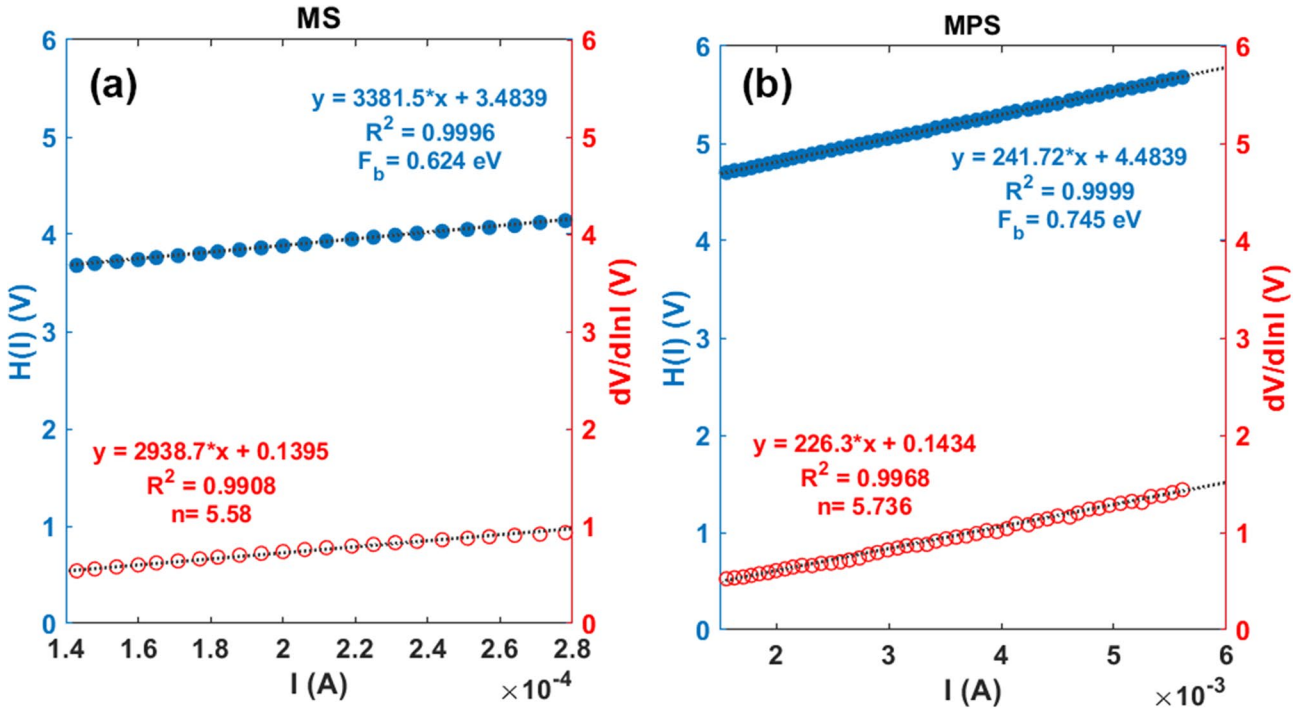

Fig. 6 The plots of dV/d Ln(I) − I and $H(I)$ − I for: **a** MS and **b** MPS diodes

Table 1 Electrical parameters extracted from the different methods for MS and MPS diodes

Sample	n		RR	R_s (kΩ)			R_{sh} (kΩ)	Φ_B (eV)	
	TE	dV/dLn(I)		TE	dV/d Ln(I)	$H(I)$	TE	TE	$H(I)$
(MS)	3.58	5.58	4.56	3.13	2.94	3.38	14.3	0.63	0.62
(MPS)	2.97	5.72	320	0.45	0.23	0.24	144	0.77	0.75

4 Conclusions

In the present study, the Al/(PVP: Sn-TeO_2)/p-Si and Al/p-Si diodes were made using a spin coating method, and the effect of the interfacial layer on its electrical characteristics was investigated. The average sizes of TeO_2 [related to (110) and (212) crystal plates] and SnTe nanoparticles were estimated at 31 nm and 41 nm. The EDS analysis shows that the nanostructures contain only Te and Sn elements. The energy bandgap of the prepared (Sn-TeO_2) nanostructure was found as 4.65 eV from the $(\alpha h\upsilon)^2$ vs ($h\upsilon$) plot. Electrical parameters of the fabricated Al/p-Si diodes with and without (PVP: Sn-TeO_2) interlayer were extracted both the standard TE theory and Cheung functions using I–V measurements in the voltage range of ± 4.5 V at room temperature. The CTMs of them were also examined both the forward bias $\mathrm{LnI_F}$-$\mathrm{LnV_F}$ and reverse $\mathrm{Ln}I_R - {V_R}^{0.5}$ plots. $\mathrm{Ln}I_F - \mathrm{Ln}V_F$ plot shows that the dependence of the current on the voltage has as an exponential relation: $I \sim V^m$, where m is related to the slope of each region. Both the experimental and theoretical value β was calculated from the $\mathrm{Ln}I_R - {V_R}^{0.5}$ plot and the results show that the CTM is governed by the SE emission and PFE emission for MS and MPS diodes, respectively. All these experimental results indicated that the existence of the (PVP: Sn-TeO_2 interlayer leads to an increase of Φ_0, RR, and the decrease of n, R_s. The observed discrepancies in the main electrical parameters obtained from TE theory and Cheung functions can be attributed to the nature of the calculation method and also voltage-dependent of them.

Acknowledgements This study was supported by Gazi University Scientific Research Project. (Project Number: GU-BAP.05/2019-26).

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