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Impact of trap charge and temperature on DC and Analog/RF performances of hetero structure overlapped PNPN tunnel FET

Karabi Baruah[1] · Rajashree Das[1] · Srimanta Baishya[1]

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Abstract
Impact of interface trap charges (ITCs) as well as temperature on the performance of a proposed dual dielectric constant spacer source/drain, overlapped double gate tunnel FET with a source pocket was investigated using two-dimensional Technology Computer-Aided Design (TCAD) device simulator. The proposed device is Si-based with Germanium as the source material, SiGe as a pocket material, and has a high-k gate dielectric. Its performance in terms of DC and analog/RF parameters vis-à-vis a conventional double gate PNPN TFET was compared. The device shows better results than the conventional one with an ON current of 1.71×10^{-3} A/μm, ON–OFF current ratio 10^{11}, and subthreshold swing of 45 mV/decade. The study was focused on the analysis of the electric field, transfer characteristics, transconductance (g_m), output conductance (g_d), parasitic capacitances, gain-bandwidth product (GBP), cut off frequency (f_T) for both the damaged (presence of donor/acceptor interface trap charges) and undamaged (no trap) conditions. The study revealed that the proposed structure is more immune to the interfacial trap charges as compared to the conventional device. Apart from this, the analysis shows a degradation of subthreshold swing (SS) and OFF current (I_{OFF}) at elevated temperatures.

Keywords Band to band tunneling (BTBT) · Cut off frequency (f_T) · Dual-k spacer · DG-TFET · Gain-bandwidth product (GBP) · Source and drain overlap · Temperature sensitivity (s_T) · Tunnel field-effect transistor (TFET)

1 Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have played a vital role in the exponential growth of the microelectronics industry. However, aggressive downscaling of the same gives rise to several serious issues such as high leakage current, high subthreshold swing, and other short channel effects which degrade the device performance for low power applications [1, 2]. These challenges enforce the researchers to look for new devices whose operation mechanism may be different from that of MOSFET i.e. the thermionic emission. In this regard, Tunnel FET can be considered as a fit candidate for low power applications in advanced technology node. It can overcome the fundamental limit of subthreshold swing (60 mV/decade) of conventional MOSFET using interband tunneling at the source-channel junction [3, 4]. In the case of n-channel TFET, the source is p-type and tunneling of electrons occurs from the valence band of the source to the conduction band of the channel. This interband tunneling mechanism allows TFET to exhibit low subthreshold swing and low leakage current [5, 6]. However, TFET has many disadvantages such as low ON current, inherent ambipolar conduction, high threshold voltage and high gate-drain capacitance. Many innovative techniques have been used to resolve these issues. Some of such salient techniques are gate work function engineering [7, 8], high dielectric constant engineering [9, 10], spacer material [11], overlapping of source/drain region [12, 13], bandgap engineering [14, 15], hetero dielectric [9, 16], pocket doping [17–19], gate engineered dopingless TFET [20, 21], etc. Among these engineering architectures, the heavily doped source pocket PNPN TFET offers higher on current with lower SS as well as improved reliability [22]. Spacer engineering can also enhance the performance of TFET [11, 23]. Double gate tunnel FET provides better electrostatic control and helps to overcome the limitations of threshold voltage, subthreshold swing (SS), and ON-current limitation of a single gate TFET [24]. Moreover, reliability is a major

✉ Karabi Baruah
karabibaruah26@gmail.com

[1] Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar, Assam, India

concern for any Nanoscale device as Semiconductor materials are extensively used in various applications, like sensor materials [25–28]. In this regard, the interface trap charges (ITCs) are one of the reasons for performance degradation or unreliable performance. Material defects near the tunnel junction induce parasitic conduction through trap-assisted tunneling (TAT) which is responsible for SS degradation [29, 30]. Rigorous investigation shows the interface quality/traps are the major sources of instability [30–36]. Interface trap charges are generally induced during fabrication processes by stress-induced and process-induced damages [33]. In TFET, the traps mainly appear due to high electric field at the tunneling junction. Furthermore, the trap charges that exist on the surface of the substrate change the electric field at the tunneling junction, which further alters the tunneling current and hence the device performance. Based on the polarity of a trap, it can be categorized into two types namely, the donor (positive) and acceptor (negative) traps. The donor trap in an empty state can work as a positive trap or it can work as a neutral charge when occupied by an electron. On the other hand, the acceptor trap is known as a neutral charge in an empty state and it works as a negative charge when occupied by an electron.

As the packing density is increasing day by day, heat dissipation also increases significantly. Hence the transistors nowadays have to operate at a higher temperature than usual. Therefore, it is obligatory to analyze the device performance at higher temperatures. A few works have been reported to understand the temperature dependence of transfer characteristics of various field-effect transistors [37, 38]. In [38], it is reported that the temperature dependence of III-V TFET is a strong function of gate voltage, due to which the transfer characteristic is partitioned in terms of gate bias. The Leakage current is determined by SRH generation recombination current at low gate bias. When the gate bias is increased to a higher value, it excites carriers from the trap center to the conduction band. However, at higher gate bias, the BTBT mechanism dominates with the negligible presence of trap centers due to narrow barrier width at high gate voltage. The final partition of the characteristics is based on carrier transport by diffusion.

In this work, we re-investigated the effect of trap charges and temperature on DC, analog, and RF parameters of a proposed overlapped DG-PNPN-TFET, which overcomes the effect of interfacial trap charges even over a wider range of temperature (250 K–400 K) than the conventional TFET.

2 Device design and simulation parameters

Figure 1a shows the cross-sectional view of the proposed device (overlapped-DG-PNPN-Heterostructure-TFET). The design parameters of conventional PNPN TFET and proposed structure used in the simulation process are listed in Table 1. For this work, the Si body thickness used is 10 nm and HfO_2 is used as a gate dielectric with a thickness of 2 nm. Accordingly, the equivalent oxide thickness (EOT) of the gate oxide is 0.37 nm for the proposed device. The EOT is the thickness of SiO_2 gate oxide needed to obtain the same gate capacitance as that obtained with thicker

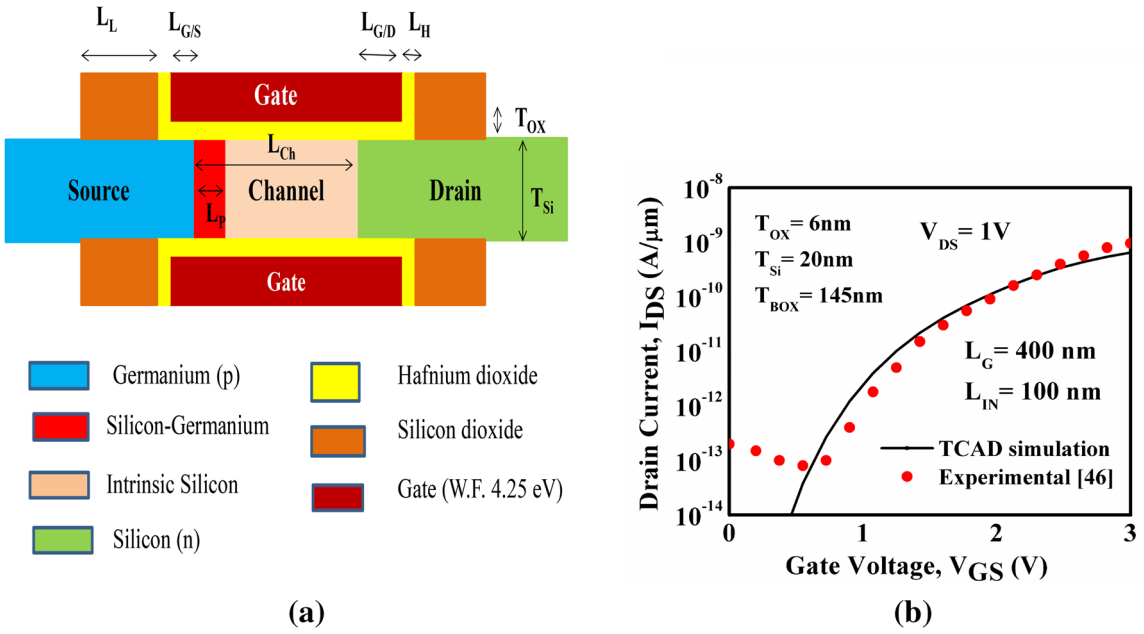

Fig. 1 **a** Cross sectional view of proposed PNPN-TFET, **b** Calibration of TCAD models with experimental data [46]

Table 1 Device design parameter used for simulation

Parameters	Conventional PNPN TFET	Proposed TFET
Channel length (L_{Ch})	22 nm	22 nm
Gate oxide thickness (T_{OX})	2 nm	2 nm (EOT = 0.37 nm)
Silicon thickness (T_{Si})	10 nm	10 nm
Source doping (N_S)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Channel Doping (N_{Ch})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Drain doping (N_D)	1×10^{18} cm^{-3}	1×10^{18} cm^{-3}
Pocket doping (N_P)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
Pocket length (L_P)	2 nm	2 nm
Gate work function (WF)	4.25 eV	4.25 eV
Trap density (N_f)	1×10^{13} cm^{-2} eV^{-1}	1×10^{13} cm^{-2} eV^{-1}
Mole fraction of SiGe (M.F.)	0.3	0.3
Gate-source overlapped ($L_{G/S}$)	–	4 nm
gate-drain overlapped ($L_{G/D}$)	–	4 nm
High k spacer (HfO2) length (L_H)	–	2 nm
Low k spacer (SiO2) length (L_L)	–	10 nm

high k dielectric (HfO_2). Germanium (bandgap 0.66 eV at room temperature) is used as source material to boost the ON current due to its narrower bandgap. Both the structures have the same doping profiles. A higher source doping (1×10^{20} cm^{-3}) as compared to drain doping (1×10^{18} cm^{-3}) is used to suppress the ambipolar conduction [39] which is a built-in property of tunnel FET. A highly doped n-pocket of SiGe (mole fraction 0.3) is introduced in the source side to reduce the tunneling width and to increase the lateral electric field thereby minimizing the SS and potential drop at the tunneling junction [22]. Gate-to-source as well as gate-to-drain overlap promise good electrostatic control on the channel, resulting in better ON-state current. This arrangement, of course, increases the miller capacitance which degrades the device performance [40]. However, overlapping some parts of the drain by gate helps in suppressing the ambipolar conduction [12]. Due to the overlapping of the gate on the source side, the tunneling area and hence the tunneling current increases [40]. The use of the spacer is to modulate the fringing field arises from the gate to source and to drain. This helps in shifting the maximum electric field and energy band profile in the channel, resulting in a modified tunneling current [23, 41]. Moreover, an optimum value (4.25 eV) of gate metal work function was used to obtain improved characteristics.

The conventional and proposed TFET were simulated using the SENTAURUS TCAD device simulator [42]. Various models used are non-local BTBT for tunneling of carriers from one energy band to another specified energy band, bandgap narrowing to take care of the high doping effects in the heavily doped regions, concentration and field-dependent mobility, SRH for carrier recombination, and Fermi Dirac statistics. The estimated value of interface trap charge density was chosen from various experimental works within the range of 10^{11}–10^{13} cm^{-2} eV^{-1} [43–45]. The trap energy levels used is 0.035 eV for both the types of traps. Uniform distribution of ITCs was considered at the Si-HfO2 as well as SiGe-Si interfaces for the proposed device and Si-SiO2 and SiGe-Si interfaces for the conventional TFET. The traps that may present in the Ge-HfO2 interface and Ge-SiGe interface were ignored. Thus, we have considered a trap density of 10^{13} cm^{-2} eV^{-1} for both the acceptor as well as donor traps. The TCAD simulator was calibrated with the experimental results [46] as shown in Fig. 1b.

3 Result and discussion

The energy profiles of conventional and proposed PNPN TFET in the OFF state and ON states for no trap condition are shown in Fig. 2a and b, respectively. The measurement was made along with a horizontal cutline 2 nm below the Si-HfO_2 interface. At $V_{GS} = 0$ V, the tunneling.

probability from the valance band of the source to the conduction band of the channel is almost negligible because of the wider tunneling barrier width present at the source-channel junction for both the conventional and proposed devices. However, in the ON state ($V_{GS} = 2$ V), the gate voltage pulls down the conduction band of the channel well below the valance band of the source. As such, electrons can easily tunnel from the source to channel thus recoding a band-to-band tunneling current. SiGe is used as pocket material for both the devices as it has fewer material defects and its bandgap can be adjusted by varying the mole fraction. The mole fraction considered is 0.3 for all the cases [47]. Due to the presence of lower energy gap material (Ge), there is more band bending at the source region of the proposed device, resulting in higher electron tunneling. Due to

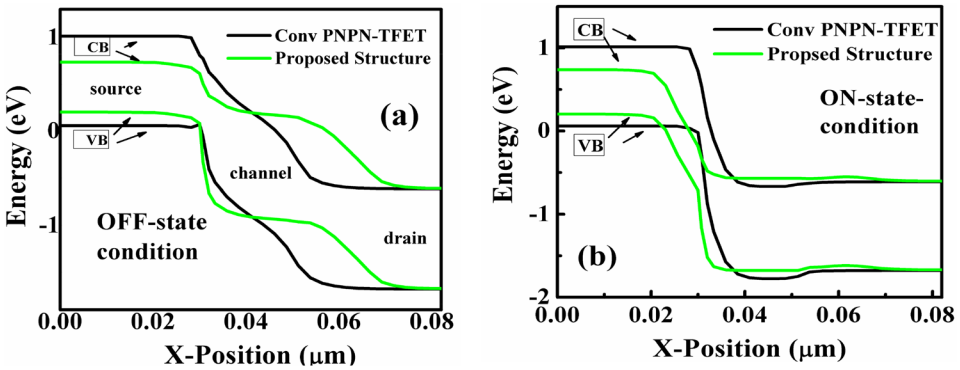

Fig. 2 Energy band diagram of conventional PNPN TFET and proposed structure in **a** OFF-state and **b** ON-state condition

gate overlapping on the source, the tunneling area and hence, current increases. Undesirable ambipolar conduction can be minimized by overlapping some portion of the gate over the drain as well. Another cause of the low energy barrier in the proposed device is the high k dielectric (HfO_2) material used as the gate dielectric.

Figure 3a shows the impact of different ITCs on BTB generation of electrons for the proposed devices along the X-axis. The generation rate is of the order of 10^{32} cm^{-3} s^{-1}, which is higher than the conventional one (of the order of 10^{29} cm^{-3} s^{-1}, not shown in the Figure). The graph shows almost a constant behavior for different types of the trap in case of the proposed structure. The onset of BTB generation in Fig. 3a can be compared with the energy band diagram in Fig. 2b.

Figure 3b shows the electric field variation with different traps along the X-axis. The side spacer modulates the fringing field arising from the gate, resulting in a shift of maximum electric field to the right of the tunneling junction. Due to overlap of the gate over the source the high electric field impact area increases, hence the tunneling area and ON current. From the graph, it can be visualized that there is not much variation of electric field profile with different trap charges, but a slightly higher electric field is observed for a positive trap which results in the change of tunneling current.

The concentration of electrons and holes from source to drain of the proposed device is shown in Fig. 3c. From the graph, it can be seen that electron concentration starts increasing from a point of 20 nm and reached the order of 10^{20} cm^{-3} (equivalent to the p^+ source region) in the channel region. This is due to the tunneling of electrons from the valance band of the source to the conduction band of the channel due to the gate voltage. The hole concentration starts decreasing from the same point where the electron concentration starts increasing as the tunneling mechanism starts to occur.

Figure 4a shows the comparative transfer characteristics of conventional PNPN TFET and the proposed-overlapped-hetero-structure-PNPN TFET for gate voltage ranging from − 0.5 to 1.5 V, with a constant drain voltage (0.7 V). It is clear from the figure that the conventional PNPN TFET shows low ON current and OFF current as compared to the proposed one. The high ON current (mA range) and steeper SS are achieved in the proposed model due to the use of low band-gap material (Ge) as a source and gate on source overlapped. However, due to the high k gate dielectric material, the leakage current degrades. But, a higher I_{ON}/I_{OFF} ratio is

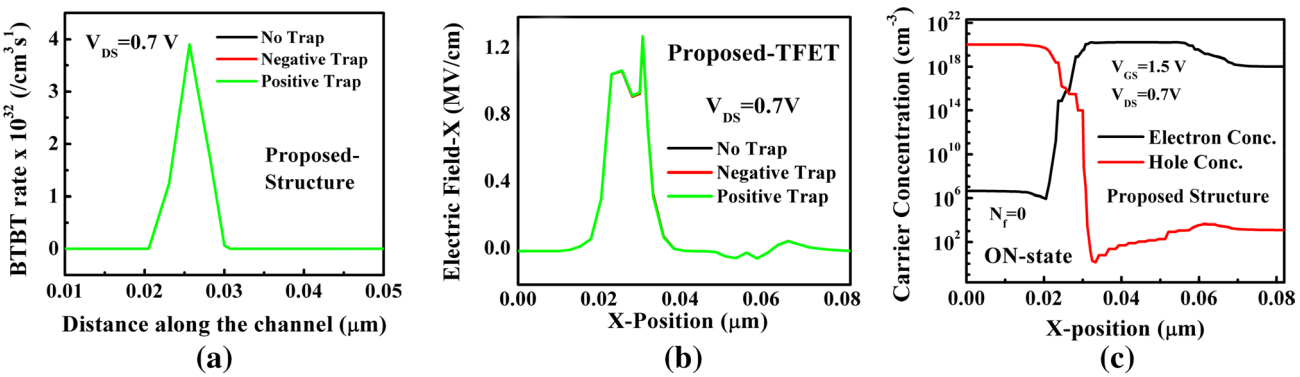

Fig. 3 **a** Impact of trap on BTBT rate of proposed device, **b** Variation of Electric field of proposed TFET with different ITCs along X position, and **c** Carrier concentration of proposed structure along X-position, respectively

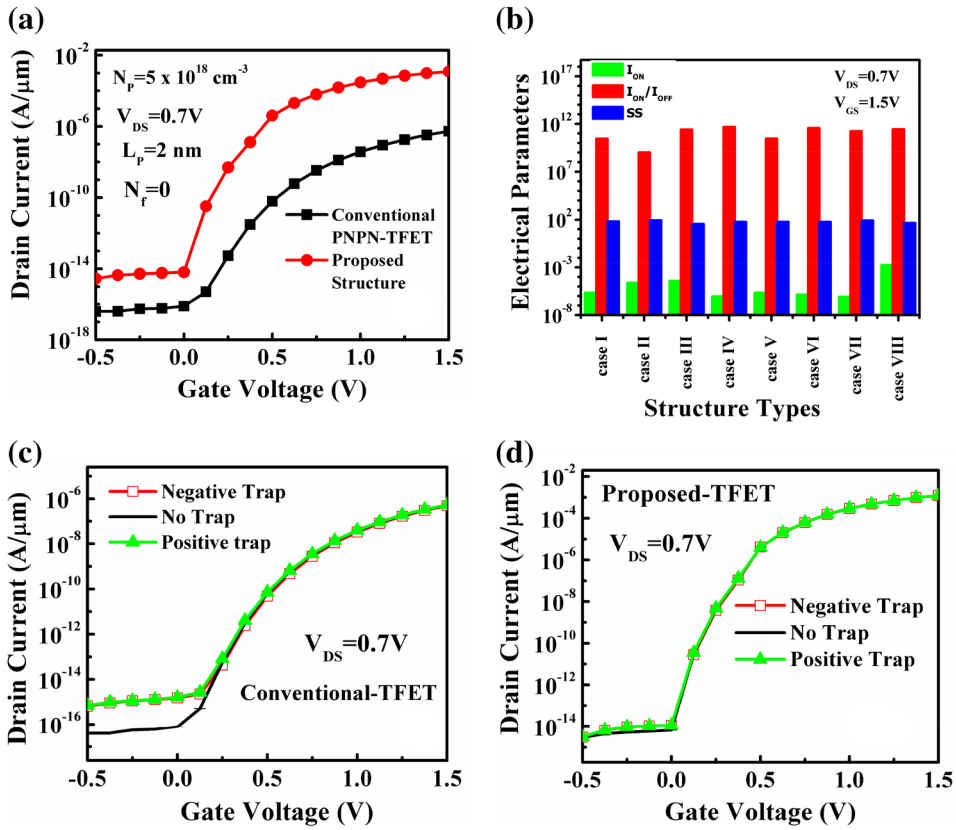

Fig. 4 **a** Comparison of transfer characteristics (I_D-V_G) of conventional and proposed structure, with V_{GS} ranging from − 0.5 to 2 V and V_{DS} = 0.7 V **b** comparison of electrical parameters (I_{ON}, I_{ON}/I_{OFF}, SS) of among various structure with V_{GS} ranging from − 0.5 to 1.5 V and V_{DS} = 0.7 V **c** impact of ITCs on I_D-V_{GS} characteristics of conventional device, and **d** impact of ITCs on I_D-V_{GS} characteristics of proposed device

achieved. Comparative plots of some of the important electrical characteristics of various such structures are shown in Fig. 4b. The parameters values used for this analysis are listed in Table 1, while the characteristics parameters such as I_{ON}, $I_{ON}/I_{OFF,}$ and SS are listed in Table 2. The comparison shows a better performance of proposed TFET in terms of ON current, ON–OFF current ratio, and SS.

Figure 4c and d show the impact of different types of traps on I_D-V_{GS} characteristics of the conventional and proposed devices, respectively, V_{DS} = 0.7 V. The trap density considered is 10^{13} cm^{-3} s^{-1}. For conventional structure, the off current degrades about one decade when positive or negative traps at the interfaces are introduced. But the effect of the interface trap charge is very less in case of the proposed structure. There is almost negligible variation in ON current with different traps for both the structures. But a significant variation in the OFF current is observed in the convention TFET due to the non-overlapped structure and low k gate dielectric material. Thus the I_{ON}/I_{OFF} ratio degrades from an order of 10^{11} to 10^{9} with donor and acceptor trap charge densities in the conventional device. However, as a consequence of immunity against the traps, the I_{ON}/I_{OFF} ratio remains unaltered in the proposed structure.

Table 2 Comparison of device electric characteristics of various structure at V_{GS} = 1.5 V and V_{DS} = 0.7 V

Sl. No	Type of structures	I_{ON} (A/μm)	I_{ON}/I_{OFF}	Avg. SS (mV/dec)
Case I	Conv.-PNPN-DGTFET	2.18×10^{-6}	2.8×10^{10}	109
Case II	Conv. With Ge source	2.35×10^{-5}	1.0×10^{9}	98
Case III	Conv. With HfO_2 gate dielectric	3.71×10^{-5}	2.4×10^{11}	61
Case IV	Conv. With gate-source overlap	8.78×10^{-7}	4.7×10^{11}	66
Case V	Conv. With gate-drain overlap	2.19×10^{-6}	2.9×10^{10}	73
Case VI	Conv. With single spacer	1.35×10^{-6}	3.6×10^{11}	68
Case VII	Conv. With dual spacer	8.29×10^{-7}	1.7×10^{11}	67
Case VIII	Proposed-PNPN-DGTFET	**1.72×10^{-3}**	2.6×10^{11}	**45**

Bold value indicates improved performance of proposed structure

Figure 5a and b show the I_D-V_{DS} characteristics of conventional and proposed TFET for a given gate voltage (2 V). These plots reveal that the deviation of output characteristics, as a function of various types of traps is very insignificant in the case of the proposed device. In other words, the proposed structure is more reliable than the conventional one.

To show the trap dependency of both the conventional and proposed devices in terms of trap energy, we analyzed the transfer characteristics and output characteristics in Figs. 4c, d, and 5a, b, respectively, for both the donor and acceptor type of trap charges with an energy level of 0.035 eV. The specific trap energy level was used from the SENTAURUS TCAD manual [43]. From Fig. 4c and d, it can be seen that there is an almost negligible variation of ON and OFF currents for both types of trap charges at 0.035 eV energy level. However, the highest I_{ON} and lowest I_{OFF} are achieved when trap dependency is considered without trap energy level, i.e. no trap condition.

The transconductance (g_m) is an important parameter for analog performance. It mainly depends on the value of the drain current. It should be high enough to have a high cutoff frequency. We observed a transconductance in the range of 10^{-3}, which is 1000 times higher than the conventional one. Figure 6a and b illustrate the effect of trap charge on transconductance characteristics as a function of

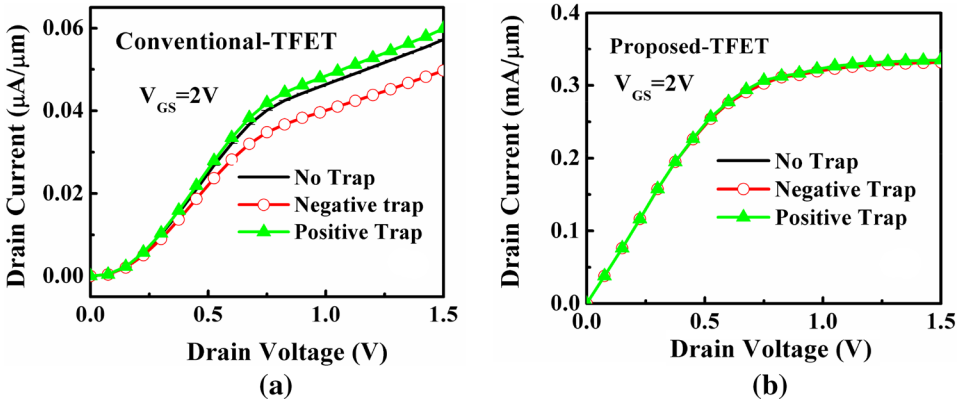

Fig. 5 Variation of Output characteristics (I_D-V_D) with different ITCs for **a** conventional PNPN TFET, and **b** proposed PNPN TFET

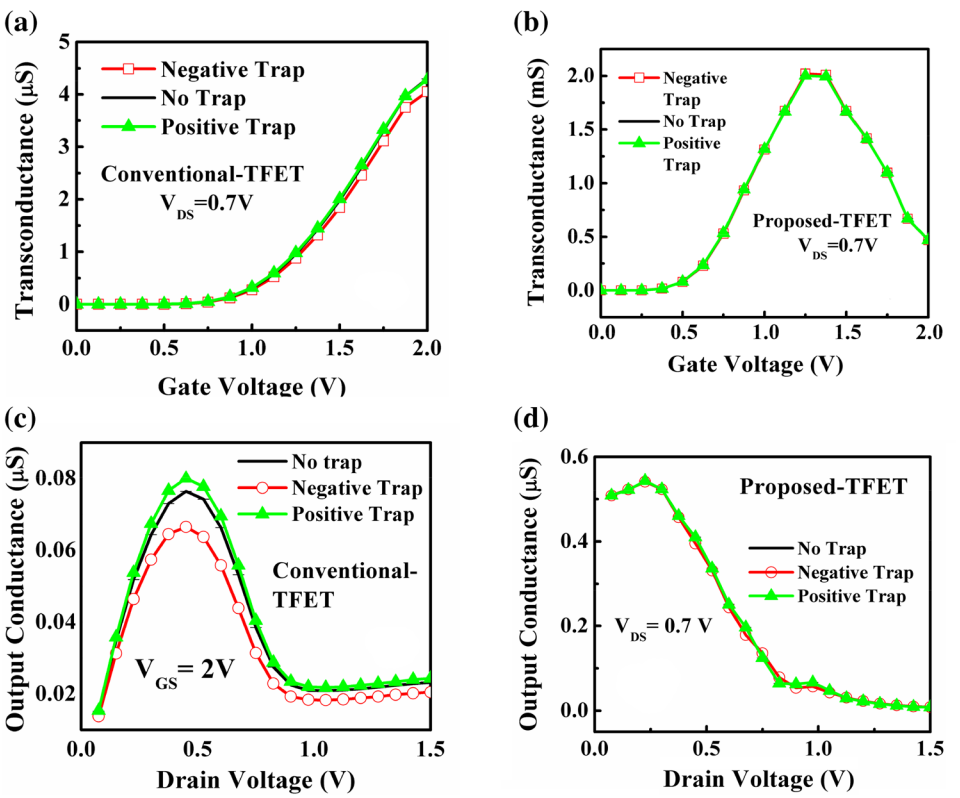

Fig. 6 Impact of ITCs on transconductance of **a** conventional TFET **b** proposed TFET. Impact of ITCs on output conductance of **c** conventional TFET **d** proposed TFET

gate voltage at $V_D = 0.7$ V. g_m increases for positive trap charge and decreases for negative trap charge in heterogenous gate dielectric GAA TFET [33]. But the figures show that in conventional double gate PNPN TFET, g_m is almost unaffected by the positive trap charge, even though it loses immunity with negative trap charges. The impact of ITCs on transconductance of the proposed structure is almost negligible compared to the conventional one.

Output conductance (g_d) is also a crucial parameter for analog performance. Figure 6c and d show the output conductance variation with drain bias for the conventional and proposed structure, respectively, with various traps. From the figure, it can be noticed that it is maximum at the linear reason and minimum at the saturation region. The rate at which the current changes with the voltage is very less in the saturation region due to the saturated nature of the current which leads to lower g_d. Figure 6c shows that g_d increases for positive trap and decreases due to the negative trap. But, this characteristic suffers little from different interface traps in the case of the proposed device. As seen in Fig. 5b, the output conductance is equivalent to the first-order differentiation of drain current with respect to drain voltage (V_D) for a given gate voltage. Since this output characteristic suffers little from the presence of traps due to the use of gate overlap and low bandgap material in the source, the output conductance behaves similarly in contrast to the conventional one.

The operating speed of a TFET largely relies on the behavior of capacitance. Thus, it is necessary to investigate the device capacitances as well as the impact of ITC on them. Figure 7a–d show the variation of the capacitances C_{gd} and C_{gg} with respect to gate bias for various trap charges at a frequency of 1 MHz and $V_{DS} = 0.7$ V. Since the inversion charge distribution of TFET is different from MOSFET, C_{gd} contributes more to the total gate capacitance (C_{gg}) than C_{gs} [48, 49]. From the plots, it can be seen that C_{gd} increases with gate voltage due to better coupling between the gate and drain, resulting in an increase of the inversion layer from the drain side to the source side with an increase in gate bias [49]. At higher gate voltage the total gate capacitance is dominated by C_{gd}. As we can observe from the figure, the impact of ITCs is negligible in the case of the proposed device in contrast to the conventional one.

Another important RF parameter is the cut-off frequency (f_T). It has a direct variation with g_m and inverse variation with total gate capacitance $C_{gg} = C_{gs} + C_{gd}$, and is given by [50, 51]:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{\left(1 + 2\frac{C_{gd}}{C_{gs}}\right)}} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{1}$$

The impact of ITCs on the cutoff frequency for both conventional and proposed structures is shown in Fig. 8a and b, respectively. In the conventional structure, it decreases in the presence of negative trap charges, while its impact is negligibly small for positive traps. The variation of f_T follows almost the same pattern as that of g_m with gate voltage. On the other hand, the proposed PNPN structure has better immunity for all types of traps.

The other important parameter for RF applications is the gain-bandwidth product (GBP), given by [52]:

$$GBP = \frac{g_m}{2\pi 10 C_{gd}} \tag{2}$$

Figure 8c and d represent this crucial parameter (GBP), with various trap charges for $V_{DS} = 0.7$ V and frequency 1 MHz. Figure 8c shows the difference of GBP with gate voltage for negative traps in the case of conventional structure. On the other hand, the proposed structure exhibit almost negligible variation of GBP with different trap types

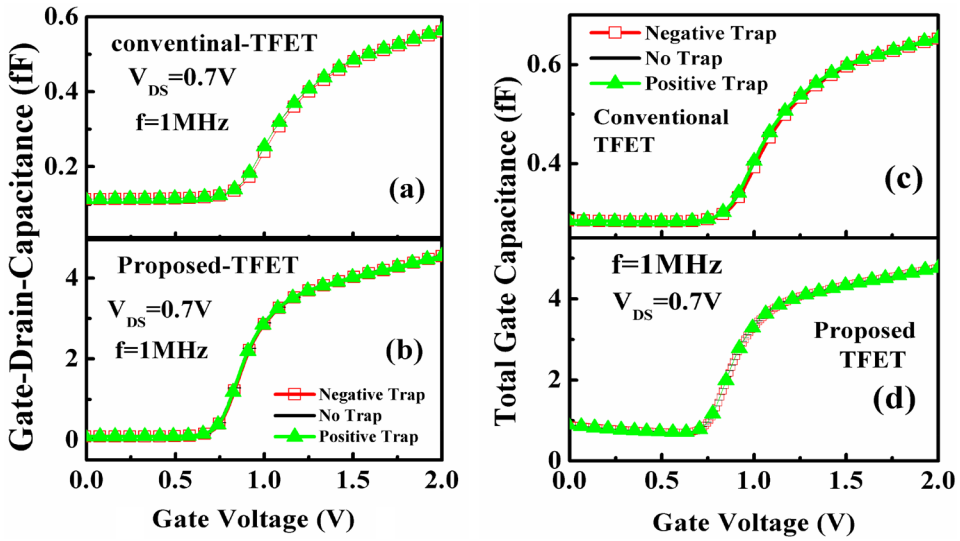

Fig. 7 Variation of parasitic capacitance as a function of gate bias with different ITCs **a–b** C_{GD} for conventional and proposed, and **c-d** C_{GG} for conventional and proposed respectively

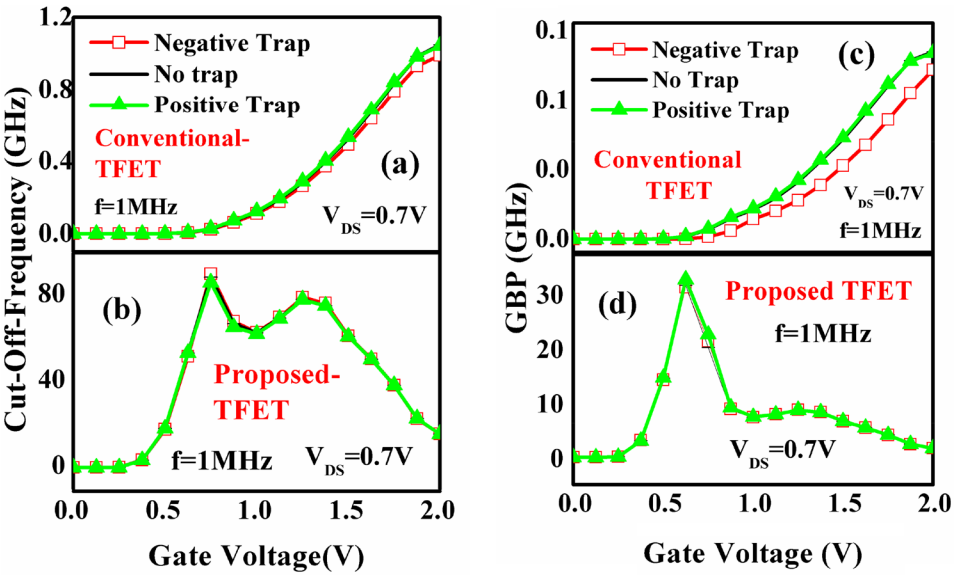

Fig. 8 Impact of ITCs on cut off frequency of **a** conventional and **b** proposed as a function of gate voltage. Gain-bandwidth product as a function of gate voltage at different traps for **c** conventional and **d** proposed TFET

as shown in Fig. 8d. It is clear from the figure that the GBP of the proposed PNPN TFET is higher than the conventional one.

The little variation of I-V characteristics and the analog properties with different trap charges ensures the reliability of the proposed device. The I-V characteristic shows little variation with different traps due to the use of high k material as the gate oxide in the proposed device. Very negligible variation is observed in the case of analog properties of the proposed structure. Both conventional and proposed structure shows a little variation of capacitance (C_{gd}, $C_{gs,}$ and C_{gg}) w.r.t. gate voltage for different traps due to the use of n^+ pocket between source and channel. However, the value is higher in the case of the proposed structure than its counterpart.

3.1 Temperature analysis

In this section, we have analyzed the characteristics of the proposed structure at various ambipolar temperatures (250–400 K) considering one type of trap at a time to understand its behavior with the temperature variation. The trap density and the trapped energy level considered are the same as in the previous section, that is, 10^{13} cm^{-2} eV^{-1} and 0.035 eV, respectively. Figure 9 shows the variation of band-to-band tunneling rate with varying temperature for the positive trap, negative trap, and no trap conditions at $V_{DS} = 0.7$ V and $V_{GS} = 2$ V. It is seen that the BTBT is weakly dependent on temperature and slightly increases with increase in temperature; but remains unaffected by traps, irrespective of its type. This is because the bandgap of a semiconductor decreases with an increase in temperature. However, SRH recombination dominates at the low electric field and has a strong dependence on temperature. Hence the characteristics

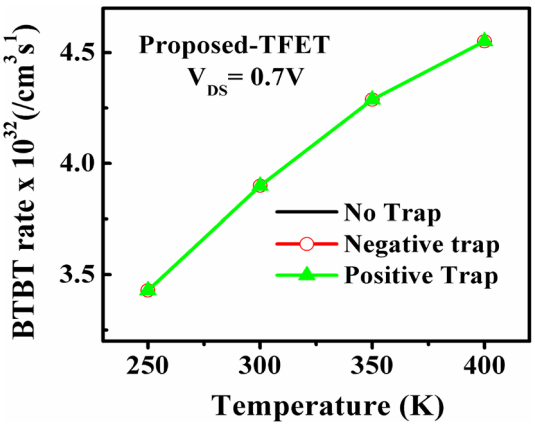

Fig. 9 Variation of BTBT rate of proposed structure as a function of temperature at different interface trap charges

curve shows a large variation in the subthreshold regime with different temperatures.

Figure 10a–c illustrate the influence of temperature on the transfer characteristic of the proposed device in the presence of negative traps, no trap, and positive traps, respectively. The temperature dependence of transfer characteristics is a strong function of applied gate voltage due to different conduction mechanisms in OFF-state and ON-state [38]. Lower gate voltage sets the leakage current (I_{OFF}). I_{OFF} increases with increase in temperature and are determined by Shockley–Read–Hall recombination current. In the subthreshold region, drain current increases exponentially and the average SS starts degrading with temperature. However, with the increase in V_{GS}, BTBT current dominates and, therefore, the temperature sensitivity of drain current becomes weak. At higher V_{GS}, the BTBT generated carriers near the source start diffusing towards the drain [38]. The

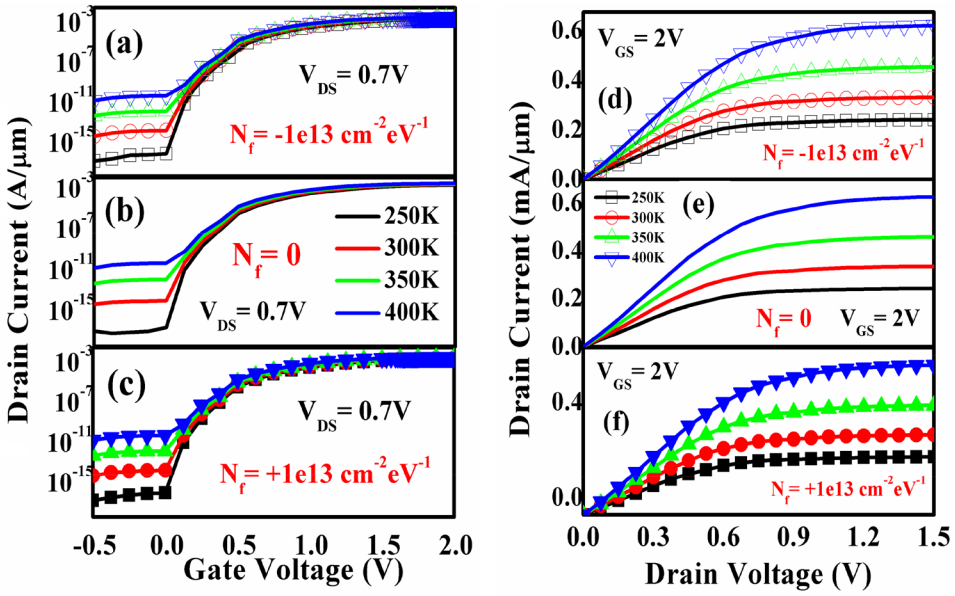

Fig. 10 Impact of temperature on transfer characteristics of proposed structure in the presence of **a** negative trap **b** no trap **c** positive trap conditions. Impact of temperature on output characteristics (I_D-V_{DS}) of proposed structure in the presence of **d** negative trap **e** no trap **f** positive trap conditions

positive and negative trap charge affected structure show almost similar behavior of transfer characteristics with temperature. The result shows that for trap affected and unaffected devices, the I_{OFF} increases from 10^{-17} to 10^{-11} A/μm when the temperature increases from 250 to 400 K. However, due to the inconsiderable increase in I_{ON}, the current switching ratio degrades from an order of 10^{14} to 10^{8}. Figure 10d–f illustrates the temperature dependence of output characteristics of the proposed structure in the presence and absence of interface traps. These plots show that the drain current increases with an increase in temperature, which is inconsistent with the previous results. The drain current increases from 0.242 to 0.627 mA for a temperature range of 250–400 K. However, the effect is unaltered for all types of traps at the interface.

The maximum effect of temperature is observed in the subthreshold region of the transfer characteristics of TFET. For this reason, a parameter called temperature sensitivity (S_T) is analyzed [35] for different trap charges as shown in Fig. 11. The result shows that the presence of acceptor and donor traps modify the temperature sensitivity by 33.33–66.67%, respectively, with respect to the undamaged device.

To illustrate the temperature affectability on device capacitance, the variation of total gate capacitance and gate-drain capacitance as a function of gate voltage for varying temperatures for an undamaged device are shown in Figs. 12a and b. The figure shows that C_{gg} increases with an increase in temperature from 250 to 400 K. Moreover, C_{gg} also increases with gate bias. The fact is that the inversion layer formed near the drain side extends to the source side as the gate bias is increased [48]. It is found from the figure that at 0.75 V gate voltage an increase of temperature from

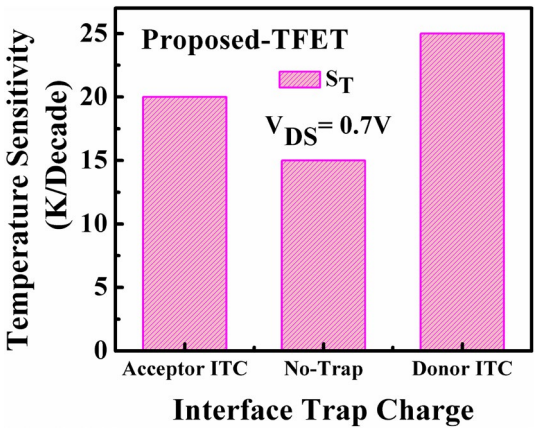

Fig. 11 Influence of ITCs on temperature sensitivity of the I_{OFF} variability of proposed TFET at different ITCs

250 to 400 K can increase the gate capacitance by 89.46%. In Table 3, some of the results of the proposed device are compared with some practical authentic sources [53–55].

4 Conclusion

A TCAD based comparative analysis in terms of dc and analog/RF performances between the conventional and a proposed PNPN TFET in presence of interface trap charges (donor and acceptor) is presented. In addition to this, the temperature affectability on the device characteristics is also studied and presented. The interface trap charges present in a nanoscale device create reliability issues on the device. We have performed a detail

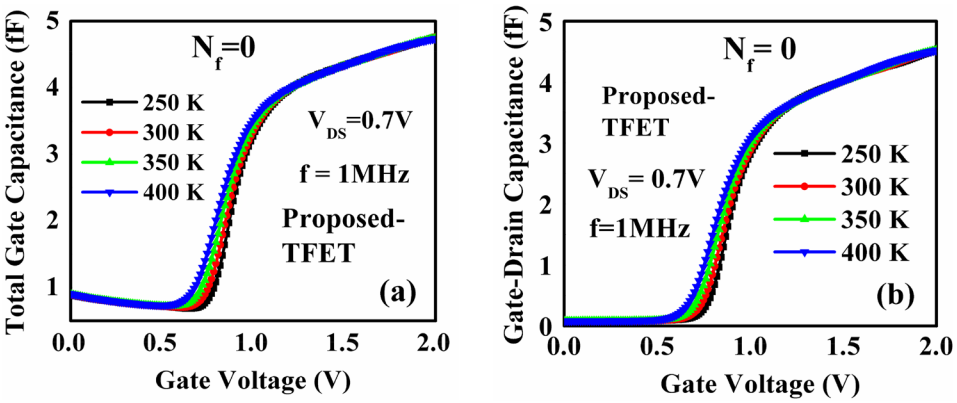

Fig. 12 Parasitic capacitance of proposed device as a function of gate voltage at various temperature (250–400 K) **a** C_{gg} **b** C_{gd}

Table 3 Comparison of results with practical authentic sources

	Ref [53]	Ref [54]	Ref [55]	This work
Device topology	Ge-TFET	SiGe/Si heterojunction	Si-Ge PAI pocket	Dual-k spacer overlapped
T_{ox}(nm)	3(SiO_2)	HfO_2/ SiO_2	SiO_2	2(HfO_2)
L_G (nm)	5000	1000	2000	22
I_{ON} (A/μm)	0.42×10^{-6}	20×10^{-6}	14.5×10^{-6}	1.72×10^{-3}
I_{OFF} (pA/μm)	0.12	10	0.1	6.5×10^{-3}
I_{ON}/ I_{OFF}	3E6	2E6	1.45×10^{8}	10^{11}
SS (mV/Decade)	~70	>120	80	45
V_D (V)	0.5	1.2	1	0.7

investigation on the effect of interface traps on both the conventional and proposed device in terms of dc as well as analog/RF performance and found that the proposed device shows lower distortion as compared to the conventional device with different interface trap charges (ITCs). It can also be used for low power applications and higher scale integration such as RF IC design, low power radio, low-power SAR ADCs, ultra-low-power receivers, etc. From the temperature analysis, it can be concluded that at lower gate voltage, the SRH recombination dominates and degrades the I_{OFF} and SS of the device at elevated temperature. However, at higher gate voltage, the BTBT mechanism dominates. Moreover, the analysis reveals that the impact of temperature is more prominent in subthreshold characteristics. In addition, the proposed device shows a positive temperature coefficient, irrespective of the presence of a type of trap charges. The study of device characteristics in the presence of the interface trap is very important, as these ITCs always exist in real devices. The performance enhancement achieved by the proposed TFET promises better reliability for high performance and low power switching applications.

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