Applied Physics A (2020) 126:614
https://doi.org/10.1007/s00339-020-03772-3

Applied Physics A
Materials Science & Processing

Electrical characterization of CdZnTe/Si diode structure

C. Dogru Balbasi[1,2] · M. Terlemezoglu[3,1,2] · H. H. Gullu[4] · D. E. Yildiz[5] · M. Parlak[1,2]

Received: 20 March 2020 / Accepted: 28 June 2020 / Published online: 15 July 2020

Abstract
Temperature-dependent current-voltage ($I-V$), and frequency dependent capacitance-voltage ($C-V$) and conductance-voltage ($G-V$) measurements were performed in order to analyze characteristics of CdZnTe/Si structure. Obtained profiles enable us to understand the different characteristics of the diode structure such as the carrier conduction mechanism and the nature of the interfacial layer. Over the temperature range between 220 and 340 K, taking consideration of the disparity in the forward-biased current, the diode parameters such as saturation current (I_0), zero-bias barrier height (Φ_{B0}) and ideality factor (n) have been obtained. The barrier height increased (0.53 to 0.80 eV) while the ideality factor decreased (4.63 to 2.79) with increasing temperature from 220 to 340 K, indicating an improvement in the junction characteristics at high temperatures. Due to the inhomogeneity in barrier height, the conduction mechanism was investigated by Gaussian distribution analysis. Hence, the mean zero-bias barrier height ($\overline{\Phi}_{B0}$) and zero-bias standard deviation (σ_0) were calculated as 1.31 eV and 0.18, respectively. Moreover, for holes in p-type Si, Richardson constant was found to be 32.09 A cm^{-2} K^{-2} via modified Richardson plot. Using the capacitance-voltage ($C-V$) and conductance-voltage ($G-V$) characteristics, series resistance (R_s) and density of interfacial traps (D_{it}) have been also investigated in detail. A decreasing trend for R_s and D_{it} profiles with increasing frequency was observed due to the impurities at the CdZnTe/Si interface and interfacial layer between the front metal contact and CdZnTe film.

Keywords CdZnTe · Thin film · Interface traps · Transport mechanism · Gaussian distribution

1 Introduction

Cadmium Zinc Telluride (CdZnTe) is a ternary II-VI semiconductor material with a high atomic number which provides strong absorption [1, 2]. It also has excellent optoelectronic properties and low leakage current due to its wide bandgap properties. CdZnTe is used in many important applications, such as solar cells [3], photodiodes [4], photoconductors [5], room temperature gamma-ray [6], X-ray detectors [7], infrared windows [8] and light-emitting diodes [9]. In this study, a detailed analysis of electrical properties of the CdZnTe/Si structure has been examined and it has been observed that Si semiconductor material could be a suitable heterojunction partner. The reasoning behind the production of CdZnTe/Si diode is the fact that the properties of Si material are very well-known which assists the evaluation of the electrical response of the film in the junction.

National Renewable Energy Laboratory (NREL) and EPIR Technologies conducted studies to develop CdZnTe-based top cells grown on p-Si solar cells as a platform to manufacture high-efficiency tandem cells [10]. Additionally, CdZnTe thin films deposited on Si substrates by molecular-beam epitaxy (MBE) have been studied to facilitate the production of HgCdTe IR detectors [11]. MOVPE growth of thick single crystal CdZnTe epitaxial layers on Si substrates were also studied for nuclear radiation detection applications [12]. In accordance with the corresponding studies, it was necessary to examine the electrical properties of the thermally evaporated CdZnTe/Si diode in a wide range of temperatures and frequencies for possible future applications. Therefore, we

✉ H. H. Gullu
hasan.gullu@atilim.edu.tr; hasanhgullu@gmail.com

1 Department of Physics, Middle East Technical University (METU), Ankara 06800, Turkey

2 Center for Solar Energy Research and Applications (GUNAM), METU, Ankara 06800, Turkey

3 Department of Physics, Tekirdağ Namık Kemal University, 59030 Tekirdag, Turkey

4 Department of Electrical and Electronics Engineering, Atilim University, 06836 Ankara, Turkey

5 Department of Physics, Hitit University, 19030 Çorum, Turkey

have conducted temperature-dependent current-voltage (I–V), frequency-dependent capacitance-voltage ($C-V$)and conductance-voltage ($G-V$)measurements under dark conditions. Temperature-dependent ($I-V$) measurements were performed to analyze the dominant conduction mechanisms through the junction and to determine the main diode parameters. In addition, frequency-dependent ($C-V$) and ($G-V$) measurements have been conducted to investigate junction properties and to understand the effect of the deep levels on the capacitance. Long-lived traps which are important to identify the physical processes in the diode, the relation between the formation of deep traps and possible degradation mechanisms were explored by extended range of frequencies [13].

2 Experimental details

CdZnTe/p-Si diode structure was prepared on p-type Si substrate having (100) orientation and 1 Ω•cm bulk resistivity with 2×10^{17} cm^{-3} doping concentration. The RCA-cleaned substrate was etched in a 10% HF solution for 10 s immediately before loading into the deposition chamber. Al back contact was thermally evaporated and annealed at 450 °C under the continuous N_2 flow to enhance the ohmicity of Al-contact. Then, CdZnTe layer was deposited by thermal evaporation method with a chamber pressure of 1×10^{-6} mbar at room temperature. The CdZnTe crystal pieces, which is used as a source material, were obtained from the ingots produced by Vertical Gradient Freeze (VGF) method in METU-CGL (Crystal Growth Laboratory) with the purity of 99.999% [14]. The rate of evaporation and film thickness were monitored and controlled by InficonXTM/2 quartz crystal monitor and CdZnTe film was deposited with a 5 Å/s evaporation rate and the final film thickness of this layer was measured as ~ 750 nm by Dektak 6 M profilometer. Deposited CdZnTe/p-Si was dipped into a solution of 2.1 g $CdCl_2$ in 100 ml methanol and annealed for 15 min at 300 °C under N_2 atmosphere prior to Au front contact formation. $CdCl_2$ treatment is a critical step to improve device performance. Then, 100 nm thick Au front contact was deposited using electron-beam evaporation and the fabricated structure was annealed at 100 °C to enhance the adhesion of the contacts to the film surface. The schematic cross-section of the Au/CdZnTe/p-Si/Al diode structure is shown in Fig. 1.

The temperature-dependent I–V measurements were performed using Keithley 2401 source-meter for the bias voltage of ± 3 V in the temperature range of 220–340 K. For these measurements, a CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium generator was used, and the temperature on the diode was adjusted using a Lakeshore DRC-91C controller. Additionally, the room temperature ($C-V$) and

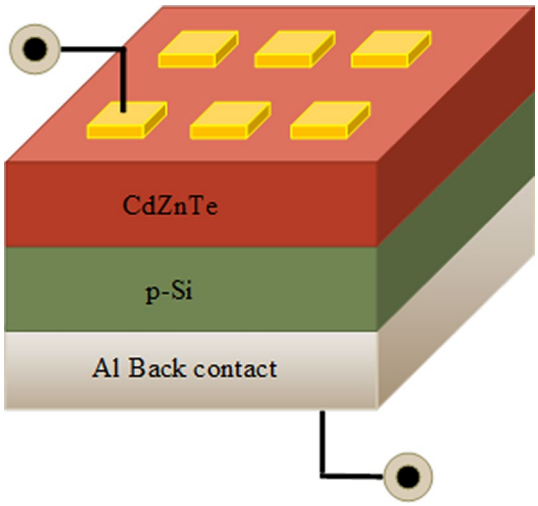

Fig. 1 Schematic cross-section of the Au/CdZnTe/p-Si/Al diode structure

($G-V$)measurements were carried out in a wide frequency range from 1 kHz to 1 MHz using computer-controlled Hewlett Packard 4192A LF model impedance analyzer.

3 Result and discussion

3.1 Temperature-dependent current–voltage analysis

Temperature-dependent ($I-V$) measurements were performed to determine the dominant conduction mechanisms and obtain the main diode parameters. Zero-bias barrier height (ϕ_{B0}) and ideality factor (n) are the two important parameters determined from ($I-V$) plots using thermionic emission (TE) theory. According to the diode equation [15], the forward-biased current can be modeled as;

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

where I_0 is the reverse-saturation current, q is the electronic charge, V is the voltage value in the forward bias region, n is the ideality factor, k is the Boltzmann constant and T is the ambient temperature. Figure 2 shows the ($I-V$) characteristics of CdZnTe/Si diode structure at various ambient temperatures. According to the measurement results, the forward current is higher than the reverse-biased current for all temperature values.

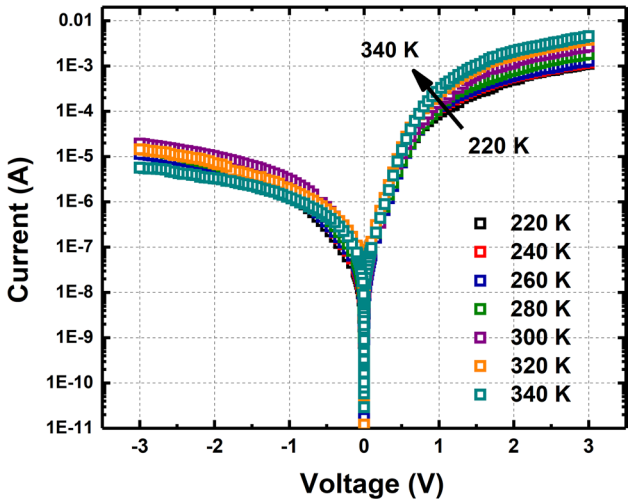

Fig. 2 $I-V$ characteristics of CdZnTe/p-Si diode structure at various ambient temperatures

Table 1 Diode parameters of CdZnTe/p-Si structure under dark conditions in the temperature range of 220–340 K

Temperature (**K**)	Ideality factor (**n**)	Saturation current ($\mathbf{I_0}$)(**A**)	Barrier Height $\mathbf{\Phi_{B0}}$ (**eV**)
220	4.63	1.68×10^{-8}	0.53
240	4.10	1.72×10^{-8}	0.58
260	3.76	2.16×10^{-8}	0.62
280	3.50	2.73×10^{-8}	0.66
300	3.18	2.77×10^{-8}	0.71
320	2.94	2.84×10^{-8}	0.76
340	2.79	3.95×10^{-8}	0.80

Intercepts of the $(I-V)$ plot with the current axis give the value of the I_0 values at any given temperature. I_0 value was used to estimate the ϕ_{B0} values using the relation

$$q\Phi_{B0} = -kT\ln\left(\frac{I_0}{A^*AT^2}\right) \tag{2}$$

where A^* is the effective Richardson constant and A s the device area. A^* value for p-type Si was used as 32 $\mathrm{Acm^{-2}\,k^2}$ under the assumption of uniform barrier height formation in the diode [15]. The obtained n, I_0, and Φ_{B0} values for each temperature are tabulated in Table 1.

As stated in Table 1, the increase in Φ_{B0} and decrease in n with increasing temperature indicates an improvement in the junction [16]. The increase in Φ_{B0} with temperature provides smaller leakage current and therefore an increase in the rectification behavior. However, at lower temperatures, the ideality factor much greater than unity results in deterioration of the device parameters [17]. Because of the observed temperature dependency in the analysis, the current transport at low temperatures was controlled by the current flowing across the patches of low barrier heights, resulting in a higher n value [18]. An apparent increase in the n and a decrease in the barrier height at low temperatures are probably caused by inhomogeneous barrier formation from low barrier patches [19]. However, TE theory is based on homogeneous barrier height formation in the junction. Considering the inhomogeneous barrier height formation and deviation from TE theory, Gaussian distribution (GD) of barrier height was studied based on a mean value $\bar{\Phi}_{B0}$ with the standard deviation of σ_0 to explain the carrier transport mechanism across the junction [20–23]. This approximation has been achieved by determining the degree of barrier height variation under the Tung's theoretical approach [24] and a good linear relationship between Φ_{B0} and n was obtained in Fig. 3. In Tung's model, bias and temperature dependent diode parameters extracted from bias and temperature independent patch parameters [24].

GD model was used to describe the potential fluctuations considering a continuous barrier distribution at the interface. Using the GD model, the total current is expressed as a sum of the current flows in all individual barrier patches [25]. Therefore, the total junction current dominated by low barrier patches is given as:

$$I = AA^*T^2\exp\left[\left(-\frac{qV}{kT}\right)\left(\Phi-\frac{q\sigma_0^2}{2kT}\right)\right]\exp\left(\frac{qV}{n_{ap}kT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{3}$$

with modified reverse saturation current,

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{ap}}{kT}\right) \tag{4}$$

where n_{ap} and Φ_{ap} are the apparent ideality factor and apparent barrier height, respectively. Using GD function, Φ_{ap} can be expressed as the temperature variation in Φ_{B0}:

$$\Phi_{\mathrm{ap}} = \overline{\Phi}_{\mathrm{B0}} - \frac{q\sigma_0^2}{2kT} \tag{5}$$

As represented in Fig. 4(a), Φ_{B0} has a linear relation with $q/2kT$ and from the analysis of intercept and slope, $\bar{\Phi}_{B0}$ and σ_0 have been determined, respectively. The value of σ_0 was found to be 0.18 while the $\bar{\Phi}_{B0}$ value was obtained as 1.31 eV. In the GD model, σ_0, which is a measure of the barrier homogeneity, shows 14% deviation from the mean value $\bar{\Phi}_{B0}$. According to the obtained values, the forward-biased

current mechanism in CdZnTe/Si diode conforms to a junction with GD of barrier height due to inhomogeneity of the interface layer and non-uniformity of interface charges. According to the GD model, ρ_2 and ρ_3, the coefficients indicating the voltage deformation of the barrier height distribution can be extracted from the following equation

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{6}$$

While Eq. 6 examines the relation between temperature and n, Fig. 4(b) shows the corresponding voltage deformation of the GD of the barrier height with respect to n. The voltage coefficients were determined from the intercept and slope of the straight line as, $\rho_2 = 0.0153$ V and $\rho_3 = 0.387$, respectively.

Finally, modified Richardson constant A^* was calculated for GD type inhomogeneous barrier height. Using Eq. 3, modified A^* can be determined as

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\overline{\Phi}_{B0}}{kT} \tag{7}$$

The modified Richardson plot using Eq. 7 was given in Fig. 5. The $\overline{\Phi}_{B0}$ and A^* values were found as 1.32 eV and 32.095 $Acm^{-2}\,k^{-2}$ from the slope and intercept of the $ln[(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)]$ vs. q/kT plot, respectively. The value of $\overline{\Phi}_{B0}$ obtained using Eqs. 4 and 7, were found to be very similar. Even the inhomogeneity of the barrier height exists in the diode, the modified A^* value was in accordance with the reported values [26].

3.2 Frequency-dependent capacitance–voltage analysis

In this study, the frequency dependence of the forward and reverse bias $(I-V)$ and $(G-V)$ characteristics of Au/CdZnTe/p-Si/Al diode structure have been investigated in the frequency range of 1 kHz – 1 MHz and voltage range of ± 3 V at room temperature.

As can be seen in Fig. 6a, b, capacitance and conductance of the diode show sensitivity to applied voltage and frequency. Capacitance values are decreasing while conductance increases with increasing frequency. The obtained higher values of capacitance at low frequencies in Fig. 6a can be attributed to the carrier charges at surface traps and their relaxation time, since they can easily follow the ac signal and yield an excess in the measured capacitance [27]. The capacitance at high frequency represents the response of free carriers, while capacitance at low frequency represents the response of not only free carriers but also deep trap levels [27–29]. Significant amount of deep trap levels may co-exist with the shallow levels and contribute noticeably to the space charge [30]. This is because the CdZnTe film may be non-intentionally doped which suggests that the free carriers are due to the defects. These defects may be intrinsic to the polycrystalline CdZnTe or due to extrinsic impurities such as Cl resulting from $CdCl_2$ treatment [31]. Ideally, the $(C-V)$ and $(G-V)$ characteristics are expected to be independent of frequency. Several mechanisms can give rise to a frequency dependent capacitance and conductance such as, Schottky barrier behavior, deep traps in CdZnTe, Cl diffusion, the front contact, interface traps and high series resistance [32, 33].

Additionally, R_s (series resistance) and D_{it} (Density of interface traps) are important parameters that significantly change both the $(C-V)$ and $(G-V)$ characteristics from ideal cases [32]. R_s parameter is effective in the forward bias region for high frequencies, while D_{it} is effective at low frequencies.

3.2.1 Series resistance (R_s)

It should be noted that the value of series resistance can affect both capacitance and conductance characteristics. The value of voltage-dependent resistance R_i can be extracted in the total measured range as

$$R_i = \frac{G_m}{G_m^2 + (\omega C_m)^2} \tag{8}$$

where ω $(2\pi f)$ is the angular frequency and C_m and G_m are the measured capacitance and conductance values for any voltage. Although this approach evaluates the effects of parasitic resistance in the total measured range, at sufficiently high frequencies $(f \geq 300kHz)$ and in the positive voltage region, it can be used to calculate the R_s values [22, 23, 32].

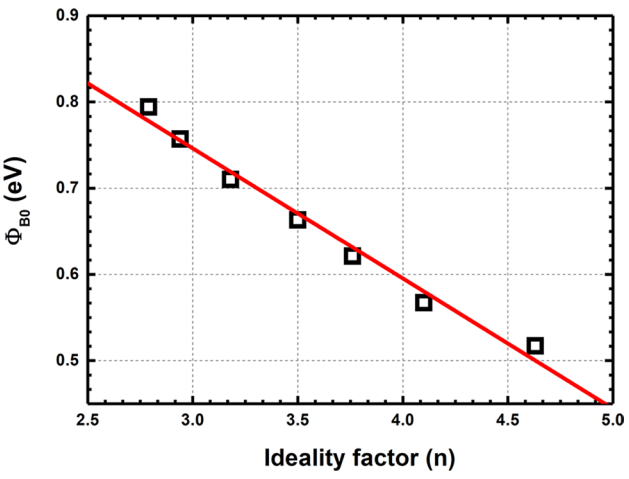

Fig. 3 The linear relation between barrier height and ideality factor for CdZnTe/p-Si diode structure

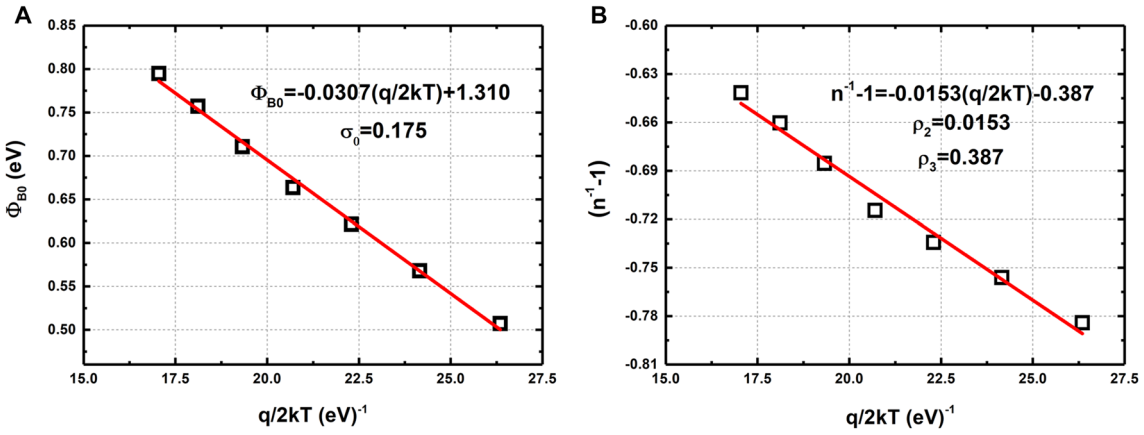

Fig. 4 Plot of **a** Φ_{B0} vs. $q/2kT$, and **b** $\left(n^{-1}-1\right)$ vs. $q/2kT$ for CdZnTe/p-Si diode structure

The applied bias voltage and frequency dependence profile of the R_s were evaluated according to Eq. 8 for high frequencies, and its characteristic behavior is presented in Fig. 7. As shown in the figure, the value of R_s increased with decreasing frequencies due to the impurities at CdZnTe/Si interface layer, front metal contact, and CdZnTe layer.

3.2.2 The density of interface traps (D_{it})

D_{it} can be attributed to the periodic lattice structure at the surface, surface preparation, interfacial layer, and impurities in the semiconductor. Hill-Coleman approximation technique is a quantitative method to obtain the density of interface traps [34]. According to this approximation, frequency-dependent $(C-V)$ and corresponding $G/w-V$ plots are

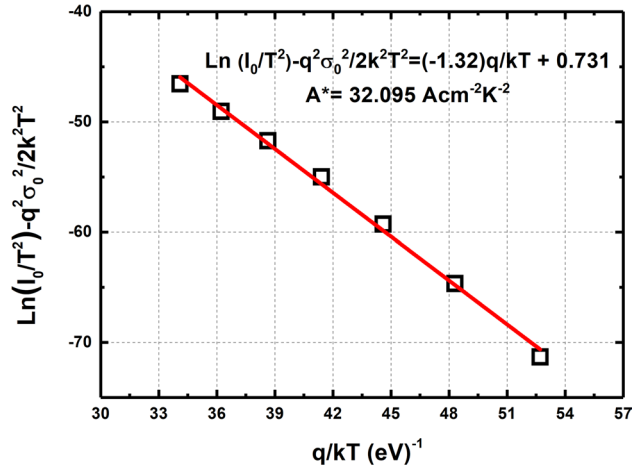

Fig. 5 $ln[(I_0/T^2)-(q^2\sigma_0^2)/(2k^2T^2)]$ vs. q/kT for CdZnTe/p-Si diode structure

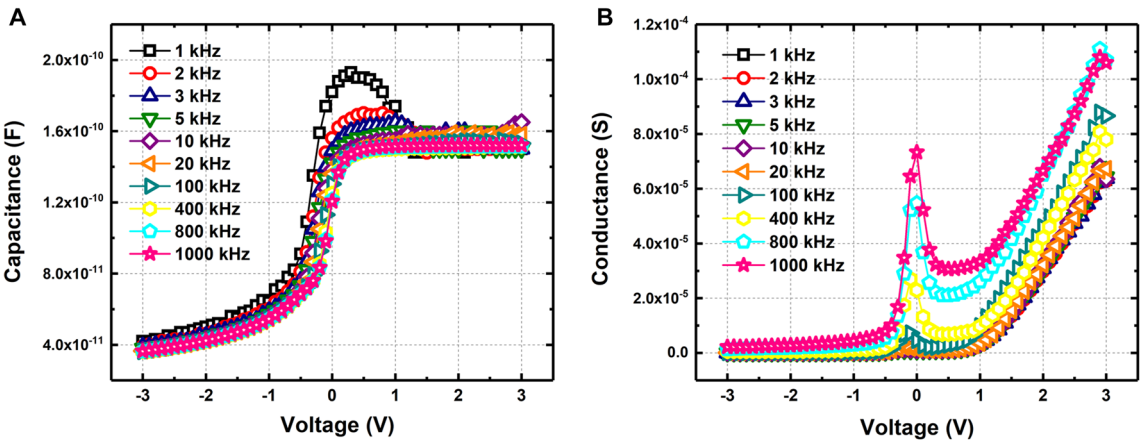

Fig. 6 Frequency dependence of **a** $(C-V)$ and **b** $(G-V)$ plots of CdZnTe/p-Si diode structure at room temperature

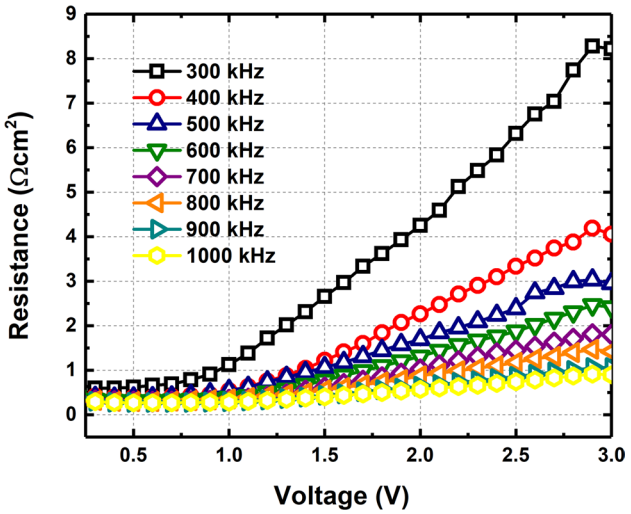

Fig. 7 R_s at different frequencies for the forward bias region of CdZnTe/p-Si diode structure under the dark condition at room temperature

required for the estimation of D_{it}. As a result, frequency dependence distribution of D_{it} can be determined as [35];

$$D_{it} = \left(\frac{2}{qA}\right)\frac{\left(G_m/w\right)_{\max}}{\left(\left(G_m/w\right)_{\max}/C_i\right)^2 + \left(1 - C_m/C_i\right)^2}, \quad C_i = C_m\left[1 + \frac{G_m}{wC_m}\right] \tag{9}$$

where q is the elementary charge, A is the diode area, G_m/w is the max-peak value of the measured conductance as shown in Fig. 8(a), C_m is the corresponding measured capacitance value and C_i is the interfacial capacitance.

The conductance can be considered as a measure of the interface trap density. It indicates loss mechanisms resulting from the capture of interface traps and emission of carriers [36]. To determine the distribution of density of interface trap, G/w was calculated using each $(C-V)$ and $(G-V)$ plots at several modulation frequencies. $G/w-V$ is then plotted to extract the maximum value of G/w at each frequency which in turn gives rise to D_{it}.

The frequency distribution of the calculated D_{it} values is given in Fig. 8(b) and the profile of the D_{it} shows a decreasing behavior when the applied frequency increased. When interface traps exist at the interface, the device behavior deteriorated due to these traps and their lifetime [36]. At low frequencies, the interface traps can follow the ac signal and cause an increase in calculated D_{it}. Nevertheless, the interface traps at high frequencies cannot follow an ac signal [34].

4 Conclusion

In this study, the electrical properties of the CdZnTe/p-Si structure were investigated using temperature-dependent $(I-V)$ and frequency-dependent $(C-V)$ and $(G-V)$ profiles. These profiles allowed us to understand the carrier conduction mechanism and the nature of the interfacial layer of the CdZnTe/p-Si structure. $(I-V)$ analysis indicated that the junction behavior showed good rectification. Hence, Si material can be considered as a suitable heterojunction partner to CdZnTe. Due to the inhomogeneity of the barrier height, as the temperature of the ambient

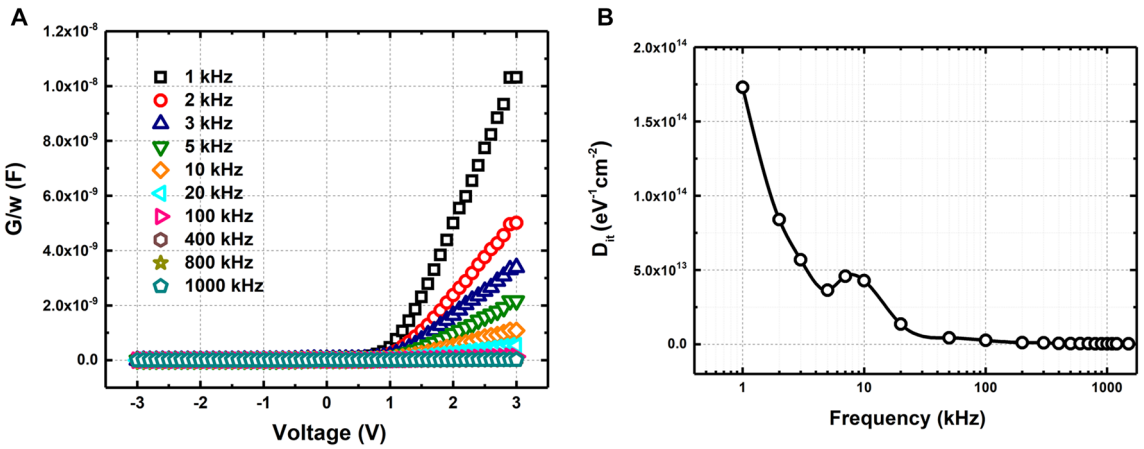

Fig. 8 Plots of **a** $G/w-V$ and **b** Corresponding frequency dependent distribution of D_{it} obtained using Hill- Coleman method for CdZnTe/p-Si diode structure

increased, n value of the diode decreased while Φ_{B0} was increasing. It has been confirmed that the inhomogeneity of the barrier height had a Gaussian Distribution behavior with $\overline{\Phi}_{B0}$ and σ_0 as 1.31 eV and 0.18, respectively. Additionally, using a modified Richardson plot, modified A^* was calculated as 32.09 A cm^{-2} K^{-2} which was approximately the same as the theoretical value for p-Si. Moreover, capacitance results showed sensitivity to frequency and decreased with increasing frequency. R_s value was observed to be more effective on the impedance measurements at high frequencies in the forward bias region while D_{it} was effective at low frequencies. Such non-uniformity in CdZnTe/Si structure was expected due to the diffusion mechanism of the extrinsic impurities such as Cl and the distribution of deep level traps from the complex nature of CdZnTe deposition and processing.

Compliance with ethical standard

Conflict of interest The authors declare that there is no conflict of interests regarding the publication of this manuscript.

References

1. D. Bonnet, P. Meyers, J. Mater. Res. **13**, 2740 (1998)
2. L. Kosyachenko, in Sol. Energy, edited by Radu D. Rugescu (IntechOpen, 2010).
3. A. Rohatgi, R. Sudharsanan, S.A. Ringel, M.H. MacDougal, Sol. Cells **30**, 109 (1991)
4. S. Chusnutdinow, V.P. Makhniy, T. Wojtowicz, G. Karczewski, Acta Phys. Pol. A **122**, 1077 (2012)
5. Y. Zhang, L. Wang, R. Xu, J. Huang, J. Tao, H. Meng, J. Zhang, J. Min, Appl. Surf. Sci. **388**, 589 (2016)
6. A. E. Bolotnikov, S. Babalola, G. S. Camarda, Y. Cui, S. U. Egarievwe, A. Hossain, G. Yang, and R. B. James, (2009).
7. T.E. Schlesinger, J.E. Toney, H. Yoon, E.Y. Lee, B.A. Brunett, L. Franks, R.B. James, Mater. Sci. Eng. R Reports **32**, 103 (2001)
8. D.S. Hobbs, B.D. MacLeod, Wind. Dome Technol. Mater. IX **5786**, 349 (2005)
9. P. Bouchut, J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. **9**, 1794 (1991)
10. M. Carmody and A. Gilmore, NREL Subcontract Rep. 1 (2011).
11. T.J. de Lyon, J. Electrochem. Soc. **141**, 2888 (1994)
12. M. Niraula, K. Yasuda, S. Namba, T. Kondo, S. Muramatsu, Y. Wajima, H. Yamashita, Y. Agata, I.E.E.E. Trans, Nucl. Sci. **60**, 2859 (2013)
13. D. Grecu, U. Jayamaha, G. Rich, and V. G. Karpov, Conf. Rec. IEEE Photovolt. Spec. Conf. 680 (2000).
14. Ö. B. Balbasi, Y. Ergunt, C. Dogru, M. Ünal, M. P. Kabukcuoglu, M. Parlak, and R. Turan, in Proc. SPIE 10762, Hard X-Ray, Gamma-Ray, Neutron Detect. Phys. XX, 107620R (San Diego, California, 2018), p. 29.
15. S.M. Sze, D.C. Mattis, Phys. Today **23**, 75 (1970)
16. S.S. Hegedus, W.N. Shafarman, Prog. Photovoltaics Res. Appl. **12**, 155 (2004)
17. A.A. Ojo, W.M. Cranton, I.M. Dharmadasa, *Next Generation Multilayer Graded Bandgap Solar Cells* (Springer, Cham, Switzerland, 2019)
18. F.E. Jones, B.P. Wood, J.A. Myers, C. Daniels-Hafer, M.C. Lonergan, J. Appl. Phys. **86**, 6431 (1999)
19. Ş. Aydoğan, M. Sağlam, A. Türüt, Appl. Surf. Sci. **250**, 43 (2005)
20. C. Bozkaplan, A. Tombak, M.F. Genişel, Y.S. Ocak, K. Akkilic, Mater. Sci. Semicond. Process. **58**, 34 (2017)
21. M. Terlemezoglu, O. Bayrakli, H.H. Güllü, T. Çolakoğlu, D.E. Yildiz, M. Parlak, J. Mater. Sci. Mater. Electron. **29**, 5264 (2018)
22. H.H. Güllü, M. Terlemezoğlu, O. Bayrakli, D.E. Yildiz, M. Parlak, Can. J. Phys. **96**, 816 (2018)
23. O.B. Sürücü, H.H. Güllü, M. Terlemezoglu, D.E. Yildiz, M. Parlak, Phys. B Condens. Matter **570**, 246 (2019)
24. R.T. Tung, Mater. Sci. Eng. R Reports **35**, 1 (2001)
25. R.T. Tung, Phys. Rev. B **45**, 13509 (1992)
26. R.C. Neville, J.J. Loferski, Phys. Today **35**, 65 (1982)
27. Y. Badali, Ş. Altındal, İ. Uslu, Prog. Nat. Sci. Mater. Int. **28**, 325 (2018)
28. M. J. Deen and F. Pascal, Springer Handbooks 1 (2017).
29. L.C. Kimerling, J. Appl. Phys. **45**, 1839 (1974)
30. J.V. Li, A.F. Halverson, O.V. Sulima, S. Bansal, J.M. Burst, T.M. Barnes, T.A. Gessert, D.H. Levi, Sol. Energy Mater. Sol. Cells **100**, 126 (2012)
31. J.S. Park, S. Kim, Z. Xie, A. Walsh, Nat. Rev. Mater. **3**, 194 (2018)
32. Ş. Altindal, A. Tataroğlu, I. Dökme, Sol. Energy Mater. Sol. Cells **85**, 345 (2005)
33. J. Poortmans and V. Arkhipov, Thin Film Solar Cells Fabrication, Characterization and Applications (John Wiley and Sons, 2006).
34. Dieter K. Schroder, Semiconductor Material and Device Characterization, Third Edition (John Wiley & Sons, 2005).
35. W.A. Hill, C.C. Coleman, Solid. State. Electron. **23**, 987 (1980)
36. R. Engel-Herbert, Y. Hwang, and S. Stemmer, J. Appl. Phys. **108**, (2010).