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Design and analysis of dual-gate misalignment on the performance of dopingless tunnel field effect transistor

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Abstract

The submitted work presents a designed and analyzed dopingless double-gate tunnel field effect transistor. In the designed dopingless structure, doping is introduced by charge plasma technique and silicon is used as a choice of material. Initially, gate misalignment was done by shifting the bottom gate away from the drain region and toward the drain region by 50% and 100% amount. Further, both gates (top and bottom) have been misaligned by 50% and 100% for analyzing the device for analog and linearity performance. Analog parameters, device parameters and linearity parameters were calculated in order to understand the device behavior. By misaligning gates, it is found that when the bottom gate is shifting away from the source region, both gates have been misaligned by 100% showing that analog and linearity performance of the devices degrades. When the bottom gate is shifted toward the source, both gates have been misaligned by 50% providing better analog and linearity performance. Among all the misaligned structures, when both gates have been misaligned by 50% gives the best result such as ON-state current, OFF-state current, I_{ON}/I_{OFF}, and subthreshold slope are 2.3 µA, 5.07 aA, 4.5×10^{11} and 32 mV/decade respectively.

Keywords Tunneling · Dopingless · Misalignment · Tunnel field effect transistor · Subthreshold slope · ON current

1 Introduction

As the miniaturization of circuits has taken place by scaling down the metal oxide semiconductor field effect transistors (MOSFETs) [1], scaling down the MOSFET [2] or Fin-FET [3] introduces a number of short-channel effects (SCEs) and higher leakage current (OFF-state current) which degrade the device performance [4]. Further, scaling is affected by the stringent power constraints and subthreshold slope that is non-scalable [4]. The theoretical limit of the subthreshold slope for a MOSFET is 60 mV/decade [5]. To reduce the subthreshold swing for MOSFET below 60 mV/decade is very difficult.

Therefore, intensive research is going on to find the alternative devices that could replace MOSFETs to achieve lower power dissipation and lower subthreshold swing as compared to MOSFET. One of the most efficient devices is tunnel field effect transistor (TFET) [6, 7] because of its lower OFF-state current, higher I_{ON}/I_{OFF}, lower subthreshold swing, threshold voltage and capability in suppressing the various SCEs [8–11].

For low voltage applications, Field effect transistor (FET)-based devices may not be used because of their higher subthreshold slope and low ON-current-to-OFF-current ratio (I_{ON}/I_{OFF}). TFET provides an alternative for low-voltage applications [12]. TFET has limitations to the ON current that is quite low, because current-carrying mechanism in TFET is primarily due to the band-to-band tunneling (BTBT) of electrons from source to channel [4]. In the case of FET-based devices, current flows because of the thermionic emission of electrons [4].

A lot of works have been done by researchers to improve the analog performance and ON-state current in the TFET device. Various techniques have been suggested by researchers for improving the ON-state current such as gate work function engineering [13], by using high-K gate dielectric [5], nanowire [14], by using heteromaterial or low bandgap material [15, 16], heterojunction [17], and nanotube [18]. These techniques

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provide a significant increment in the ON-state current or drain current. Negative capacitance technique is also employed for the optimization of TFET [19] that shows significant improvement in ON-state current and subthreshold swing. Further, some other structures for tunnel field effect transistors with modifications are analyzed for various applications such as heteromaterial planner TFET for sensing application [20] and dielectrically modulated dopingless TFET for biosensing application [21]

Using the double-gate technique, MOSFET has been designed for achieving better control on the drain current. For achieving the better control, both gates must be perfectly aligned. Aligning both gates is a difficult task [22–25]. Misalignment has been studied on double-gate MOSFET (DGMOSFET) by misaligning the top and bottom gate [26]. The studies reported in [23] found that misalignment toward the source side provides better resistance to SCEs as compared to source side misalignment. The work done by [27, 28] gives the misalignment effects on analog/RF performance on DGMOSFET and junction-less transistor. Till now the various studies have been done on misalignment effect on MOSFETs.

Misalignment effects on dopingless TFET (DLTFET) by misaligning the bottom gate with respect to the top gate are analyzed and compared with conventional double-gate TFET (DGTFET) [28]. The results conclude that DLTFET shows better analog/RF performance than conventional DGTFET when the bottom gate is misaligned by 50% toward the source [28]. When the bottom gate is misaligned toward drain, it was found that both devices present similar performance and performance decreases as misalignment increases toward drain [28]. TFET can be made cheaper by using dopingless technique, in which the required doping can be induced in the substrate by two methods such as charge plasma (CP) and electrostatic.

This paper is arranged as follows: Section II demonstrates the structures and simulation model. Section III presents the results and discussion followed by a conclusion. In this work, dopingless double-gate TFET (DLDGTFET) is demonstrated as a symmetrical device. Further misalignment technique has been introduced to make the TFET as an asymmetrical device, in which both top and bottom gates are misaligned. Further, device parameters, analog parameters, and linearity parameters have been studied and the results show significant improvement in the analog performance of misaligned DLDGTFET.

2 The designed device schematic and design specifications

A charge plasma (CP)-based DLDGTFET is designed and analyzed for device parameters, analog parameters, and linearity parameters. Figure 1 describes the 2-D cross-sectional view of symmetrical and asymmetrical DLDGTFET, in which different colors define the source, channel, drain electrodes, and oxides. Specifications for designing the DLDGTFET are mentioned in Table 1. Figure 1a shows the basic structure (BS) of DLDGTFET in which top and bottom gates are perfectly aligned. L_S, L_C, L_D, T_{OX}, T_{Si}, L_{SS}, and L_{DS} are the source length, channel length, drain length, equivalent oxide thickness, silicon body thickness, source spacer, and drain spacer length, respectively. In the designed DLTFET, electron and holes are induced by CP technique [29–31]. For forming source, gate, and drain regions, platinum metal electrode (work function 5.93 eV), polysilicon metal electrode (work function 3.9 eV), and hafnium metal electrode (work function = 3.9 eV) have been chosen, respectively. Hafnium and platinum metals form the drain and source regions, respectively, for satisfying the condition for CP technique for introducing n-type and p-type charge carriers in the drain and source region. CP techniques introduce the required doping concentration for source gate and drain

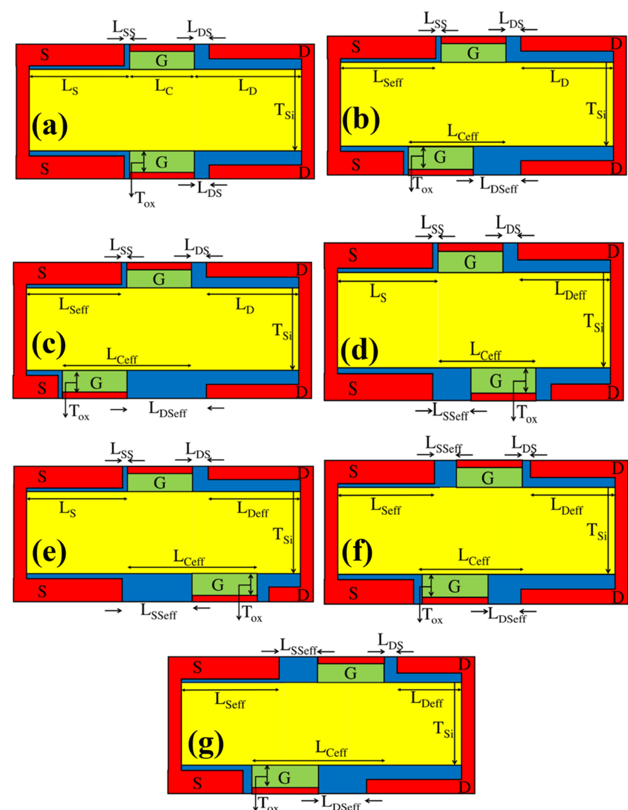

Fig. 1 **a** 2-D structure of designed basic structure (BS) of DLDGTFET. **b** Designed misaligned structure when source is underlapped by 50%. **c** Designed misaligned structure when source is underlapped by 100%. **d** Designed misaligned structure when drain is overlapped by 50%. **e** Designed misaligned structure when drain is overlapped by 100%. **f** Designed structure when both gates are misaligned by 50%. **g** Designed structure when both gates are misaligned by 100%

Table 1 Description for the specifications of DLDGTFET device parameter

Parameters	Specifications
Gate/channel length	50 nm
Source length	100 nm
Drain length	100 nm
Intrinsic body thickness	10 nm
Gate oxide material	HfO_2
Gate work function	4.5 eV
Source work function	5.93 eV
Drain work function	3.9 eV
Oxide thickness	4 nm
Source/drain oxide thickness	1 nm/3 nm

regions. Tunneling of the charge carriers takes place at the source–channel interface.

Figure 1b shows the DLDGTFET in which the bottom gate is shifted or misaligned toward the source side, i.e., source is underlapped by 50% (SU50). In other words, the bottom gate is moving away from the drain side and the device is going to be asymmetrical and effective channel length (L_{Ceff}) and effective drain spacer length (L_{DSeff}) are increased when compared to Fig. 1a. Further, in Fig. 1c, underlapping or misalignment of source with respect to the bottom gate is increased to 100% (SU100) causing L_{Ceff} and L_{DSeff} to increase further.

In Fig. 1d, the bottom gate is misaligned or overlapped with respect to the top gate by 50% toward the drain side (DO50). When the bottom gate is moving away from the source side, effective channel length (L_{Ceff}) and effective source spacer length (L_{SSeff}) increase. In Fig. 1e, drain overlapping is done by 100% (DO100) making the further increment in L_{Ceff} and L_{SSeff}.

In Fig. 1f, both top and bottom gates have been misaligned by 50% (BM50), i.e., top gate is moving toward the drain and the bottom gate is moving toward source. Because of BM50, L_{Ceff}, L_{SSeff}, and L_{DSeff} increase. When the misalignment is increased to 100% (BM100) as described in Fig. 1g, further increment in L_{Ceff}, L_{SSeff}, and L_{DSeff} can be seen.

All the mentioned devices in Fig. 1 were simulated using the Silvaco TCAD tool [32]. For proper functioning of the device, various physical models are taken into consideration. The models such as AUGER model, Shockley–Read–Hall (SRH) recombination and generation model, concentration-dependent mobility model (CONMOB), and Lombardi mobility (constant voltage and temperature) model are used for mobility and leakage currents [33, 34]. For quantum effects, Fermi–Dirac statistics are taken into consideration by using FERMI and FERMI.IN models [10]. For defining tunneling between source and channel interface, non-local band-to-band tunneling model is used [28, 31, 33].

3 Results and discussion

In this section, a detailed discussion regarding the working principle of DLDLTFET is provided by considering the gate misalignment. For misaligning, the bottom gate is shifted away from the drain and toward the drain. Further, both gates top and bottom are misaligned. All the structures are demonstrated in Fig. 1. Various parameters of the various devices are analyzed across device thickness and length. Internal parameters such as electric field, potential, energy band diagram, and carrier concentration and non-local band-to-band tunneling rate are calculated. The device behavior of all the structures demonstrated in Fig. 1 can be understood by seeing the graphs of internal parameters. Different colors show the results for BS, SU50, SU100, DO50, DO100, BM50, and BM100. The specifications for the designed BS are mentioned in Table 1. For understanding the proper functioning of the device, the designed device is calibrated with [5]. Figure 2a shows the calibration curve between the designed DLDGTFET and [5]. Figure 2b shows models were calibrated with the experimental work. Figure 2c shows the potential variation for BS as well as for all misaligned devices. Potential toward the source side is quite low because of the platinum metal electrode that has a high value of work function (5.93 eV). A platinum electrode is used toward the source side for inducing the p-side region in which holes are the majority charge carriers. Due to the introduction of holes, potential toward the source side is negative and increases further. There is an early rise in the potential for SU100, i.e., shown by the blue line in Fig. 2c, as the bottom gate is moved away from the drain. Because of 100% misalignment toward the source side by bottom gate, source–channel interface is created earlier. That interface forms an abrupt junction where 100% source is underlapped by the bottom gate. Further, potential increases inside the n-type channel where electrons are the majority carrier. Potential increases until the top gate comes into the picture. The top gate also forms the abrupt junction and induced n-type charge carriers to cause the potential to increase further. Toward drain side, potential is maximum and remains nearly constant for all the device structures. Potential variation for remaining structures varies similarly for BS, SU50, DO50, DO100, BM50, and BM100 shifts toward the right side. Figure 2d demonstrates the variation of the electric field in BS and misaligned devices. The electric field is defined as the negative of the slope of potential with respect to distance. In Fig. 2c for SU100, the slope is small in the source region and potential variation from a higher negative value to the lesser negative value

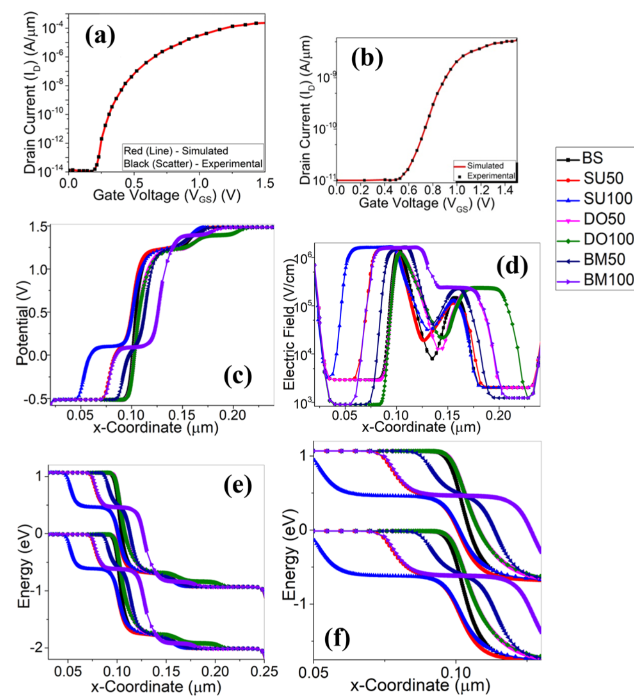

Fig. 2 **a** Calibration curve. **b** Calibration curve with the experimental work [35]. **c** Potential variation across the designed device in ON-state. **d** Electric field variation across the device structure in ON-state. **e** Energy band diagram for the designed device in ON-state. **f** Energy band diagram of the designed device

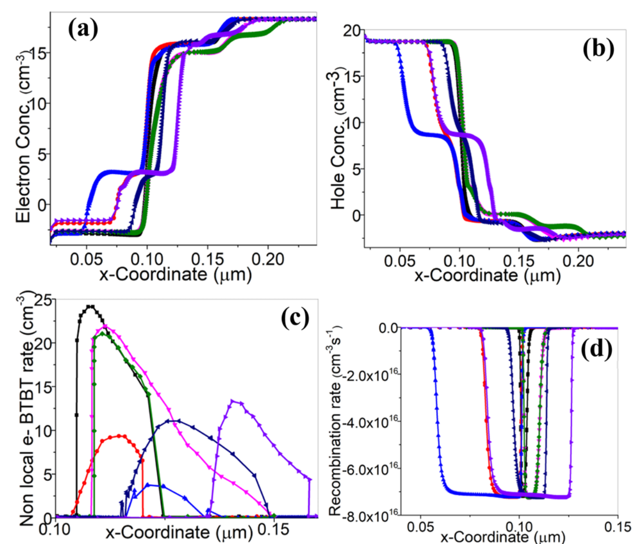

Fig. 3 **a** Electron concentration across the device structure at ON-state. **b** Hole concentration across the device structure at ON-state. **c** Non-local band-to-band tunneling rate across device structure. **d** Recombination rate across device structure

causes an electric field to decrease and it is minimum at the center beyond which slope is again increasing. As soon as the source and channel interface due to the bottom gate is formed, it has a depletion region on both sides of the interface. In that region, the electric field increases up to the charge neutrality point (CNP) because the slope of potential increases and it is maximum at that point. As we move away from the CNP, potential increases and slope decreases; hence, the electric field decreases. Further, potential varies in the positive direction and slope increases gradually and electric field decreases. Hence, electric field variation for all the structures follows the slope variation in the potential curve. Figure 2e, f describes the energy band diagram, and it is calculated in the ON-state at $V_{GS} = V_{DS} = 1$ V. Blue line shows the energy variation in conduction and valence band for SU100. The source–channel interface is formed earlier because the source is underlapped by 100% due to the bottom gate. At the interface, p-type source and n-type channel form the reverse bias junction. Because of the reverse bias junction and concentration gradient band, bending takes place at the interface between the source and bottom gate. Further, it remains nearly constant until the interface between the source and channel due to the top gate comes into the picture. That interface also forms a reverse bias junction and causes bands to bend further.

Because of the band bending depletion, width between source and channel decreases and overlapping between valance band of source and conduction band of channel increases, i.e., the requirement for tunneling to takes place. For BS, band overlapping between valance band of source and conduction band is maximum and shown by the black line. At the drain side, channel and drain form n–n-type interface and because of that, energy remains almost constant. Similarly, for BS, SU50, DO50, DO100, BM5, and BM100 bands, bending takes place and shifts toward the right side based on the percentage of misalignment of the gate.

Figure 3a, b represents the electrons and holes concentration in the BS and misaligned devices. As described in the figure, blue line describes for SU100 that shows an early increase in electron concentration, in which p-type source and n-type channel due to bottom gate form an interface earlier as compared to other structures as shown in Fig. 1; hence, electron concentration raises in the channel, and further, it goes nearly constant. At the interface between channel under the top gate (n-type) and source (p-type), again electron concentration increases. Electron concentration reaches maximum toward the drain side where channel and drain both are of n-type. Electron concentration remains nearly constant in the drain region. The reverse is happening for the holes concentration as it is maximum toward the source side (p-type) and it decreases inside the channel (n-type) and it is minimum toward the drain side (n-type). Similar variation can be seen in all misaligned structures for electron and hole concentration

variation such as BS, SU50, DO50, DO100, BM50, and BM100.

Non-local BTBT rate and recombination rate are demonstrated in Fig. 3c, d. Black line shows the variation in the BTBT rate for BS in which it is the highest. It has the maximum value of drain current because the overlapping of bands between source and channel is the highest and depletion width is least. More number of electrons can tunnel from the valence band of p-type source to the conduction band of n-type channel causing BTBT rate to be highest, and electrons are tunneling up to a significant distance. But the recombination of carriers is taking place at the source–channel interface, and recombination rate width is the least as shown in Fig. 3d. The recombination of charge carriers is taking place at the interface of p-type source and n-type channel. Similarly, for blue line that demonstrates the SU100 structure, it can be seen in Fig. 2e that very small band is overlapped; hence, in Fig. 3c, tunneling rate is minimum. The bottom gate misalignment toward the source by 100% shows approximately zero tunneling rates. Tunneling starts between the source and channel due to top gate, and tunneling takes place inside the channel for the distance as described in Fig. 3c. But recombination of charge carriers has started earlier as compared to other structures because the source is underlapped by 100% due to bottom gate misalignment. And recombination of charge carrier can be seen for a longer distance as compared to BS, and it is up to the source–channel interface due to top gate as shown in Fig. 3d. Similarly, variations in the BTBT rate and recombination rate take place for the remaining devices, such as SU50, DO50, DO100, BM50, and BM100. Drain current in the log and linear scale is given in Fig. 4a, b, respectively. Simulation is done by varying the gate voltage (V_{GS}) from 0 to 1 V for a constant value of V_{DS}, i.e., 1 V. For the structure, BM100 drain current rises earlier than other structures and it increases parabolically as V_{DS} increases further and represented by the purple color in Fig. 4a. Similarly, for remaining structures, drain current rises a little later and shifts toward the right side as shown in log scale of I_{DS} vs. V_{GS} graph. In the linear graph, it is visible by royal blue color that the current in the ON-state is maximum for the BM50 structure at $V_{DS} = 1$ V and is in the range of microampere. It rises later than BM100 and crosses BM100 to reach the maximum value. Current for this structure is highest because various factors are responsible for maximizing the drain current such as tunneling rate, distance traveled by charge carriers during tunneling, recombination rate and overlapping between bands. In Fig. 2e, overlapping of bands for BM50 is sufficient to start the tunneling of carriers from source to channel. Tunneling rate for this structure is less as compared to other structures such as BS, DO50, DO100, and BM100 but more than SU50, SU100. However, it has the highest amount of ON-state current. When top and bottom

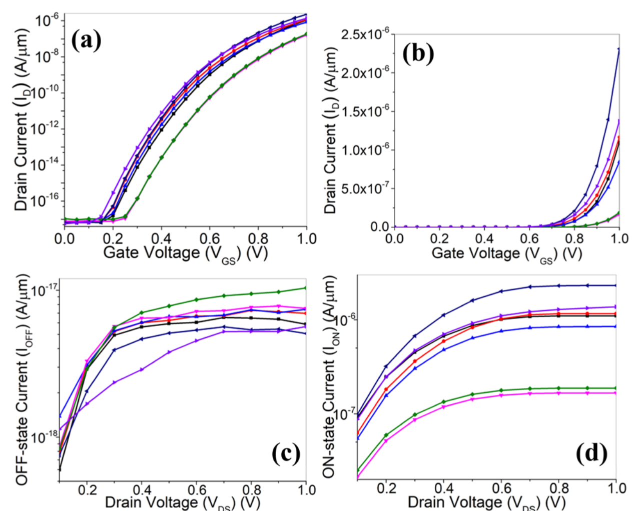

Fig. 4 **a** Drain current–gate voltage characteristics of device at $V_{DS} = 1$ V in log scale. **b** Drain current–gate voltage characteristics of device at $V_{DS} = 1$ V in linear scale. **c** OFF-state current variation with drain voltage. **d** ON-state current variation with drain voltage

both gates have been misaligned by 50%, i.e., top gate is shifted toward right and bottom toward left, tunneling starts at the interface between the source and channel formed due to top gate. At the interface between the source and bottom gate, recombination is happening and contributing in the current source. Carriers tunnel to a very far distance as compared to other misaligned structures except DO50 structure in which carriers are tunneling to the maximum distance, but tunneling rate falls very rapidly. For the structure DO50 and DO100, ON-state current is less when compared with other structure as shown in Fig. 4a, b. It can be seen in Fig. 3c that tunneling rate is more for DO50 and DO100, but tunneling rate falls very speedily. Distance travelled by charge carriers during recombination for DO50 and DO100 is also less causing drain current to be lowered.

Figure 4c demonstrates the OFF-current for all the structures. For the structure, when the bottom gate is misaligned by 100% (DO100) shows the maximum value of OFF-state current and shown by the green line in Fig. 4c. In other words, we can say that shifting the bottom gate toward drain causes effective source length to increase; hence, OFF-current is more. DO50 also resembles the same behavior by misaligning bottom gate by 50% toward drain, and effective source length increases but lesser than DO100; hence, OFF-state current is more but lesser than DO100. When both gates have been misaligned by 50% and 100% (BM50 and BM100) shown the least amount of OFF-state current, it increases as VDS increases. Figure 4d shows the ON-state current and can be seen that as VDS increases, current increases for all the structures. ON-state current is maximum for BM50 structure when both the gates are misaligned and

least for DO50 structure when the bottom gate is shifted toward drain by 50%.

Figure 5 describes the ON-state current-to-OFF-state current ratio (I_{ON}/I_{OFF}), threshold voltage (V_{TH}), subthreshold slope (SS), and average subthreshold slope (AVSS). In Fig. 5a, I_{ON}/I_{OFF} is increasing as V_{DS} increases and it goes maximum when both gates have been misaligned by 50% (BM50) at $V_{DS}=1$ V as shown by royal blue color. As effective source length is increasing for the structure DO50 and DO100, ON-state current and OFF-state current as shown in Fig. 4c, d show the worst behavior among BS, SU50, SU100, BM50, and BM100 and cause I_{ON}/I_{OFF} to be lowered. In threshold voltage curve in Fig. 5b, V_{TH} is the most for all the devices at $V_{DS}=0$ V and it decreases as V_{DS} increases. With respect to the BS, V_{TH} is more for DO50 and DO100. V_{TH} is less for SU50, SU100, BM50, and BM100 and shows very small variation as V_{DS} increases. For the purple color in Fig. 5b, V_{TH} is less for a small value of V_{DS} and again is the least for $V_{DS}=1$ V causing I_D to rise earlier than other structures (Fig. 4a). The subthreshold slope defines the rate of increase in the drain current with respect to the V_{GS}. Its variation with V_{DS} is demonstrated in Fig. 5c. As V_{DS} is approaching toward 1 V, SS is shifting toward V_{DS}. When effective source length is increasing, the bottom gate shifted toward the right side shows the maximum value for SS. It means that the rate of drain current with V_{GS} is small and I_D changes slowly for a higher value of V_{GS} as shown in Fig. 4a. For the royal blue color (Fig. 5c), SS is giving the least value among other structures which causes drain current to rise faster and reaches a maximum value at $V_{DS}=1$ V (Fig. 4a). DO50, D0100, and BN100 show the higher value of SS with respect to BS, and SU50, SU100, and BM50 show the smaller value of SS with respect to BS. Average subthreshold slope (AVSS) is defined by the following equation [31]:

$$\text{AVSS} = \frac{\left(V_T - V_{OFF}\right)}{\log\left(I_{VT}\right) - \log\left(I_{VOFF}\right)} \quad (1)$$

where V_T is the threshold voltage, V_{OFF} is defined as gate voltage from where drain current takes off, I_{VT} is the drain current at $V_{GS}=V_T$, and I_{OFF} is the drain current of the device at $V_{GS}=V_{OFF}$ [31]. The graph is shown in Fig. 5d that AVSS initially decreases and then increases as V_{DS} is increasing. For DO50 and DO100, AVSS is higher than BS. And for remaining structures, AVSS is lowered than BS. Least value is shown when both gates have been misaligned by 100%. BM50 structure also resembles the same with a small variation than BM100.

By scaling down the device dimension, there is a possibility for noise to corrupt its operated signal easily. Also, for using the device for low noise application in CMOS technology, the device must have a higher signal-to-noise ratio, high linearity for output parameters, and lower distortion [31]. As intermodulation distortion introduced in different frequency components, device performance degrades. Hence it is necessary to study the linearity parameter of the device. Gate oxide thickness of 4 nm is used in the designed device that makes the gate current to be zero and reduces the possibility of interference with the drain current. By scaling down the device, we are making it to operate at low supply voltage with higher signal to noise ratio for better detection of weak input signal. The linearity parameters that were calculated and analyzed for the BS and misaligned structures such as SU50, SU100, DO50, DO100, BM50, and BM100 are second-order transconductance (g_{m1}), second-order transconductance (g_{m2}), third-order transconductance (g_{m3}), third-order intermodulation distortion (IMD3), third-order input interception point (IIP3), second-order and third-order harmonic distortion (HD2 and HD3) [36–39]. These parameters can be calculated using the following equations:

$$g_{m1} = \frac{dI_{DS}}{V_{GS}}\ \text{S} \quad (2)$$

$$g_{m2} = \frac{d^2 I_{DS}}{dV_{GS}^2}\ \text{SV}^{-1} \quad (3)$$

$$g_{m3} = \frac{d^3 I_{DS}}{dV_{GS}^3}\ \text{SV}^{-2} \quad (4)$$

$$\text{IIP3} = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s}\ \text{dBm} \quad (5)$$

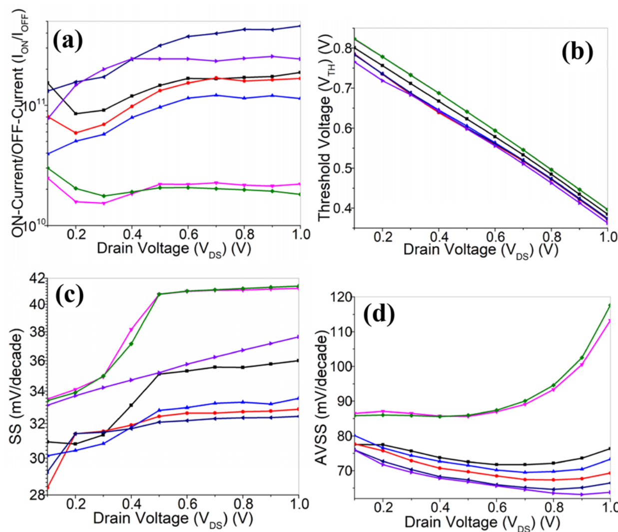

Fig. 5 **a** I_{ON}/I_{OFF} ratio variation with drain voltage. **b** Threshold voltage variation with drain voltage. **c** SS variation with drain voltage. **d** AVSS variation with drain voltage

$$\mathrm{IMD3} = \left(\frac{9}{2} \times (\mathrm{VIP3})^3 \times g_{\mathrm{m3}}\right)^2 \times R_\mathrm{s} \ \ \mathrm{dBm} \tag{6}$$

$$\mathrm{HD2} = \frac{1}{2} \times V_{\mathrm{in}} \times \frac{\left(\frac{\partial g_{\mathrm{m1}}}{\partial V_\mathrm{G}}\right)}{2g_{\mathrm{m1}}} \ \ \mathrm{dBm} \tag{7}$$

$$\mathrm{HD3} = \frac{1}{4} \times V_{\mathrm{in}}^2 \times \frac{\left(\frac{\partial^2 g_{\mathrm{m1}}}{\partial V_\mathrm{G}^2}\right)}{6g_{\mathrm{m1}}} \ \ \mathrm{dBm} \tag{8}$$

where Rs is 50Ω and Vin is 50 mV for the alternating current (AC signal).

First-order transconductance (g_{m1}), second-order transconductance (g_{m2}), and third-order transconductance (g_{m3}) values are shown in Fig. 6. It demonstrates that for the royal blue color, the g_{m1} is maximum near the operating voltage. SU50, SU100, and BM50 have a value higher than BS and DO50, and DO100 and BM100 has a smaller value than BS. A higher value of BM50 structure is responsible for the higher gain of the device among other misaligned structures. Variation of g_{m2} with changes in the misaligned percentage is also described in Fig. 6. g_{m2} also resembles the same curve as g_{m1} but has a higher value than g_{m1}. g_{m2} is the highest when both gates have been misaligned by 50% and the lowest for DO50, DO100, and BM100 structures. g_{m3} has also been plotted with respect to the applied gate-to-source voltage for various misaligned structures. The distortion limit and stable operation point are decided by the g_{m3}. In the g_{m3} curve, BM50 shows the maximum value and BM100 shows the least value.

Second-order and third-order harmonic distortions were calculated for all the misaligned structures including BS in order to find the better device for low noise operation and demonstrated in Fig. 7a, b. Harmonic distortion value for a device that is better for low noise operation should be low. As shown in Fig. 7a, it is seen that distortion near the lower gate voltage by all the devices is very high and it decreases as gate voltage increases. When both gates top and bottom have been misaligned by 50%, it has the highest peak around lower VGS. Least value is also achieved by the structure in which both gates have been misaligned by 50% as shown by royal blue color. In Fig. 7b, HD3 also has the maximum value for royal blue color and it decreases as VGS is increasing and the least value is also achieved by the royal blue color.

Third-order input intercept point is described in Fig. 8a, and it is used in determining the theoretical point at which amplitude of the third-order harmonic distortion and the input signal has the same value. If the linearity of the device for a particular frequency needs to be checked, then IIP3 point needs to be calculated. For a device to be linear at the particular frequency, IIP3 point should have a maximum value. In Fig. 8a, for lower gate voltage, all the devices have nonlinear behavior as the VGS is increasing and IIP3 is also increasing. As compared to the BS structure, SU50, SU100, and BM50 have more IIP3 value. For DO50, DO100, and BM100, it shifts toward downside with respect to BS variation. IMD3 is plotted for the BS and other misaligned structures such as SU50, SU100, DO50, DO100, BM50, and BM100 in Fig. 8b. It should have maximum value for a better device. With respect to the fundamental harmonic for amplitude modulated signal that has more than one frequency component, signal amplitude for third-order harmonic is represented by IMD3. For BS structure, when both top and bottom gates are perfectly aligned, IMD3

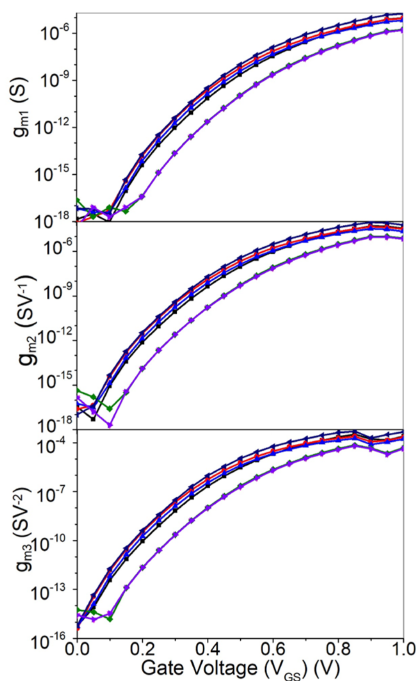

Fig. 6 Transconductance (g_{m1}), second-order transconductance (g_{m2}), and third-order transconductance (g_{m3}) variation with applied gate voltage

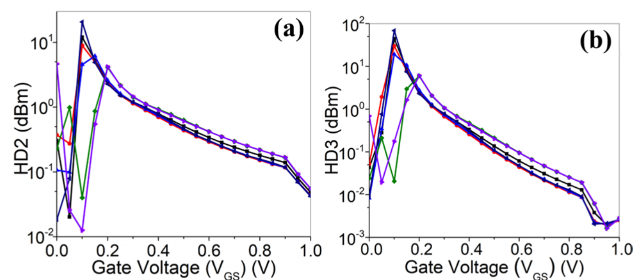

Fig. 7 **a** Second-order harmonic distortion variation with applied gate voltage. **b** Third-order harmonic distortion variation with applied gate voltage

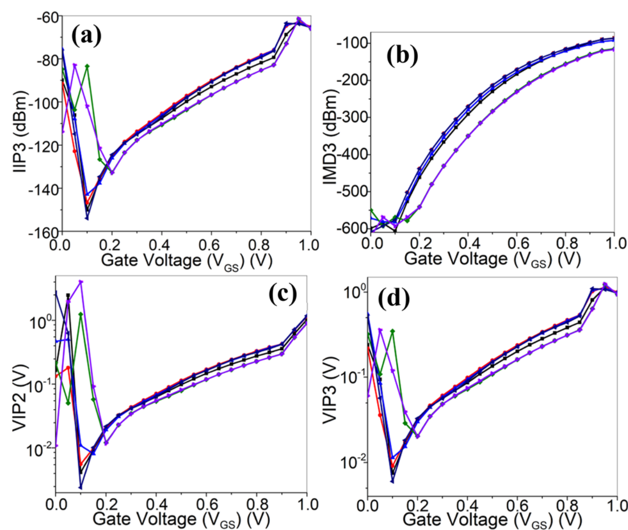

Fig. 8 **a** IIP3 variation with applied gate voltage. **b** Third-order IMD variation with applied gate voltage. **c** Second-order voltage intercept point variation with applied gate voltage. **d** Third-order voltage intercept point variation with applied gate voltage

variation in Fig. 8a is described by black line. SU50, SU100, and BM50 have the value IMD3 more than BS. For DO50, DO100, and BM100, it shifts to downward with respect to BS. BM50 and SU50 have the maximum value of IMD3 and resemble nearly same pattern as V_{GS} increases.

Figure 8c, d represents the VIP2 and VIP3 for all the structures. For the device to have high linearity, these values should be high. VIP tells about the input voltage at which amplitude of the first harmonic of output drain current and third harmonic of drain current goes equal. As shown in the figure, it shows that for lower gate voltage, all the structures have higher VIP value and it decreases rapidly. Further, with an increase in VGS, VIP value increases for all the structures. With respect to BS, SU50, SU100, and BM100 have higher values of VIP3 and are upward to black line. For DO50, DO100, and BM100, VIP value is lowered. Figure 8d shows that VIP3 has a lower value as compared to VIP2 which signifies that third-order harmonic has more amplitude than second harmonic. And it is also more for SU50, SU100, and BM50 and lowered for DO50, DO100, and BM100 with respect to BS.

4 Conclusion

The charge plasma-based dopingless double-gate TFET is designed and analyzed. The designed device is initially misaligned by 50% and 100% by shifting the bottom gate toward the source and toward the drain. Further, both gates (top and bottom) are misaligned by 50% and 100% to find the device performance. Designed structure confines the possibility of interface misalignment during the fabrication process. The device with all the misaligned structure is analyzed for analog and linearity parameters. And results for analog performance show that when both gates have been misaligned by 50%, BM50 gives the better analog performance as compared to other structure. For BM50, ON-state current, OFF-state current, I_{ON}/I_{OFF}, and subthreshold slope are 2.3 μA, 5.07 aA, 4.5×10^{11}, and 32 mV/decade, respectively. In the linearity parameters, second-order transconductance (g_{m1}), second-order transconductance (g_{m2}), third-order transconductance (g_{m3}), third-order intermodulation distortion (IMD3), third-order input interception point (IIP3), second-order and third-order harmonic distortion (HD2 and HD3) are calculated. The result shows that the BM50 structure gives overall better performance among other structures and makes it suitable for low-voltage sensing applications.

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