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An insight to the performance of vertical super-thin body (VSTB) FET in presence of interface traps and corresponding noise and RF characteristics

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Abstract

We investigated vertical super-thin body (VSTB) FET performance in presence of different interface (HfO_2/Si) trap distributions (uniform and Gaussian) and concentrations using TCAD tools. For trap concentration (TC) of 10^{13} eV^{-1} cm^{-2}, the percentage change in on-to-off current ratio (I_{on}/I_{off}) is 93.91% for uniform trap (UT) and 49.8% for Gaussian trap (GT) distribution. For the same TC, subthreshold swing (SS) shows percentage change of 5.1% for UT and 11.41% for GT distribution. Thus, the device performance shows good immunity for TC up to 10^{13} eV^{-1} cm^{-2}. However, for TC = 10^{14} eV^{-1} cm^{-2} SS degrades significantly. The influence of traps on the cumulative effect of three noise sources (diffusion + generation–recombination/G–R + flicker) and on individual noise sources (G–R and diffusion) is explained qualitatively at low and high frequencies (f = 1 MHz and 10 GHz). The study shows that the overall noise cannot disturb the device performance at very high frequency. Various radio-frequency (RF) parameters like transconductance (g_m), total input capacitance (C_{gg}), gate-drain capacitance (C_{gd}), unit-gain cutoff frequency (f_T), and gain–bandwidth-product (GBP) are also studied for variation of trap types. For TC = 10^{14} eV^{-1} cm^{-2}, the percentage change in f_{Tmax} (GBP_{max}) is − 21.43% (− 8%) for UT and − 22.86% (− 9.6%) for GT distribution.

1 Introduction

Since the invention of transistor, outstanding evolution of semiconductor industry has made the world's electronic life faster and easier beyond imagination [1]. The origin of this tremendous growth of microelectronic industry is the continuous down-scaling of transistor size. Various parasitic capacitances involved in a circuit also reduce with the down-scaling of device size and thereby, speed of the circuit is enhanced [2–4]. However, the adverse effect of various short channel effects (SCEs) on device electrical characteristics is becoming more severe with every advancement of transistor technology [5]. At different phases of time, microelectronic industry came up with unique solutions to the increasing problem of SCEs. Down-scaling of planer 2-D MOSFETs has achieved its physical limit long ago and hence, these are being replaced by new FET architectures such as SOI FETs, multi-gate FETs, FinFETs etc. However, these contemporary devices have their own limitations. SOI FETs, which outperform 2-D planer FETs in terms of speed and power consumption, are not being largely produced anywhere in the world due to its costly wafer development process [6–9]. Using double-gate in a planer FET enhances gate control and provides increased drive current (I_{on}) by creating two separate 2-D inversion layers. However, these inversion layers may overlap with each other beyond a critical body thickness (5 nm or less) [10, 11]. In such case, carriers in the overlapped channels encounter two opposite gate-fields as a consequence of which carrier–carrier scattering and surface roughness scattering increases and thereby I_{on} degrades [11–14]. Further, on-current (I_{on}) degradation due to SOI-thickness-fluctuation-induced-scattering in thin-body multi-gate transistors limits scaling of device size [14]. Double/triple gate FinFETs with very thin fins also suffer from I_{on} degradation for the same reason explained for multi-gate planer FETs. Besides, down-scaling of FinFETs demands high aspect ratio (height to width) fins. But, manufacturing of such fins is becoming a challenging task for lower technology nodes, as these 3-D fins standing alone may be

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damaged/washed away during cleaning, particularly when using sonication for enhanced particle removal, which is important for cleaning of 3-D relief [10, 11, 15, 16].

Therefore, we need a reliable FET architecture which is capable of mitigating the current limitations of various contemporary devices (SOI FETs, multi-gate FETs, and FinFETs). In 2014, a new FET structure called vertical superthin body (VSTB) FET [11] was proposed. VSTB FET is a single-gate structure, in which its vertical thin body is firmly supported by one or more shallow trench isolation (STI) dielectric walls. Unlike multi-gate FETs, a single gate controls overall electrostatics of such device; thus for ultra-thin body (UTB) dimensions, carrier–carrier scattering reduces in the channel and I_{on} improves [10–14]. Also, STI dielectric wall supports the vertical thin body to enhance its mechanical strength and hence, helps reliable scaling process [10, 11]. 2-D analytical modeling for surface potential and threshold voltage of VSTB FET has also been developed [17]. But, an extensive study on vertical super-thin body (VSTB) FET performance in presence of various device constraints is needed to be developed to establish its reliability for circuit applications. For deep-submicron FETs, substantial increase in gate leakage current through thin SiO_2 gate dielectric layer is a serious concern [18, 19]. To solve this issue, replacement of SiO_2 gate dielectric by several high-k dielectrics such as Y_2O_3, Al_2O_3, La_2O_3, HfO_2, and their related compounds has been investigated [20, 21], out of which, Hf-based oxides have drawn most research attention as the interface quality of these oxides with bulk Si is better than any other high-k dielectric/Si interface [22–24]. However, it has been reported in many research papers that HfO_2/Si interface suffers from large number of trap charges [25–27]. Therefore, performance assessment of transistors with such oxide–semiconductor (HfO_2/Si) interface is needed to be investigated in terms of various trap distribution types and concentrations. Apart from that, MOS device operation is affected by various noise sources such as diffusion, generation–recombination/G–R, and flicker noise [28–31].

In this work, a simulation study on net noise (diffusion + generation–recombination + flicker) and RF performance of VSTB FET in presence of uniform and Gaussian trap distributions is reported. The basic physics working behind the degradation of device performance due to trap presence at the oxide–semiconductor (HfO_2/Si) interface is discussed. The dependency of individual noise power spectral density (PSD) on trap distribution types, trap concentrations, and operating frequency is also addressed here.

2 Device geometry and simulation strategy

Figure 1a depicts the complete 3-D view of VSTB FET and Fig. 1b shows 2-D cross-sectional view of the same. Different steps for fabrication method of such structure are also described [11]. The thin vertical body is supported by STI dielectric wall at one side. Arsenic (As) is used as the doping element in the source and drain regions and phosphorus (P) is used for doping in the body region. The doping concentrations used for various regions are: source: 10^{19} cm^{-3}, channel: 10^{15} cm^{-3}, drain: 10^{17} cm^{-3}, and substrate: 10^{15} cm^{-3}. To reduce leakage current (I_{off}), lower doping is used in the drain region as compared to the source region. However, on-current (I_{on}) degradation due to increased drain resistance in the lightly doped drain (LDD) is an issue. High-k dielectric

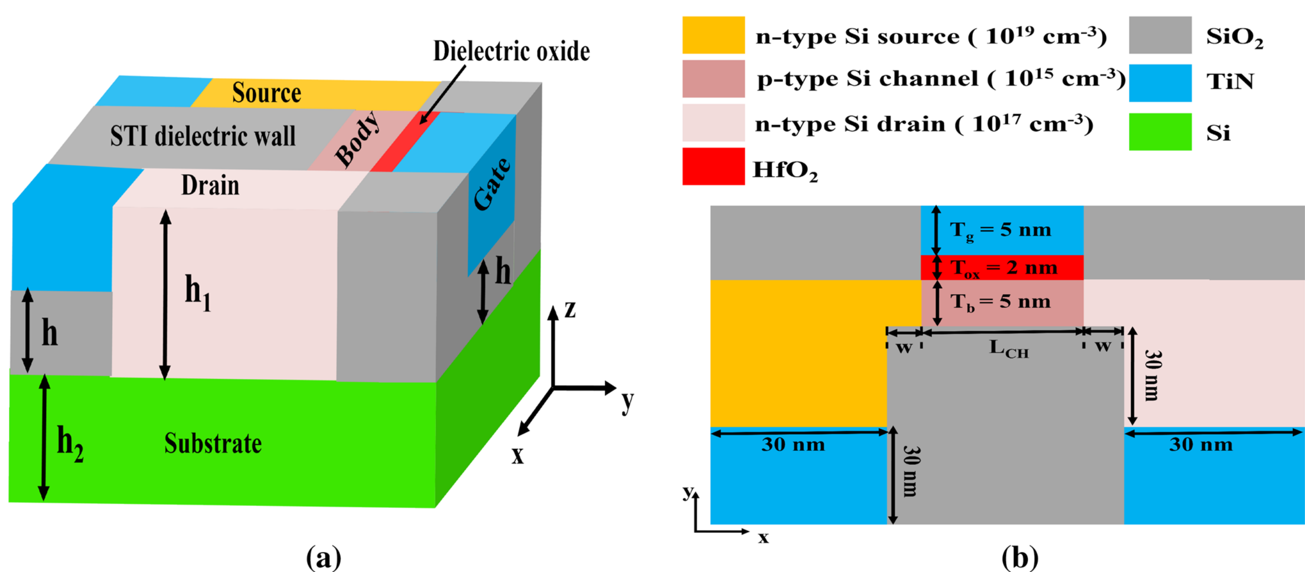

Fig. 1 Vertical super-thin body (VSTB) MOSFET **a** complete 3-D view, and **b** 2-D cross-sectional view across *XY* plane

oxide HfO_2 ($\varepsilon_r = 22$) and TiN (work function = 4.66 eV) are used as gate dielectric oxide and gate metal, respectively. Various device dimensions used are: channel length ($L_{CH} = 26$ nm), gate thickness ($T_g = 5$ nm), body thickness ($T_b = 5$ nm), and oxide thickness ($T_{ox} = 2$ nm). Equal source and drain extension length ($w = 4$ nm) are used. Height of body (h_1) and substrate (h_2) uses are 35 and 20 nm, respectively. Height of SiO_2 layer (h) placed between source/drain/gate contacts and substrate is 15 nm.

3-D and 2-D Sentaurus TCAD tool based on drift diffusion transport model [17, 32, 33] was used to perform the work. Initially, the input and output characteristics were studied using 3-D TCAD tool [32]. As the ITRS outlined all the desired values of various figures of merit (FoM) of future technology nodes in terms of per micrometer [34], we eventually focused on device cross-sectional performance in presence of traps and various noises. Therefore, device noise characteristics and RF performance were investigated by 2-D TCAD tool [32]. Relevant physics models were activated in the simulator to study various realistic phenomena effecting device electrical characteristics. Influence of high doping concentrations was taken care of by activating the Fermi–Dirac statistics and doping-dependent Shockley–Read–Hall (SRH) recombination model [32]. Bandgap narrowing was enabled to take care of highly doped source and drain regions [32]. Influence of device doping profile and high-k dielectric oxide on carrier mobility was accounted by enabling doping-dependent Masetti model and enhanced Lombardi model with high-k degradation, respectively [32]. Velocity saturation effect, which is a very common SCE for nanoscale device, was taken care of by triggering high-field saturation model [32]. Quantum density gradient model was also enabled to consider quantum correction effect [32]. Stress and strain may be induced in the thin vertical body by the thick STI dielectric wall. To acknowledge the stress effect, stress-induced electron mobility model and stress-dependent saturation velocity model were included [32, 35, 36]. Deformation potential model was activated to consider strain effect [32, 35, 36]. Device performance in n-type FET mainly gets degraded due to acceptor-like traps [37]. Regarding traps located at the insulator–semiconductor (HfO_2/Si) interface, two types of trap (acceptor-type) distribution were considered in this work: uniform and Gaussian [28, 32] as below:

$$d_{UNI} = N_0 \text{ for } E_0 - 0.5E_S < E < E_0 + 0.5E_S, \quad (1)$$

$$d_{GAU} = N_0 \exp(-(E - E_0)^2/2E_S^2). \quad (2)$$

Various parameters related to the above distribution functions are described in Table 1. Also, both the trap distributions over an energy range considered in this work are shown in Fig. 2 [28].

3 Results and discussion

The main objective of the work is to study device performance dependency on trap distribution type and concentration. In Sect. 3.1, input characteristics of FinFET and VSTB FET are compared. Also, a basic study on output characteristics of 3-D VSTB FET device is presented with the help of energy band diagram. Section 3.2 presents the transfer characteristics (I_D–V_{GS}) degradation in presence of various types of trap distributions and concentrations. Net noise parameters for the cumulative effect of three noise sources (diffusion + generation–recombination/G–R + flicker) at low and high frequencies ($f = 1$ MHz and $f = 10$ GHz) are also discussed. In Sect. 3.3, frequency and trap dependency of G–R and diffusion noise are addressed. Lastly, in Sect. 3.4, variation of RF FoM with respect to variation in trap concentration and distribution type is presented.

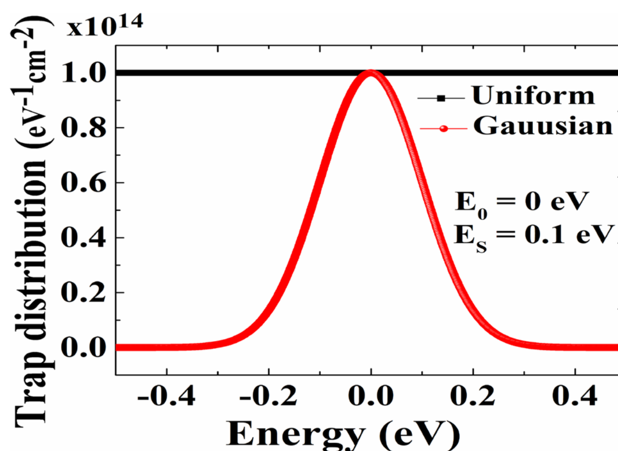

Fig. 2 Uniform and Gaussian trap distribution vs. energy [28]

Table 1 Various parameters of trap distribution

Symbol	Parameter	Value
N_0	Maximum concentration of traps in Gaussian distribution or trap concentration in uniform distribution	(10^{11}, 10^{12}, 10^{13}, 10^{14}) eV^{-1} cm^{-2}
E_0	EnergyMid in a Gaussian distribution	0 eV
ES	EnergySig in a Gaussian distribution	0.1 eV

3.1 Study of basic characteristics (input and output)

TCAD extracted 3-D simulated views of single gate FinFET, inner view of FinFET, and VSTB FET are shown in Fig. 3a–c, respectively. The simulation set up, various dimensional parameters, and materials used for FinFET is kept as the same (described in Sect. 2) as used for VSTB FET. The input characteristics (I_D–V_{GS}) of both the devices are compared in Fig. 3d, which demonstrates that VSTB FET exhibits much better off-current (I_{off}) and subthreshold swing (SS) as compared to the same-scale FinFET device. Such superiority in I_{off} and SS is found since, vertical STI dielectric wall in VSTB FET offers pseudo-SOI type of isolation between source and drain [11]. On the other hand, absence of such isolation in FinFET device increases I_{off} and thus, SS deteriorates significantly. Table 2 presents a comparative overview between various electrical parameters of FinFET and VSTB FET. Drain-induced barrier lowering

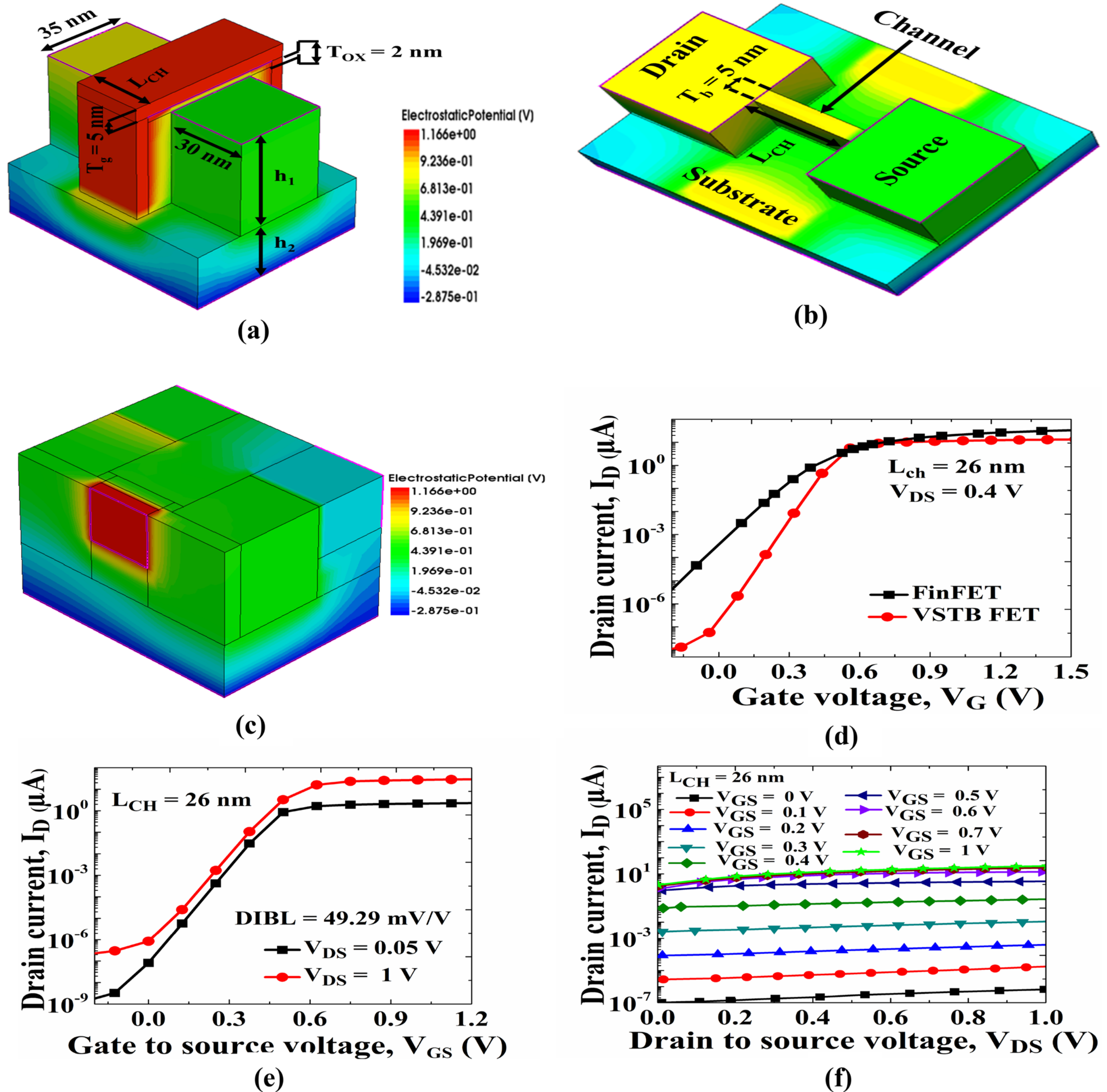

Fig. 3 TCAD extracted views of simulated 3-D devices **a** FinFET, **b** inner view of FinFET excluding gate and gate oxide, **c** VSTB FET; I_D–V_{GS} plots of **d** FinFET and VSTB FET, **e** FinFET for DIBL calculation, **f** I_D–V_{DS} plot of VSTB FET for different V_{GS} values

Table 2 Comparative performance analysis of FinFET and VSTB FET

Analysis	$*I_{off}$ (nA/μm)	I_{on}/I_{off}	SS (mV/dec)
FinFET	0.368	5.55×10^4	114.02
VSTB FET	0.00019	5.98×10^7	69.8

$*I_{off}$ and I_{on} is estimated at $V_{GS}=0$ V and $V_{GS}=1$ V, respectively

(DIBL) for VSTB FET is calculated from Fig. 3e using the relation [38]:

$$\mathrm{DIBL} = (V_{T,lin} - V_{T,sat})/(V_{DS_{sat}} - V_{DS_{lin}}), \tag{3}$$

where $V_{DS_{sat}} = 1$ V and $V_{DS_{lin}} = 0.05$ V. $V_{T,lin}$ and $V_{T,sat}$ are threshold voltages (estimated for a constant current of 10^{-7} A) at $V_{DS_{lin}}$ and $V_{DS_{sat}}$, respectively. The output characteristics (I_D–V_{DS}) of the device is depicted in Fig. 3f, which shows that the device works for low values of V_{DS} too. At $V_{DS}=0$, a little I_D flow is observed (Fig. 3f) and the reason for that has been explained later on.

Device energy band (E-band) diagrams corresponding to three different bias conditions: zero bias/equilibrium ($V_{GS}=0$, $V_{DS}=0$), bias 1 ($V_{GS}=0.8$, $V_{DS}=0$), and bias 2 ($V_{GS}=0.8$, $V_{DS}=0.4$), are shown in Fig. 4a–c, respectively, from which the internal physics working behind device electronics can be understood. Under equilibrium condition, source-to-channel transition barrier (Fig. 4a) is very high for which channel cannot form. Besides, level of conduction band (E_C) at drain side (64–94 nm) is higher than that of source side (0–30 nm) due to the doping nature of the device (source: 10^{19} cm^{-3}, drain: 10^{17} cm^{-3}). Thus, I_D is zero for zero bias condition. Under bias 1 ($V_{GS}=0.8$, $V_{DS}=0$), gate field reduces source to channel barrier height, which is also evident from Fig. 4b; thus source electrons move to channel region and form inversion layer. Another observation of Fig. 4b is that in the channel region (34–60 nm), conduction energy level (E_C) lies below the electron Fermi level (E_{fn}), which illustrates that the channel behaves as degenerate semiconductor. At such condition, although $V_{DS}=0$, gate fringing fields contribute a little amount of lateral fields which lead to weak movement of the channel electrons to the drain [39]. Thus, at $V_{DS}=0$ too, a negligible flow of I_D is observed (Fig. 3f), which increases with the increase in V_{GS}. In Fig. 4c, under bias 2 ($V_{GS}=0.8$, $V_{DS}=0.4$) E_C at the drain side goes down that of source and channel region; thus channel electrons can easily move to the drain and contribute to significant I_D flow. Here also, channel behaves as degenerate semiconductor.

3.2 Study of device characteristics in presence of traps and corresponding net noise performance

This section presents device performance in presence of various trap distributions and the net noise (diffusion + G–R + flicker) characteristics. From Fig. 5a, b, which depict I_D–V_{GS} plot for uniform trap (UT) and Gaussian trap (GT) distributions, respectively, it is clear that with increasing trap concentration (TC) for both the distributions (UT and GT), the transfer characteristics deteriorate from their ideal nature (under no trap condition). Traps present in the semiconductor-insulator surface create extra energy states, which randomly capture and later release carriers moving through the channel and thus, alter E-band diagram of the device. Figure 5c, d represent, respectively, E-band diagrams for UT and GT distribution. For both the distributions, at the channel region (34–60 nm) E_C goes up of E_{fn}, which illustrates the fact that interface trap reduces carrier density at the channel region. Thus, at a fixed value of V_{GS}, number of channel charges decreases more and more with increasing

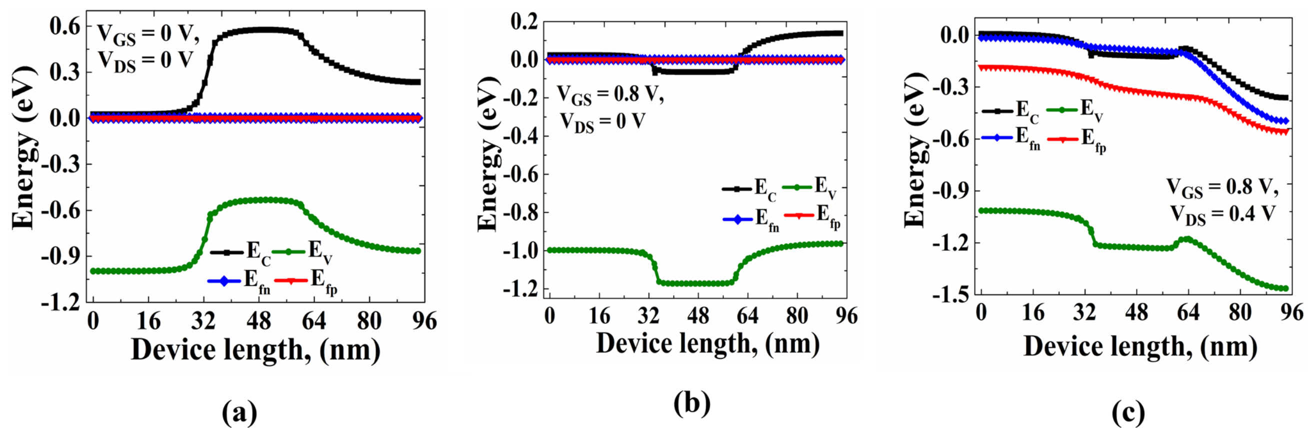

Fig. 4 Energy vs. device length for **a** zero bias/equilibrium ($V_{GS}=0$, $V_{DS}=0$), **b** bias 1 ($V_{GS}=0.8$, $V_{DS}=0$), and **c** bias 2 ($V_{GS}=0.8$, $V_{DS}=0.4$)

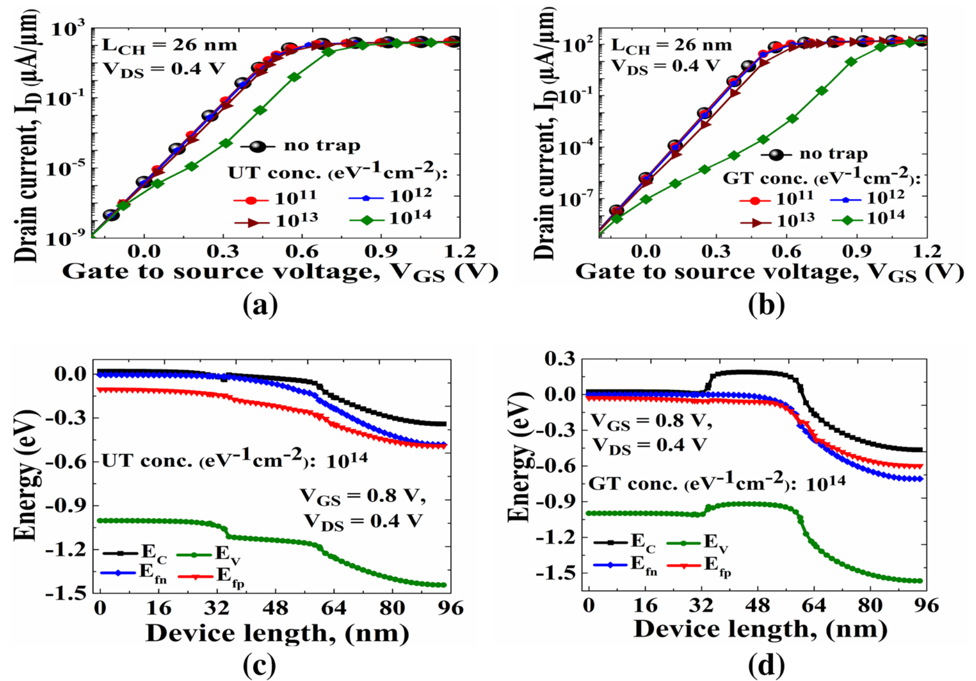

Fig. 5 I_D–V_{GS} plot variations for **a** uniform trap (UT) distribution, and **b** Gaussian trap (GT) distribution; energy vs. device length for **c** UT distribution, **d** GT distribution

TC and hence, I_D degrades (Fig. 5a, b). For a particular trap concentration, degradation of I_D is more severe in case of GT (Fig. 5b). This happens due to non-uniform distribution of Gaussian traps. Although, degradation in I_D for any type of trap (UT/GT) is negligible for lower TC [(10^{11}–10^{13}) eV^{-1} cm^{-2}], effect of the traps on I_D becomes prominent for TC = 10^{14} eV^{-1} cm^{-2} (Fig. 5a, b).

For ideal condition (no trap), the estimated value of cross-sectional I_D is 114.562 μA/μm at V_{GS} = 0.65 V and 127.18 μA/μm at V_{GS} = 0.7 V. In this section, at V_{DS} = 0.4 V, I_{on} is calculated as I_D at V_{GS} = 0.65 V (V_{GS} = 0.7 V) for UT (GT) distribution. For such estimated I_{on}, in ideal condition (no trap), value of I_{on}/I_{off} is 0.73×10^8 for UT and 0.81×10^8 for GT. The values of I_{off} (at V_{GS} = 0 V and V_{DS} = 0.4 V) and SS under no trap condition are 1.56477 pA/μm and 66.17 mV/dec, respectively. Variations of I_{off}, I_{on}, I_{on}/I_{off}, and SS with respect to trap distribution type and TC are shown in Fig. 6a–h. Figure 6a, c, e, g corresponds to UT and Fig. 6b, d, f, h corresponds to GT. Both, I_{off} (Fig. 6a, b) and I_{on} (Fig. 6c, d), decrease for the presence of UT/GT traps. However, since, decrease in I_{off} is relatively higher than decrease in I_{on}, I_{on}/I_{off} (Fig. 6e–f) shows improvement for increasing TC (UT/GT) except for the case of GT of TC = 10^{14} eV^{-1} cm^{-2} (Fig. 6f). For GT with such high TC (10^{14} eV^{-1} cm^{-2}), I_{on} reduces drastically (Fig. 6d), which leads to fall of I_{on}/I_{off}. On the other hand, to attain any particular value of I_D, since, device with interface traps needs more V_{GS} than any ideal device (with ideal interface), deterioration in SS increases with increasing TC (Fig. 6g, h). Percentage changes in I_{on}/I_{off} and SS in trap-affected device with respect to ideal condition (no trap) is presented in Table 3.

Figure 7a, b represents gate voltage electron noise spectral density (S_{vg}ee) as a function of V_{GS} for UT and GT, respectively. Electron density across the channel length for maximum GT concentration of 10^{14} eV^{-1} cm^{-2} at two frequencies is shown in Fig. 7c. Plots of drain current noise spectral density (S_{id}) vs. V_{GS} for UT and GT are shown in Fig. 7d, e, respectively. From Fig. 7a, b, d, e, it is clear that at a fixed V_{GS} value, PSDs of both types of noise (S_{vg}ee and S_{id}) fall by a large order for high frequency (f = 10 GHz), as the charge trapping probability also reduces at higher frequencies [40]. This property helps the device to work efficiently at higher frequencies.

At f = 1 MHz, under no trap condition and for both the trap distributions (Fig. 7a, b), S_{vg}ee plots, following several spikes, gradually decrease with increase in V_{GS}. Such nature of plot can be explained by the carrier concentration variation in the channel for varying V_{GS} values. At lower V_{GS}, channel consists of very low concentration of charges. In such a state, random capturing and releasing of charges by the traps lead to large variation in the number and velocity of channel charges, which eventually reflect on S_{vg}ee values. At higher V_{GS}, inversion layer is formed and channel charge concentration becomes very high. Therefore, any type of variation in charge concentration due to traps is now weakly felt by the high concentrated channel charges, and hence, S_{vg}ee decreases for higher V_{GS}.

However, at f = 10 GHz, for lower values of V_{GS} (Fig. 7a, b), S_{vg}ee initially increases and then slowly gets saturated at higher V_{GS}. For the same V_{GS} value, charge density developed across the channel at high frequency is lower than that of low frequency (Fig. 7c). As such, at lower V_{GS}, very less

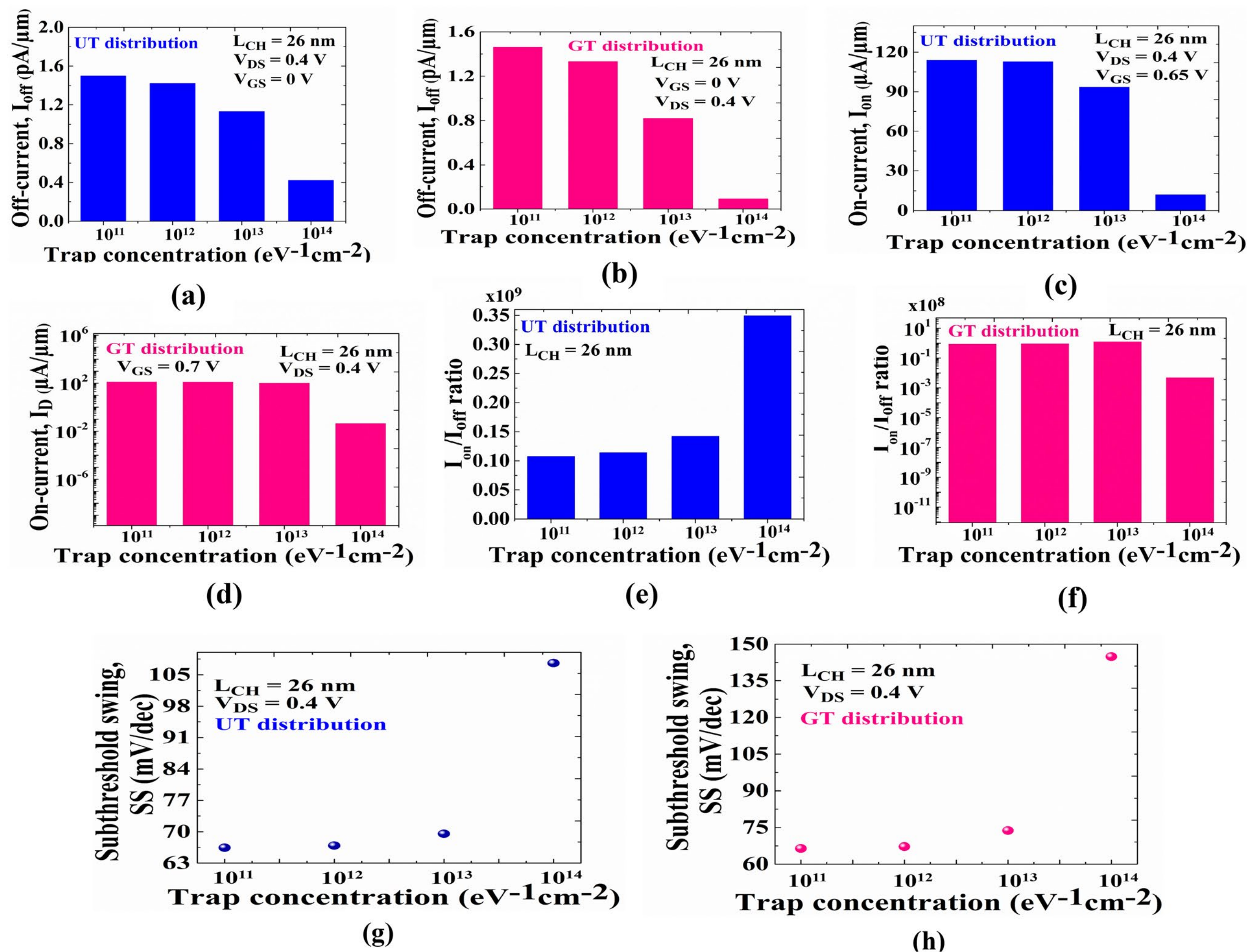

Fig. 6 Different parameters as a function of trap distribution types and concentration **a** I_{off} for UT, **b** I_{off} for GT, **c** I_{on} for UT, **d** I_{on} for GT, **e** I_{on}/I_{off} for UT, **f** I_{on}/I_{off} for GT, **g** SS for UT, and **h** SS for GT

Table 3 Device performance deviation for different types of trap distribution and concentration

Parameters	UT with TC (eV^{-1} cm^{-2})				GT with TC (eV^{-1} cm^{-2})			
	10^{11}	10^{12}	10^{13}	10^{14}	10^{11}	10^{12}	10^{13}	10^{14}
% change in I_{on}/I_{off}	46.76	55.43	93.91	377.21	5.76	13.11	49.8	−99.41
% change in SS	0.41	1.12	5.1	62.62	0.42	1.54	11.41	118.94

number of charges exist in the channel and hence, probability of charge trapping also becomes low at high frequency. But, beyond a critical value of V_{GS} charge concentration in the channel increases, and due to this, charge trapping probability becomes high; thereby, S_{vg}ee also starts to increase (for $V_{GS} > 0.15$ V in Fig. 7a, b). However, for very high V_{GS} (> 0.75 V in Fig. 7a, b), S_{vg}ee gets saturated due to the same reason explained for reduction in S_{vg}ee at $f = 1$ MHz for high V_{GS}. Another observation of Fig. 7a, b is that the net value of S_{vg}ee at any particular frequency increases with increasing trap (UT/GT) concentration. This happens due to the greater charge-trapping probability with higher TC. Also, compared to UT distribution, GT distribution contributes to higher S_{vg}ee.

S_{id} variations with respect to change in V_{GS} follow such pattern (Fig. 7d, e), which increases initially for lower V_{GS}, but gets saturated for $V_{GS} > 0.6$ V, as I_D also saturates at higher V_{GS}. Also, PSD of S_{id} is lesser at $f = 10$ GHz due to reduction in the charge trapping probability at high frequency [40]. It is observed that for TC of the order of 10^{14} eV^{-1} cm^{-2}, S_{id} pattern deteriorates to a large extent from its linear characteristics at lower V_{GS}. Also, GT distribution

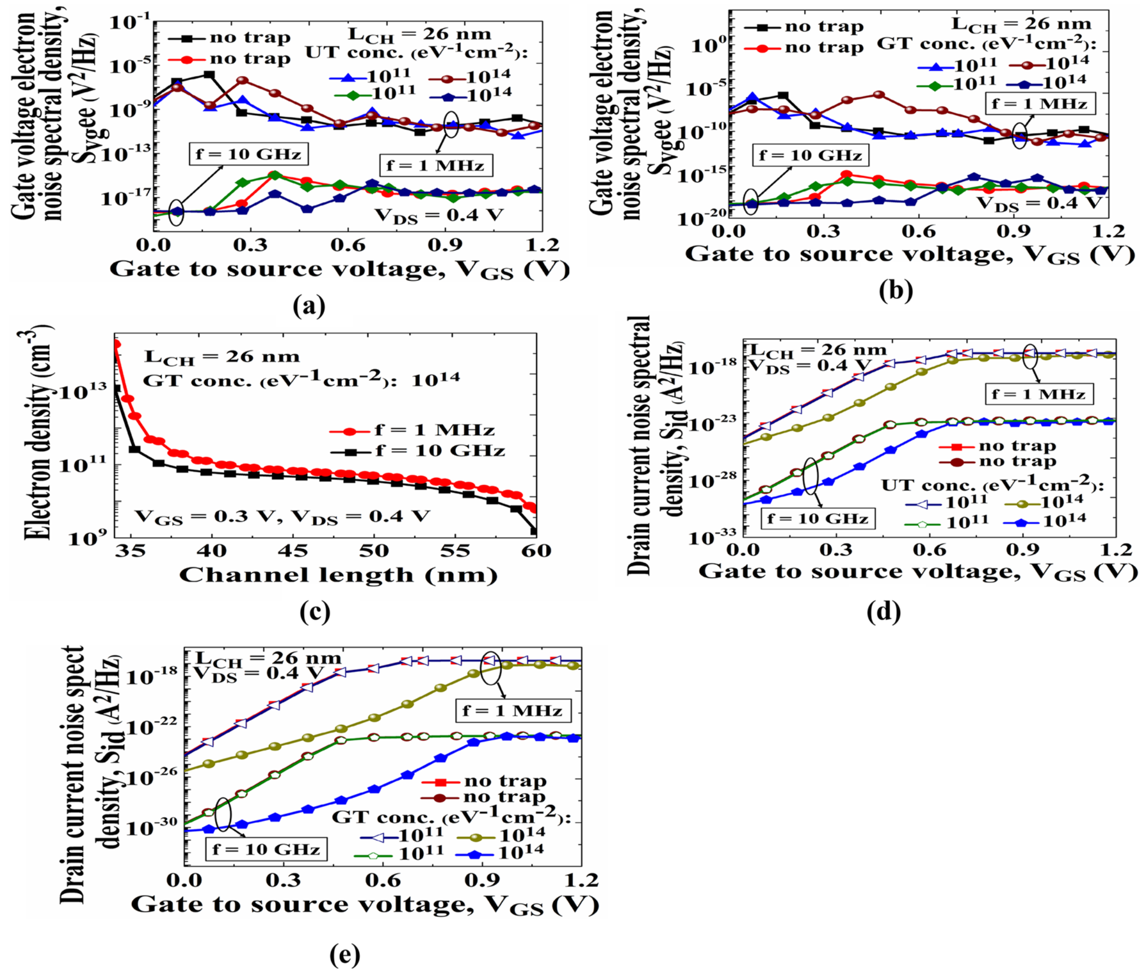

Fig. 7 Net noise (diffusion + G–R + flicker) PSDs: gate voltage electron noise spectral density (S_{vg}ee) for **a** uniform trap (UT), and **b** Gaussian trap (GT); **c** electron density across the channel length (L_{CH}); drain current noise spectral density (S_{id}) for **d** uniform trap (UT), and **e** Gaussian trap (GT)

(Fig. 7e) has more significant effect on S_{id} compared to UT distribution (Fig. 7d).

3.3 Individual noise (G–R and diffusion) performance

It is observed that at low and high frequencies, the net noise (diffusion + G–R + flicker) characteristics of the device are dominated by generation–recombination (G–R) noise and diffusion noise, respectively [28]. Flicker noise, the origin of which is the conductance fluctuation of charge carriers moving through a channel affected by contaminants, is much prominent at lower frequencies and decreases significantly with increase in frequency [29, 30]. As the primary focus is on high frequency, flicker noise effect can be ignored for advanced devices. In this section, we perform a study on G–R and diffusion noise nature of the device. We have considered only Gaussian trap (GT) distribution, as with this type of distribution device performance gets more affected, which have already been seen in Sect. 3.2. Figure 8a, b shows S_{vg}ee vs. V_{GS} plots for G–R noise at $f = 1$ and 10 GHz, respectively. Same type of plots for diffusion noise are shown in Fig. 8c ($f = 1$ MHz) and (d) ($f = 10$ GHz).

Comparing Fig. 8a, c, it is clear that for any given value of V_{GS} in the case of G–R noise, the PSD of S_{vg}ee is much higher at $f = 1$ MHz than that of diffusion noise. At low frequency, the fluctuation in concentration and velocity of the carriers is mainly caused by Shockley–Read–Hall (SRH) and defect centres associated with the channel [31] and hence, S_{vg}ee for G–R noise becomes high. Also, PSD of S_{vg}ee increases for higher trap concentration (Fig. 8a). Again, at $f = 1$ MHz for a given value of V_{GS} comparing Figs. 7b and 8a (Sect. 3.2), it can be seen that the net S_{vg}ee curves (Fig. 7b of Sect. 3.2) for different trap concentrations are also following almost the same pattern of S_{vg}ee corresponding to G–R noise only (Fig. 8a). At $f = 10$ GHz, for all values of V_{GS},

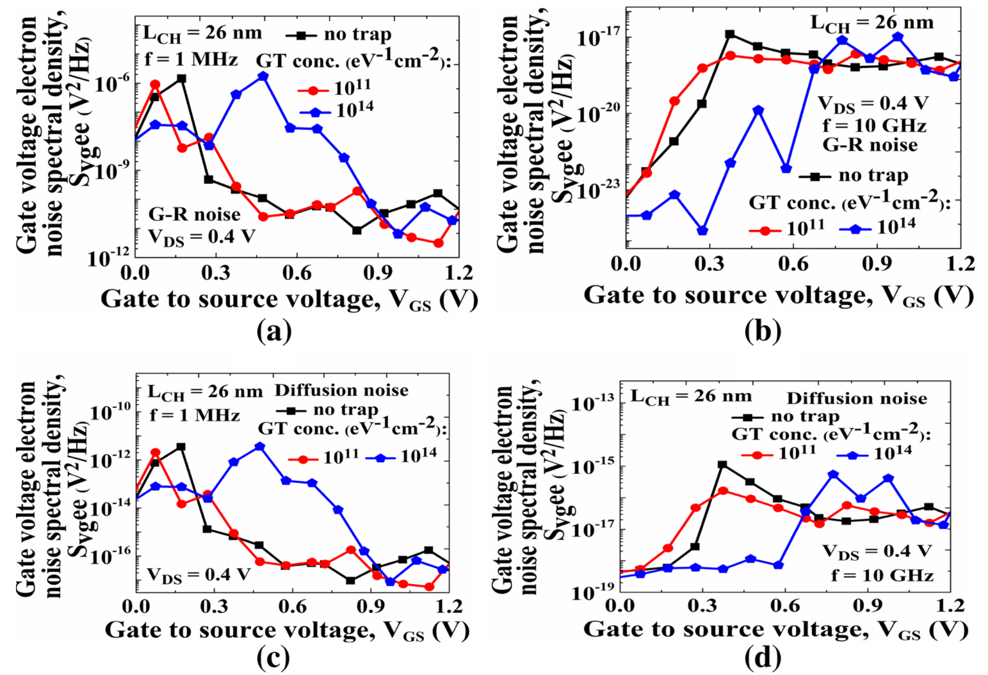

Fig. 8 Gate voltage electron noise spectral density ($S_{vg}ee$) for Gaussian trap (GT) distribution **a** G–R noise at $f = 1$ MHz, **b** G–R noise at $f = 10$ GHz, **c** diffusion noise at $f = 1$ MHz, and **d** diffusion noise at $f = 10$ GHz

amplitude of $S_{vg}ee$ exhibits higher values in case of diffusion noise (Fig. 8d) than that of G–R noise (Fig. 8b). At high frequency, probability of charge trapping and de-trapping by recombination centres is reduced. For fast variation of V_{GS}, channel charges undergo a diffusion mechanism, the rate of which is a strong function of V_{GS}. Thus, if V_{GS} varies very fast, the average diffusion rate of carriers also changes significantly with time, leading to a prominent diffusion noise at high frequency. Irrespective of V_{GS} values, the net noise PSDs ($S_{vg}ee$ in Fig. 7b of Sect. 3.2) at $f = 10$ GHz are comparable to diffusion noise $S_{vg}ee$ curves (Fig. 8d).

3.4 Device RF performance in presence of traps

The RF performance is studied under three cases: no trap (NT), uniform trap (UT), and Gaussian trap (GT). Figure 9a–f correspond to various RF parameters like transconductance (g_m) at $f = 10$ GHz, total input capacitance (C_{gg}) at $f = 10$ GHz, total input capacitance (C_{gg}) at $f = 1$ kHz, gate-drain capacitance (C_{gd}) at $f = 10$ GHz, unit-gain cutoff frequency (f_T) at $f = 10$ GHz, and gain–bandwidth-product (GBP) at $f = 10$ GHz as a function of V_{GS}, respectively. The variations shown are for trap concentration of 10^{14} eV^{-1} cm^{-2}.

It can be seen from Fig. 9a that as V_{GS} starts to increase, g_m rises sharply at three different V_{GS} values for three different cases (NT, UT, and GT). The point of V_{GS}, at which g_m rise occurs, shifts towards right as we go from NT to UT to GT. Generally, for a fixed value of V_{DS}, when V_{GS} is applied, rise in I_D occurs at the lowest V_{GS} under NT condition. But, presence of traps hinders the normal I_D rise nature by participating in channel transport mechanism. At such condition, effective channel charge becomes a function of interface traps and mostly reduces. Therefore, both I_D and g_m fall. This is the reason behind the right shifting of g_m rise point across V_{GS} axis. As the effect of GT is more prominent than that of NT and UT distribution, g_m rise requires larger V_{GS} in case of GT as compared to the other two cases. From Fig. 9b, it is clear that at $f = 10$ GHz for a given amplitude of V_{GS} as we go from NT to UT to GT, the value of C_{gg} follows a descending order. Also, distortion/stretch out in capacitance–voltage (C–V) plot (Fig. 9b) is not observed. The reason of such nature of C–V plot is as follows: at high-frequency ($f = 10$ GHz) interface traps, which have longer charging/discharging time constant compared to time-period of applied high-frequency gate bias, cannot response as fast as applied gate field; thus the distortion/irregularity in charge distribution caused by interfacial traps becomes minimal at high frequency. However, at low frequency ($f = 1$ kHz), interfacial traps actively participate in channel charge distribution and thus randomness/distortion is added to the C–V plot, which is also observable in Fig. 9c. The peak value of C_{gd} (Fig. 9d) is seen to follow an ascending order going from NT to UT to GT. The unit-gain cutoff frequency (f_T) and GBP are calculated from the relations [28, 41, 42]:

$$f_T = g_m / 2\pi C_{gg}, \tag{3}$$

$$\mathrm{GBP} = g_m / 20\pi C_{gd}, \tag{4}$$

f_T and GBP (Fig. 9e, f) attain peak values at smaller V_{GS} under NT condition. But, introduction of traps degrades f_T

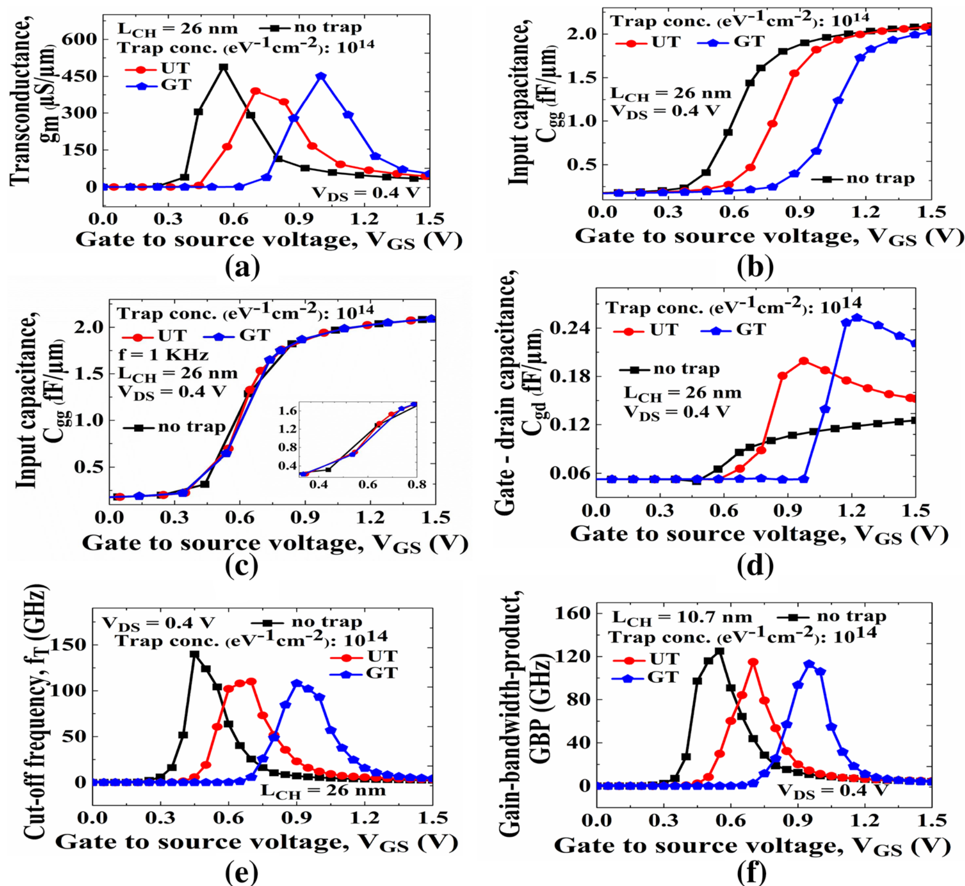

Fig. 9 RF figures of merit (FoM) as a function V_{GS} and trap nature **a** transconductance (g_m), **b** input capacitance (C_{gg}) in $f = 10$ GHz, **c** input capacitance C_{gg} in $f = 1$ kHz, **d** gate-drain capacitance (C_{gd}), **e** unit-gain cutoff frequency (f_T), and **f** gain–bandwidth-product (GBP)

and GBP at lower V_{GS} by suppressing g_m (Fig. 9a). All the values of different RF FoM: peak transconductance (g_{mp}), peak input capacitance (C_{ggp}), peak gate-drain capacitance (C_{gdp}), maximum cutoff frequency (f_{Tmax}), and maximum gain–bandwidth product (GBP_{max}) for the three cases (NT, UT, and GT) are listed in Table 4, from which it can be concluded that VSTB FET is suitable for high-frequency operations.

4 Conclusion

In this work, the effect of various interfacial trap (HfO_2/Si) distributions on VSTB FET performance is presented. It is observed that the Gaussian trap (GT) distribution disturbs fundamental parameters such as I_{on}, I_{on}/I_{off}, and SS significantly. Irrespective of trap distribution types (UT/GT), for trap concentration < 10^{14} eV^{-1} cm^{-2} device performance shows negligible deterioration. The change in energy band diagram for a particular bias condition in presence of interfacial traps (UT or GT) is also discussed. A qualitative analysis of net noise (diffusion + G–R + flicker) and individual noise PSD dependency on trap distribution type and concentration is also reported. It is observed that for lower values of V_{GS} too, the values for unity-gain cutoff frequency (f_T) and gain–bandwidth-product (GBP) of the device are in gigahertz (GHz) range; this property helps the device to work efficiently in low-power high-speed circuits.

Table 4 RF FoM for various trap distributions

Cases	g_{mp} (µS/µm)	C_{ggp} (fF/µm)	C_{gdp} (fF/µm)	f_{Tmax} (GHz)	GBP_{max} (GHz)
NT	454.09 (at V_{GS} = 0.57 V)	1.97 (at V_{GS} = 0.9 V)	0.094 (at V_{GS} = 0.75 V)	140 (at V_{GS} = 0.45 V)	125 (at V_{GS} = 0.55 V)
UT	390.53 (at V_{GS} = 0.7 V)	1.94 (at V_{GS} = 1.1 V)	0.19 (at V_{GS} = 0.98 V)	110 (at V_{GS} = 0.7 V)	115 (at V_{GS} = 0.7 V)
GT	450.68 (at V_{GS} = 1 V)	1.9 (at V_{GS} = 1.3 V)	0.25 (at V_{GS} = 1.23 V)	108 (at V_{GS} = 0.9 V)	113 (at V_{GS} = 0.95 V)

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