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RF analysis and temperature characterization of pocket doped L-shaped gate tunnel FET

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Abstract

This work exclusively illustrates the impact of low-k gate oxide material on the ambipolarity of SOI-DG TFET proposed previously in literature (Goswami and Bhowmick in Silicon, https://doi.org/10.1007/s12633-019-00169-7, 2019) with a comparative AC analysis of the two TFET architectures presented here. Based upon the primary DC characterisation of the proposed device, a thorough analysis of ambipolarity, impact of varying mole fraction, influence of temperature on device characteristics are performed explicitly. For the complete RF characterisation, the transconductance, cut-off frequency, transit time, power delay product, transconductance generation efficiency and parasitic capacitances are presented in detail with a comparative summarization. The reasonably high on-current of the proposed device (orders of mA/μm) with very low leakage current floor (orders of fA/μm) makes the device suitable for low power applications as well as for high fan-out operations. The seemingly low threshold voltage with notably low V_{DD} values (0.3 V) aids to substantial reduction of dynamic power consumption. The high cut off frequency (best reported in tera hertz) of the device opens the window for numerous diversified applications.

1 Introduction

The tunnel field-effect transistor (TFET) has emerged as a future transistor option due to its steep-slope demonstrations and the resulting advantages, i.e. operating at low supply voltage (V_{DD}). Reducing V_{DD} while leakage current being low is essential for minimization of energy consumption and enhancing battery life of the mobile device. The thermal limit of MOSFET sub-threshold swing (SS), set by kT/q restricts the lowering of threshold voltage (V_t) which causes significant performance degradation at low V_{DD} [2–5]. The rigorous scaling of MOSFET size in recent years has caused high sub-threshold swing, leakage current (I_{off}) and short channel effect [6]. TFETs do not suffer much from short channel effect and it exhibits small sub-threshold swing with low off- current. In double gate TFET the on-current is larger than its single gate counterpart due to the simultaneous onset of two tunneling paths [7].

The ultra-low power application demands high on-state current to increase the fan out and low off-state current simultaneously to decrease the standby power consumption. At one fell swoop, extremely low sub-threshold swing is desired for an aggressive supply voltage scaling. The doping fluctuation effects come into picture with high doping concentration and quantum confinement effects arise when dealt with nanoscale devices. It has been reported that the dominant leakage mechanism varies depending on the body design parameter values. Moderate body doping (10E18 cm^{-3}) is advantageous for suppressing I_{off} and maximizing I_{on} [8, 9]. Additionally, the gate and $n+$ pocket overlap results in a boosted electric field, and thereby the ON-state current and hence the overall performance of the TFET is enhanced [10].

When a tunneling dominated device is operated in low temperature, it shows a slightly temperature-dependent SS characteristic [11]. With proper EOT scaling, i.e. using a thin high-k dielectric layer, the TFET performance can be improved due to better capacitive coupling. In hetero structure, such as the $Si_{1-x}Ge_x$ source TFETs as investigated in [12, 13], the overlap between the Si channel and the Silicon

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Germanium source increases the tunneling area since the lateral as well as the vertical tunneling transpires simultaneously and thus increases the current. Amongst the different types of proposed SOI devices, the multigate field effect transistor (multigate FET) clearly stands out. Colinge [14] pronounces the reasons for evolving from single-gate to multi-gate device structures. It also mentions some of the challenging issues in ultra-small devices such as doping fluctuation effects and quantum confinement effect as already reported.

The ambipolarity in the TFETs has been a major challenge which limits its utility in complementary circuits and challenges its applicability in compatible CMOS technology [15–17]. Different literatures have proposed the means to address the ambipolarity issues which will be discussed in the subsequent sections in brief. The RF characterisation is also important to make a thorough investigation of any device since it hints the operating frequency, time delay and analog circuit compatibility of the device. The dominance of C_{gd} over the total gate capacitance has already been reported by Goswami [18] where he has demonstrated the influence of various types of noise like generation–recombination noise, flicker noise, diffusion noise in reference to operating frequency.

This paper comprises of five sections starting from introduction in Sect. 1. Section 2 demonstrates the proposed device geometry and operating principle of the device. Section 3 elaborates the simulation environment. The subsections of Sect. 4 depict the detailed investigation of the simulation results comprising of DC analysis and the RF characterisation of the device. Finally Sect. 5 gives the conclusion of our work.

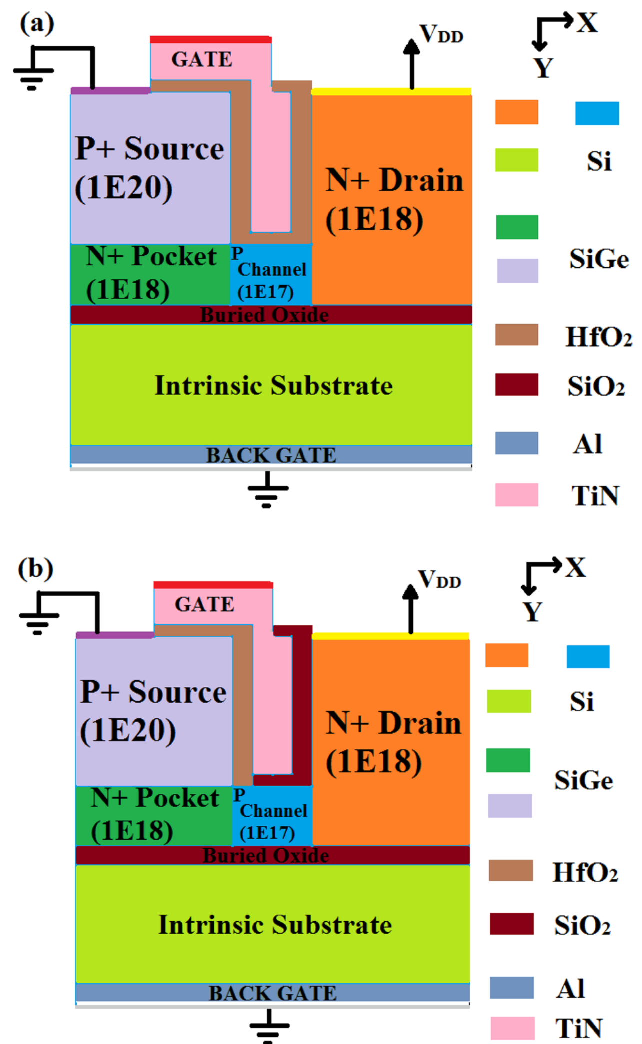

Fig. 1 Proposed device **a** structure 1, **b** structure 2

2 Device architecture and working principle

The TCAD- generated 2D structure of the proposed SOI DG-TFET is depicted in Fig. 1 in compliance with the structure presented in [1]. The detailed investigation of device architecture is represented in Table 1. Here the only difference is observed in gate oxide materials of both the proposed structures. Structure 1 is having only high-k gate oxide whereas the structure 2 presented here (Fig. 1b) employs a combination of both high-k and low-k gate oxide materials. The low-k gate oxide is incorporated towards the drain side of the gate so as to improve the ambipolar nature of TFET. The terminal bias characteristics are exemplified in the figure itself where we can see that the drain is connected to V_{DD} of 0.3 V. The source terminal and back gate are grounded. Front gate bias is varied from negative to positive potential and the transfer characteristics are observed in the subsequent sections.

The conduction mechanism in the proposed device is band-to-band tunneling, BTBT which arises out of the potential modulation by the applied gate field resulting in band bending at the source-channel tunnel junction. When the tunnelling path length, λ is narrowed by the gate bias, electrons from the valence band of the source gets a shorter path to tunnel to the conduction band of the channel. The tunneling probability defined by WKB approximation can be expressed as Equation 1

$$T(E) = \exp\left(-\frac{4\lambda\sqrt{2m^{*}}E_{g}^{3/2}}{3\hbar\left(E_{g}+\Delta\Phi\right)}\right), \quad (1)$$

In this equation E_g is the energy band gap, $\hbar$ is the reduced Plank's constant, m^* is the effective mass of electron, and $\Delta\Phi$ is the band offset, i.e. the energy difference between

Table 1 Device parameters used in the simulation

Parameter	Proposed device 1	Proposed device 2
Source dimension	40 nm × 40 nm	40 nm × 40 nm
Doping	1E20 cm^{-3}	1E20 cm^{-3}
Drain dimension	55 nm × 40 nm	55 nm × 40 nm
Doping	1E18 cm^{-3}	1E18 cm^{-3}
Channel dimension	20 nm × 15 nm	20 nm × 15 nm
Doping	1E17 cm^{-3}	1E17 cm^{-3}
Substrate dimension	100 nm × 30 nm	100 nm × 30 nm
Box dimension	100 nm × 5 nm	100 nm × 5 nm
Pocket dimension	40 nm × 15 nm	40 nm × 15 nm
Doping	1E18 cm^{-3}	1E18 cm^{-3}
Gate dimension	30 nm × 10 nm (horizontal) 35 nm × 10 nm (vertical)	30 nm × 10 nm (horizontal) 35 nm × 10 nm (vertical)
Back gate dimension	100 nm × 5 nm	100 nm × 5 nm
Gate oxide thickness	3 nm	3 nm

valence band of source and conduction band of channel. Similarly, in uniform electric field limit, the Kane's model determines the BTBT generation rate G per unit volume given by the following equation

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right), \quad (2)$$

here $F_0 = 1$ V/cm; P is a user defined parameter specifically 2 and 2.5 for the direct and indirect BTBT, respectively; A and B are the Kane parameters; and F is the electric field. Again, TFET shows V_{GS} -dependent SS behaviour implying that the sub-threshold swing changes with the applied gate bias. This enables faster switching operation of TFETs compared to that of the MOSFETs. The SS may be expressed by the following equation

$$\mathrm{SS} \equiv \frac{\delta V_g}{\delta(\log I_d)} = \frac{\delta V_g}{\delta \psi_s} \frac{\delta \psi_s}{\delta(\log I_d)}, \quad (3)$$

In the above equation V_g is the gate voltage, I_d is the drain current, and ψ_s is the surface potential. The first term denotes the gate governance to the channel whereas the second term represents the current flow mechanism.

3 Simulation models

The simulation of the proposed TFETs has been accomplished using Sentaurus TCAD, a commercially accessible computer-aided design tool from Synopsys [19]. Fermi–Dirac Statistics has been employed instead of Boltzmann Statistics with 'doping dependent mobility' model to account for high doping concentration so that the effect of doping concentration on carrier mobility is taken into account. From Eq. 1 it is found that the tunneling probability is a function of the bandgap at the tunnel junction in TFETs, hence the bandgap narrowing model has been activated such that the modulation of energy bands is properly handled [19]. Shockley–Read–Hall (SRH) recombination model has been used in the simulation. To handle the inter-band tunneling more efficiently, band-to-band tunneling model is employed. To analyse the effects of temperature variation the advanced hydrodynamic model is activated so that influences of impact ionization are addressed properly in the device.

4 Results and discussion

This work has been an extension of our previously published work [1] where the primary investigation of the proposed TFET structure (Fig. 1a) had been done which comprises the impact of scaling on electrical parameters, influence of back gate bias, observation of DIBL effect, detailed analysis of channel length modulation, etc. In this paper we are going to discuss some of the major performance issues of TFET like ambipolarity, temperature analysis, and RF characterization taking into account the different capacitances like C_{gd}, C_{gs} and C_{gg}, transconductance, cut off frequency, time delay, and transconductance generation efficiency in the subsections followed.

4.1 Mole fraction variation

Here the results of varying $Si_{1-x}Ge_x$ mole fraction with varying values of 'x' are illustrated. As the Ge mole fraction increases in the source region the on- state current is expected to increase as per the observations presented in literature [20].This may be attributed to the fact that when $Si_{1-x}Ge_x$ is converted to only Ge ($x = 1$), the energy band gap is decreased and hence it leads to more band- to- band

generation thereby the increased on-current. The reduction of energy band gap can be verified by Fig. 2 where the pointed arrow shows the direction of bandgap narrowing with increasing 'x'. Again the proximity of tunneling width is shown by the circle (red colour).The impact of varying mole fraction in the proposed device is investigated with the help of the transfer characteristics plotted in Fig. 3. It is observed that with increasing 'x', i.e. increasing the percentage of Ge in $Si_{1-x}Ge_x$, the on-current is seen to be decreased which has been a contradictory result. This may be attributed to the limitation of WKB approximation of tunneling probability in indirect bandgap material like Si, Ge and SiGe as reported earlier in literature [21]. Again the energy Fermi level is investigated in the on-state of the device for varying mole fraction and it can be observed from Fig. 4 that as Ge mole fraction increases, the Fermi level moves down in the energy scale as marked by the arrow. When Fermi level is high at the source and channel end of the device, the probability of the occupancy of electrons is more than that of the reverse case. Hence the charge carriers are more likely to tunnel from source to channel and then the flow from channel to drain, thereby aiding to on-state current. This can be verified by the contour plot of electron concentration in the source and channel region as depicted in Fig. 5. It is known that the quasi Fermi level of electrons is directly proportional to the density of charge carriers, thereby leading to the observed variation here.

But the off-state leakage current is observed to be very high in case of all Si structure as evident from Table 2. Another interesting characteristic observed is that the threshold voltage, calculated at a drain current level of 100 nA/μm are seen to be negative for 'x' fraction 0. This may lead to very high static power consumption and can cause detrimental effect in the circuit performance by heating. To eliminate this effect, work function adjustment is needed to be carried out for the front gate since previously the metal

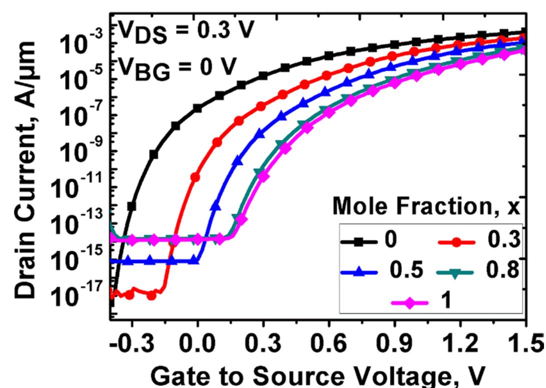

Fig. 3 Transfer characteristics for varying mole fraction in proposed structure 2

work function was attuned to get the highest on–off ratio in case of mole fraction of 0.5 each in SiGe.

4.2 Impact of temperature on device characteristics

Literature reports that TFET shows stability against the temperature variation as compared to MOSFETs due to its novel conduction mechanism, i.e. band-to-band tunneling (BTBT) from valence band of source to conduction band of channel which has been the major carrier injection mechanism in TFETs rather than the thermionic emission in MOSFETs [22–24]. Since both the source-channel and drain channel junctions are reverse biased, with increasing temperature, impact ionization comes into picture. To consider the effect of the same, advanced hydrodynamic model is incorporated in the simulation as suggested by [19]. The BTBT depends mainly upon the tunneling barrier width as evident from Eq. 1, which is independent of temperature and hence it shows better immunity towards temperature variation in the

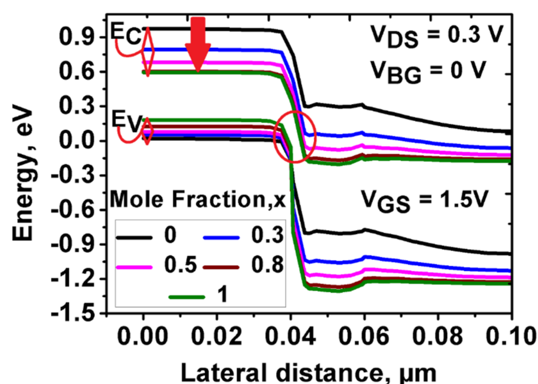

Fig. 2 ON state band diagram for varying mole fraction for proposed structure 2 taking lateral cut line at gate oxide–channel interface

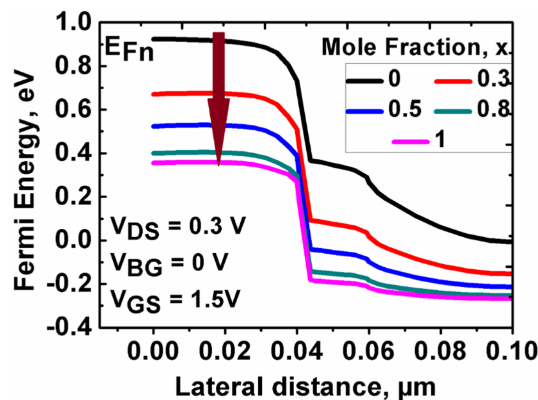

Fig. 4 Energy Fermi level for varying mole fraction in proposed structure 2 taking cut line at gate oxide–channel interface

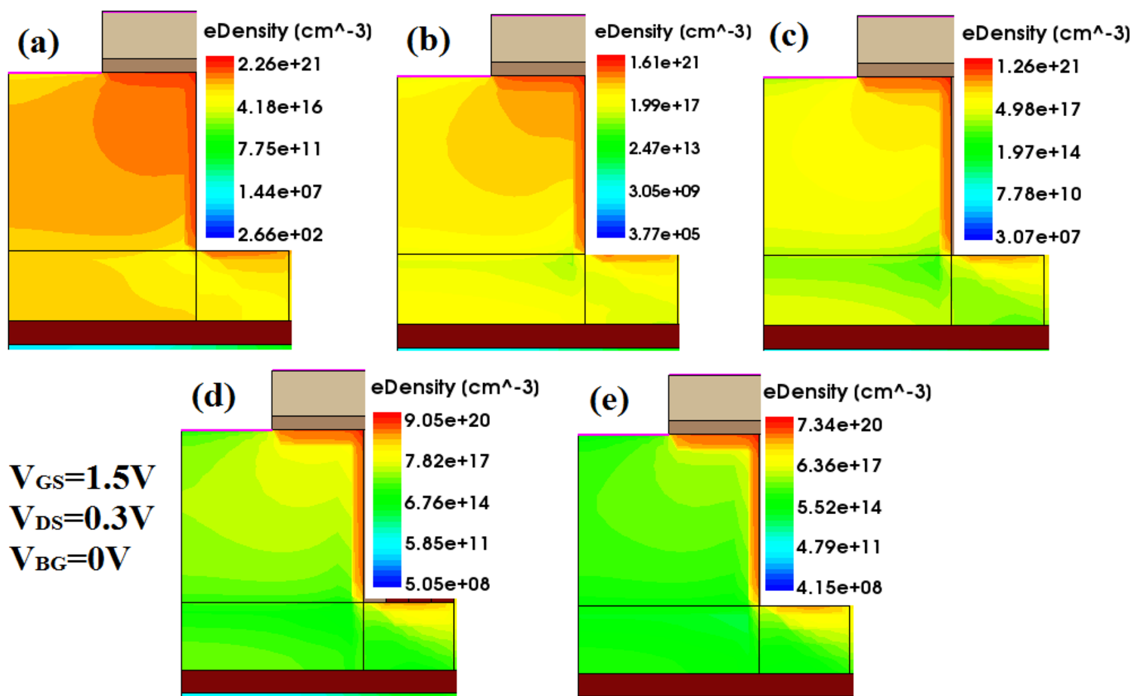

Fig. 5 Electron density contour for varying mole fraction, x **a** 0, **b** 0.3, **c** 0.5, **d** 0.8, **e** 1

Table 2 Detailed analysis of the effects of varying mole fraction in electrical parameters

Mole fraction (x)	Off- current (A/μm)	On- current (A/μm)	On/off ratio	V_{th} (V)	Point SS (mV/dec)
0	2.372×10^{-7}	4.017×10^{-3}	1.6903×10^{4}	−0.044029	11.41
0.3	6.970×10^{-11}	1.900×10^{-3}	2.4330×10^{7}	0.223852	11.94
0.5	1.030×10^{-15}	1.095×10^{-3}	1.0659×10^{12}	0.391704	22.24
0.8	1.490×10^{-14}	5.799×10^{-4}	3.8924×10^{10}	0.540642	33.73
1	1.318×10^{-14}	4.002×10^{-4}	3.0338×10^{10}	0.579259	34.54

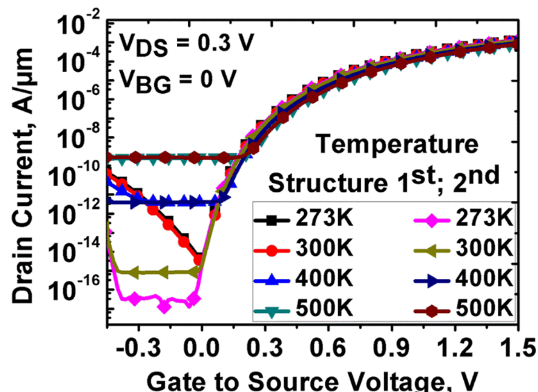

Fig. 6 Transfer characteristics with varying temperature for the proposed devices

on- state as evident from the transfer characteristic plotted in Fig. 6.

It can be noticed that for both the structures the on- state current remains almost unaffected over a range of temperature variation, thoroughly analyzed with the help of Table 3. This is arising out of the principle of conduction mechanism, i.e. BTBT as already mentioned. But in the off-state, i.e. when the gate voltage is 0 V as well as in the subthreshold regime, the tunneling barrier length increases and hence the thermally generated carriers have got a major role to play in the current conduction in this case. Eventually the off- state current is seen to be increased with increasing temperature. This trend is investigated with the help of band diagram plotted for varying temperature for structure 2 as shown in Fig. 7. We can see that for higher temperature, the band gap

Table 3 Temperature variation for proposed structure 1 and structure 2

Temperature in K	Off current (A/μm)	On current (A/μm)	On/off ratio	V_{th} (V)	Point SS (mV/dec)
(a) Structure 1					
273	4.998×10^{-15}	1.397×10^{-3}	2.795×10^{11}	0.317288	21.510
300	3.530×10^{-15}	1.308×10^{-3}	3.705×10^{11}	0.323218	22.097
400	4.092×10^{-12}	1.056×10^{-3}	2.580×10^{8}	0.349795	41.123
500	1.003×10^{-9}	8.755×10^{-4}	8.728×10^{5}	0.379564	85.444
(b) Structure 2					
273	2.210×10^{-15}	1.278×10^{-3}	5.783×10^{11}	0.317368	18.429
300	1.938×10^{-15}	1.189×10^{-3}	6.135×10^{11}	0.323501	19.667
400	3.993×10^{-12}	9.559×10^{-4}	2.394×10^{8}	0.349288	47.160
500	8.713×10^{-10}	7.983×10^{-4}	9.162×10^{5}	0.379061	81.420

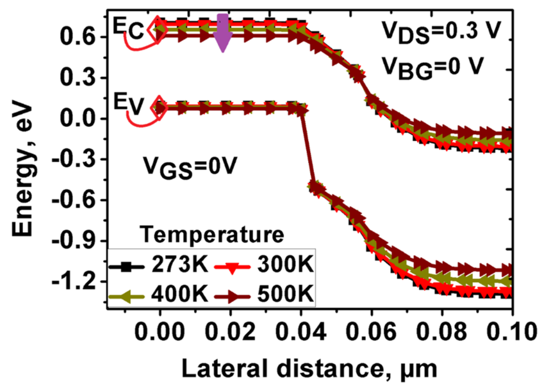

Fig. 7 OFF state band diagram for varying temperature for proposed structure 2 taking lateral cut line at gate oxide–channel interface

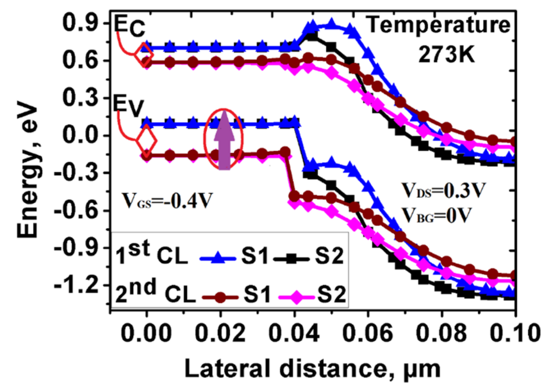

Fig. 8 Energy band diagram at a gate bias of −0.4 V for both of the proposed structures for two of the cut lines; C1: at gate oxide channel interface and C2: at the BOX channel interface

narrowing comes into picture and the conduction energy bands are seen to move downwards. Similar observations are quantified in literature[25] where the impact of bandgap narrowing (BGN) with temperature is expressed by the following equation

$$E_g(T) = E_g(300) - \frac{\propto T^2}{T+\beta}, \tag{4}$$

Here $\alpha = 4.73\times10^{-4}$, $\beta = 636$ K and E_g (300) = 1.08 eV for Silicon.

If we closely observe Fig. 6, we can see that both the structures show almost same performance trend with the variation of temperature. But when the devices are operated at room temperature (300 K) and at the freezing point of water, i.e. 0 °C (273 K) the proposed structure 2 shows better immunity towards leakage current floor towards the ambipolar region. This is due to the incorporation of low-k material towards the drain side of gate oxide to prevent the channel to drain electron tunneling, to be discussed thoroughly in the following section. Further justification can be made with the help of band diagram plotted in Fig. 8 keeping the temperature as 273 K and front gate bias as −0.4 V. Similar trend is expected to be followed at the room temperature too. The energy bands are modulated by the application of negative gate voltage as evident from the band diagram. Sincere investigation suggests that the bands are pulled up by the negative surface potential near the front gateoxide and channel interface as evident by taking lateral cut line (CL) marked in the figure with the help of a pointed arrow. On the other hand, near channel–BOX interface, the energy bands are pushed down due to the accumulated holes. The surface potential contour plotted in Fig. 9 verifies the above-mentioned point. Now if we closely observe the band diagram, it can be seen that the tunneling path length from the valence band of channel to the conduction band of drain is more for structure 2 in case of first CL than that of the structure 1. Similarly, the energy barrier height for the conduction of holes in case of second CL is more for the proposed structure 2. These altogether led to a reduced ambipolar current for the second proposed structure as compared to that of the first one at a negative gate bias of −0.4 V by the calculated factor revealed in Table 4.

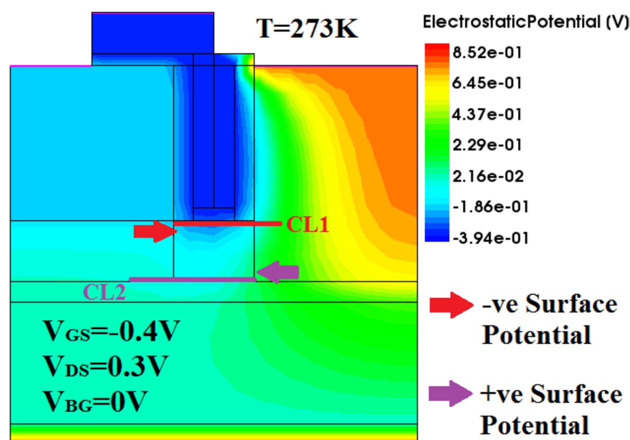

Fig. 9 Surface potential contour at VGS = – 0.4 V keeping temperature 273 K, *CL* cut line

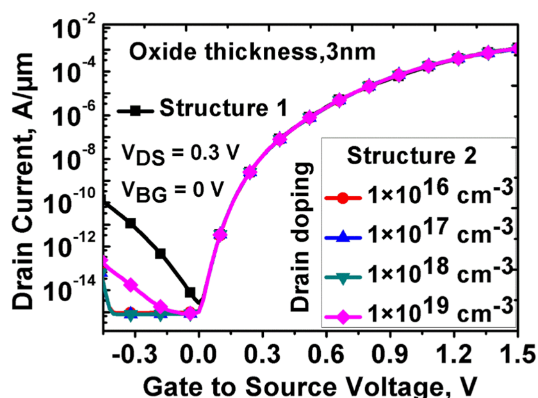

Fig. 10 Transfer characteristic to observe the effect of ambipolarity in the proposed structures

4.3 Analysis of ambipolarity

The ambipolarity, i.e. the conduction of current in both positive and negative gate voltages is due to the conduction of electrons and holes, respectively, which has been a major challenge for TFET architecture, quantified in literature. When a positive gate voltage is applied, the energy band is modulated in the source channel junction and tunneling takes place. But when a negative gate voltage is applied, the energy bands near drain channel junction is influenced and hence it acts as the tunnel junction. For the reduction of ambipolarity basically one of the following methods may be employed, reported previously (a) gate drain underlap, (b) reduction of drain doping, (c) raised buried oxide, (d) applying gate oxide as a combination of low-k and high-k material, (e) applying gate drain overlap, etc. [26–30]. To remain with the architecture of the proposed structure [1], in this work, we have employed the drain doping variation together with the use of high-k and low-k oxide materials simultaneously. Previously, the primary investigation was done in terms of the influence of back gate voltage in the off- state current but a detailed investigation of ambipolarity was omitted.

Here ambipolarity is studied till a negative gate bias of – 0.40 V with the help of transfer characteristic (Fig. 10) for both the proposed structures as shown in Fig. 1 where the front gate oxide has been only HfO_2 (structure 1) and a combination of HfO_2 (towards source side) and SiO_2 (towards channel-drain side) (structure 2). When the gate oxides with different permittivity values come in that fashion the capacitances are in parallel connection and hence the overall capacitance decreases than that of the high-k only case. It affects basically the ambipolar conduction observed exclusively at a gate to source voltage of – 0.4 V. For that specified gate bias the current for structure 1 is found to be 10^4 times more than that of structure 2 at room temperature. This may be attributed to the contour plot of band to band generation rate as shown in Fig. 11. We observe that for structure 2 the BTB generation rate is lesser than the first structure arising out of the electric field distribution and thereby causing the difference in ambipolar current.

Again, if we closely observe Fig. 10 it is seen that for proposed structure 2, as the drain doping decreases, the ambipolar current also decreases. This is due to the incremental parasitic drain resistance with the reduced drain doping [31]. The quantitative analyses in terms of electrical parameters are offered in Table 5. Except structure 1 for all the cases ambipolar current at a gate bias of – 0.4 V is in some factor of fA/μm which can be considered as a major advantage of the said TFET architecture. The on–off

Table 4 Analysis of OFF state current at gate bias of – 0.4 V for both of the proposed structures

Temperature in K	Off current of S1 (A/μm)	Off current of S2 (A/μm)	Ratio of off currents I_{off} (S1)/I_{off} (S2)
273	6.286×10^{-11}	8.869×10^{-17}	7.087×10^{5}
300	4.877×10^{-11}	9.469×10^{-16}	5.150×10^{4}
400	2.050×10^{-11}	3.821×10^{-12}	5.365
500	1.083×10^{-9}	9.097×10^{-10}	1.190

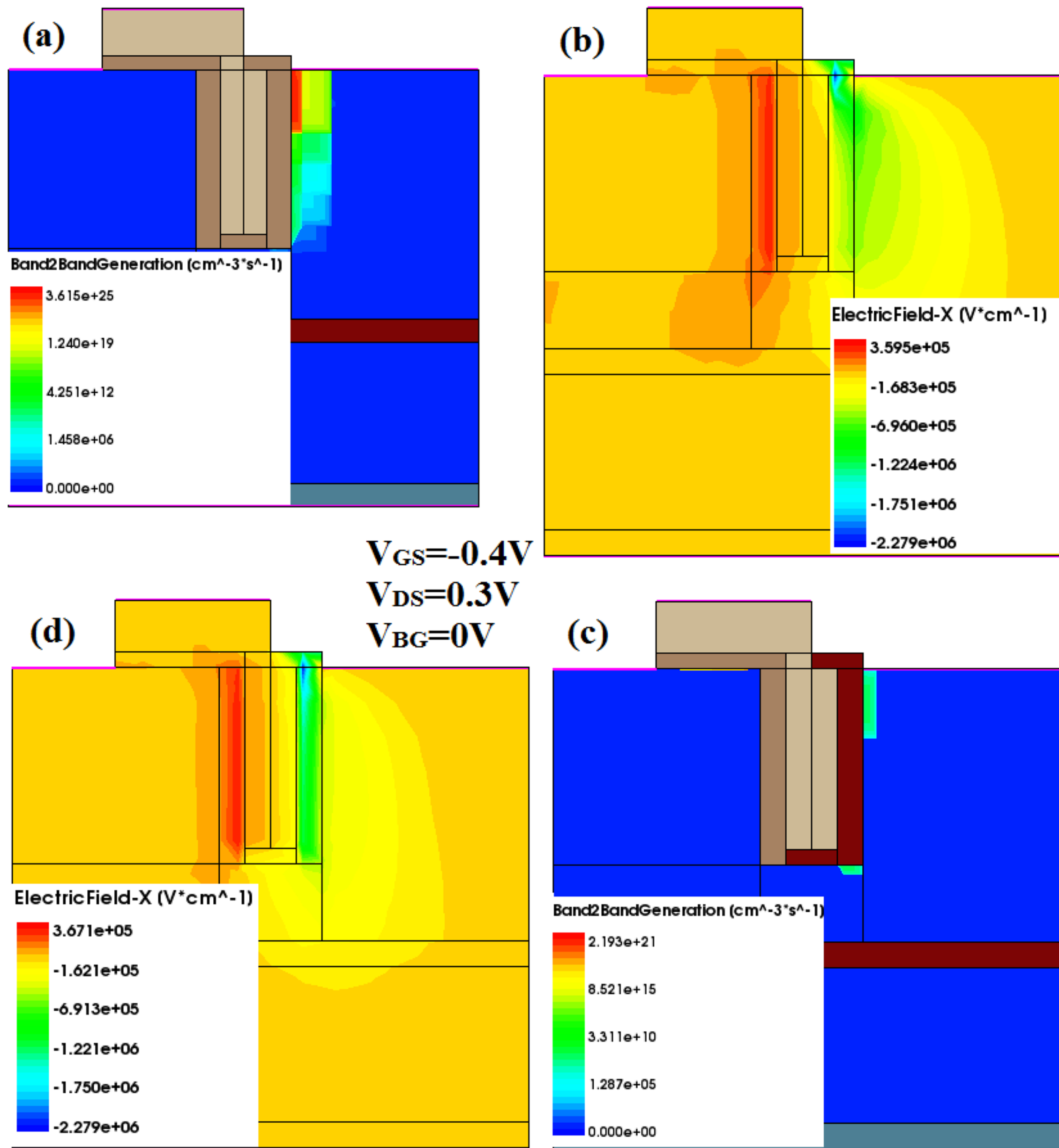

Fig. 11 Band to band generation rate and lateral electric field distribution at − 0.4 V gate bias **a**, **b** proposed structure 1 **c**, **d** proposed structure 2

Table 5 Detailed analysis of ambipolarity for both of the proposed structures

Structure drain doping (cm^{-3})	Off current at $V_{GS} = -0.4$ V (A/µm)	Off current at $V_{GS} = 0$ V (A/µm)	On current at $V_{GS} = 1.5$ V (A/µm)	On/off ratio	V_{th} (V)	Point SS (mV/dec)
S1	4.88174×10^{-11}	2.64928×10^{-15}	1.095×10^{-3}	4.133×10^{11}	0.365694	11.41
S2, 1E16	9.58151×10^{-16}	1.26139×10^{-15}	1.078×10^{-3}	8.546×10^{11}	0.391694	16.94
S2, 1E17	8.17841×10^{-16}	1.04477×10^{-15}	1.084×10^{-3}	1.037×10^{12}	0.391546	22.24
S2, 1E18	8.16516×10^{-16}	1.0273×10^{-15}	1.172×10^{-3}	1.141×10^{12}	0.391153	33.73
S2, 1E19	6.70625×10^{-14}	1.07474×10^{-15}	1.135×10^{-3}	1.0561×10^{12}	0.390724	34.54

current ratio is also excellent compared to MOSFETs with brilliant point SS values.

4.4 RF characterizations of the proposed device architectures

For analog circuit performance of any device the RF analysis plays a vital role which can be characterized by the transconductance (g_m) to estimate the switching response; parasitic gate, drain and source capacitances (C_{gg}, C_{gd} and C_{gs}) to predict the charge conduction mechanism; cut off frequency (f_T) to predict the operating frequency of the device; transit time to determine the speed of the device; time delay to evaluate the circuit performance; PDP to estimate how much power it will consume at a particular delay [31, 32]. Here we have presented all the above performance parameters one by one operating the devices at a frequency of 1 MHz and have compared them for both the proposed structures.

To begin with, the capacitance characteristics have been analyzed as shown in Fig. 12a. The combination of gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd})

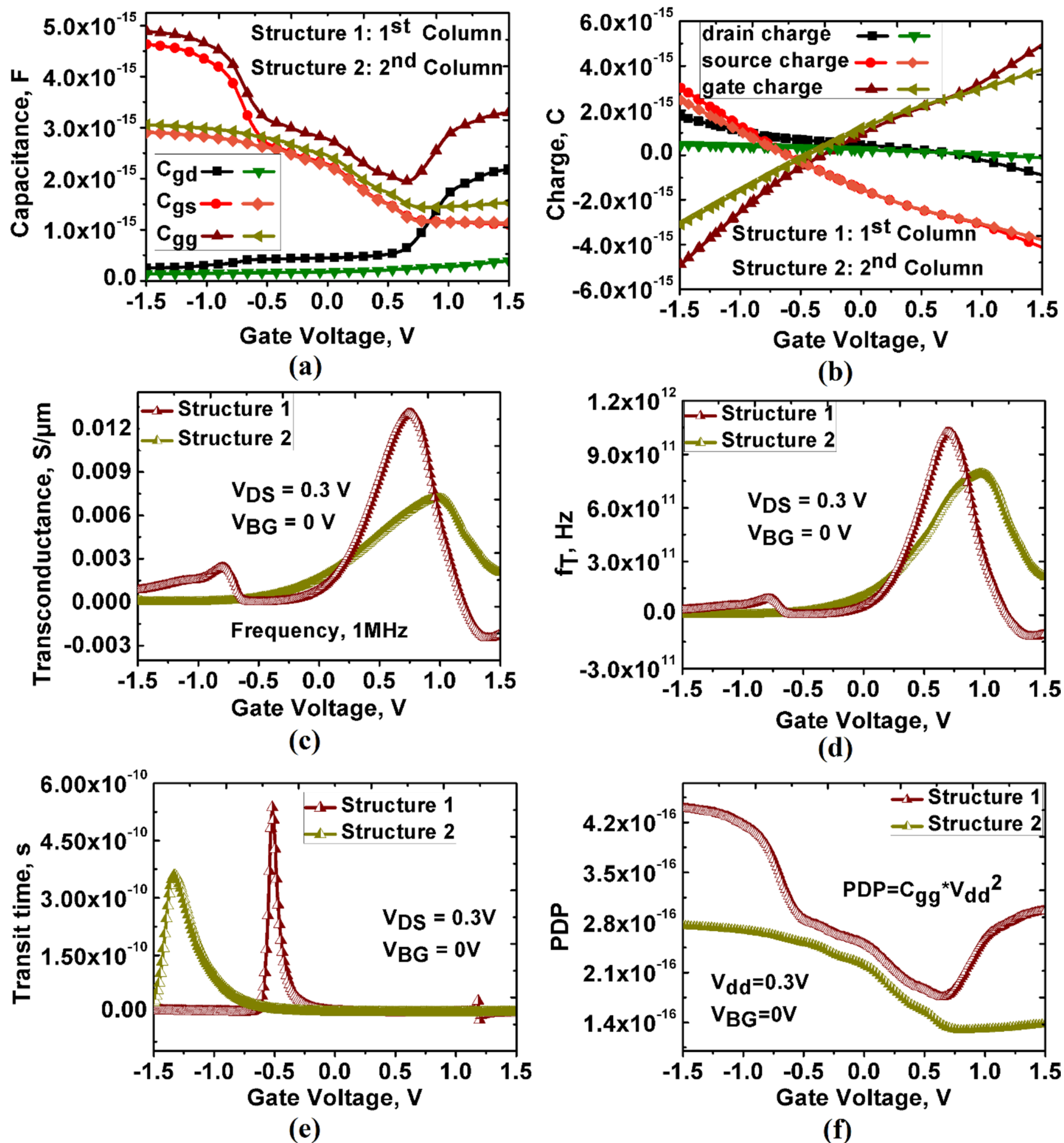

Fig. 12 Comparison of the proposed structures in terms of RF performance parameters **a** capacitances, **b** terminal charges, **c** transconductance, **d** cut off frequency, **e** transit time and **f** PDP against varying gate bias

gives the overall gate capacitance given by the following equation

$$C_{gg} = C_{gs} + C_{gd}, \tag{5}$$

In a conventional p-i-n TFET the gate to source capacitance dominates C_{gg} for the negative gate bias and the gate to drain capacitance dominates C_{gg} for the positive gate bias. But in our proposed SOI DG TFET the trend is little bit different for both the structures. When Fig. 12a is closely observed we notice that for the proposed structure 1 all the capacitance values are more than that of the second. This is due to the high-k gate oxide for the former case. Since the oxide thickness is the same for both the structures, the high-k gate oxide contributes more to C_{ox} which finally gives rise to the larger values of C_{gd}, C_{gs} and C_{gg}. Again due to the same reason, in case of proposed structure 2, the C_{gs} values are more for all the gate bias than that of the C_{gd} since low-k material is incorporated towards the drain side of gate stack as evident from Fig. 1. This behaviour can be verified with the help of terminal charge characteristics plotted in Fig. 12b. In Fig. 12b we notice that the source and drain charges sweep from positive to negative polarity with negative to positive side of the applied gate bias. This is due to the fact that at first for negative gate bias, the holes are accumulated on the surface of channel and near gate oxide all around and then it comes to depletion and finally inversion. But gate charge is seen to transform from negative to positive values which is in accordance with the applied gate bias. In TFET the RF performance is different than that of the MOSFETs due to its unique carrier transport mechanism. Here the band to band tunneling, BTBT and B2B generation plays major role in determining the transconductance of the device (Eq. 6)

$$g_m = \frac{\delta I_d}{\delta V_g}. \tag{6}$$

Larger the transconductance, faster will be the switching response means a small change in input voltage will lead to large change in the drive current. The proposed structure 1 shows a better transconductance performance than that of the proposed structure 2 as seen in Fig. 12c. This may be attributed to the influence of high-k gate dielectric in the gate oxide. The cut off frequency f_T is given by the following equation

$$f_T = \frac{g_m}{2\pi C_{gg}}. \tag{7}$$

As per the definition, the cut-off frequency, f_T is the frequency at which the short circuit current gain converts to unity. f_T totally depends upon the ratio of transconductance and total gate capacitance. From the characteristics as shown in Fig. 12d it is evident that the cut-off frequency for the proposed structure 1 is more than that of the proposed structure 2 in the voltage range where transconductance has followed the same pattern. With increasing gate bias the f_T value increases to reach its peak and then with increasing C_{gg} it truncates down. A device of interest will be the one with higher cut-off frequency and if it could be operated in ISM band then numerous application windows will be opened up for the device operation. In addition to the above-mentioned parameters, the transit time given by Eq. 8 is another important performance parameter for RF analysis.

$$\tau = \frac{1}{2\pi f_T}. \tag{8}$$

It signifies the speed of the device and is inversely proportional to the cut-off frequency. Hence the increasing f_T will have a positive impact on transit time too. If transit time is less then delay will also be less. In this case, as evident from Fig. 12e we can tell that both the proposed structures give satisfactory transit time performance since it is slightly below from 1 ns. Next, the power delay product exemplified by Eq. 9 is quantified in Fig. 12f

$$\mathrm{PDP} = C_{gg} \times V_{DD}^2, \tag{9}$$

The V_{DD} is nothing but the applied drain bias which has been 0.3 V in both the structures. So the graph follows the behaviour of C_{gg} as expected. As evident from Fig. 12f, the PDP for structure 2 is found to be less than that of structure 1 in all bias cases indicating its better energy efficiency. The low power VLSI design methodology now-a-days aim mostly on energy efficiency which is found to be better in the proposed structure 2 making it suitable for low power applications. Last but not the least, it is worth mentioning that the efficiency of low power devices are characterized with the help of transconductance generation efficiency, g_m/I_d which measures the amplification factor of the device per unit energy required to achieve it [33]. From low power analog circuit designer's point of view this term provides the criterion to select the best TFET technologies along with the proper biasing scheme to attain the required functionalities. In traditional FETs this value is limited to ~ 38.5 V^{-1} corresponding to $1/nU_t$, where n is the SS factor and U_t is the thermal voltage [34]. The SS and transconductance generation efficiency is related by Eq. 10 as

$$\frac{g_m}{I_d} = \frac{\ln(10)}{\mathrm{SS}}. \tag{10}$$

At room temperature, in this study the best value of g_m/I_d is obtained to be well above 200 V^{-1} for the best reported point SS case as evident from Table 5.

5 Conclusion

In this work, modification has been done on a structure for SOI DG-TFET previously proposed in literature [1] and is analysed thoroughly in terms of DC and AC characteristics. It has been observed that the device shows a very good performance with high on-state current in the orders of mA, I_{on}/I_{off} ratio above 10^{12} and a steep sub-threshold swing of 11.41 mV/dec when operated with 3 nm gate oxide thickness and 20 nm channel at temperature 300 K. The device is prompt with advantageous operation in terms of its reduced ambipolarity and steep SS with mere independence on temperature variations. Very nominal value of threshold voltage, V_{th} and supply voltage, V_{DD} scaled down up to 0.3 V makes the proposed TFET structure adept for low power applications. The RF performance parameters are extracted and a comparative analysis has been performed which hints the promising analog circuit applications of the proposed device in tera hertz frequency range.

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