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Design and analysis of nano-scaled SOI MOSFET-based ring oscillator circuit for high density ICs

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Abstract
This paper presents the design and analysis of ring oscillator circuit based on nano-scaled SOI MOSFETs for low power applications. Recently, fully depleted silicon-on-insulator (FD SOI) MOSFETs have been recognised as the most viable technology at nanometer nodes. Therefore, it is necessary to analyze the electrical performance of SOI technology MOSFETs and their switching characteristics. In this contribution, firstly we have investigated the short channel immunity of dual metal insulated gate (DMIG) technique-based FD SOI MOSFET and its electrical characteristics has been compared and contrasted with the available state-of-arts. The device has been designed and simulated using numerical ATLAS SILVACO simulator. FD SOI technology along with DMIG technique found to be a better solution, and provide excellent performance (higher I_{on}/I_{off} ratio, and lower sub-threshold slope) than other techniques reported at this node. Additionally, the detailed analysis of surface potential profile, electric field, electron concentration, and the contour plot of conduction current density have been taken into account. Further, for the first time, DMIG FD SOI MOSFET-based CMOS inverter and ring oscillator circuits have been designed using the same numerical simulator. DC and transient analysis itself explains that the designed CMOS inverter and ring oscillator offer lower voltage of operation with reduced power consumption, and high noise immunity. The oscillation frequency of ring oscillator is found as 84.18 GHz at 50 nm channel length.

1 Introduction

In modern communications systems, there is a need of low power and high performance integrated circuits (ICs) to observe wide range of bandwidth in accord with high gain. Additionally, in wireless technologies, the need of high switching speed and synchronization can be achieved with high speed clock signals [1, 2]. Ring oscillator has the capability of producing high speed clock signals along with high bandwidth [2]. Additionally, recent trends in VLSI design require low power optimized ICs for modern internet of thing (IoT) applications [3, 4]. However, the backbones of the high density ICs are Si MOSFETs, as each IC is made up of millions of MOS transistors. So, it is a primary requirement that the available MOS technology should provide the necessary and efficient performance after integration with such ICs.

Moreover, to construct better digital world and improve the quality of the device and user experience, the scaling of the transistors have been continuously done, while increasing performance and reducing power consumption [5, 6]. The endless scaling of MOS device beyond nano meters has affected the device performance and resulted in various short channel effects (SCEs) like, DIBL, off-state tunneling, etc. [6]. So, there is a need to overcome the device reliability issues with conventional Si MOSFETs. Various researches have been done and technologies have given resolution in the device design at nano meters dimensions like FinFET, SOI, and Recessed S/D, etc., Saremi et al. had discussed the attractive features of FinFET-based MOS structures in nano meter regime [7]. Additionally, some of complex structures had also been proposed like, surrounding gate MOSFET [8].

However, channel density problems associated with the conventional structures have been precisely overcome by the un-doped channel concept in SOI technology [9, 10]. Moreover, FD SOI technology has been reported as a most

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promising technology to overcome these problems and seen as an alternative technology due to its high performance constraints and simplest fabrication processes [11–17]. Young had come with the very first model for FD SOI MOSFET and discussed the advantages of this technology [11]. In continuation, Suzuki et al. had also described the perspective of buried oxide to off-flow the leakages in sub-threshold region through analytical model [12]. Nakajima et al. had discussed the strategy of thin BOX optimization over the performance of SOI MOSFETs [13]. Cheng et al. suggested that FD SOI has become a possible technology not only for continued CMOS scaling to 22 nm node, but also for enhancing the performance of legacy technology when rendering to old technology nodes [14]. Mishra et al. proposed a new concept of modified source in designing of FD SOI MOSFET to enhance the electrical characteristics of the device at 50 nm gate length [15]. In this, two levels of source doping have been introduced in source region. In continuation, Srivastava et al. has given the analytical model for this source modification in the design of FD SOI MOSFET to authenticate the reliability of the device [16]. Mukherjee et al. has given the impact of BOX oxide thickness on analogue circuit performance [17].

1.1 Background

Due to scaling in MOS devices, various operating problems related issues have also regarded as major challenging issues in the MOS design. When working beyond 100 nm, the related problems like boron penetration, high gate resistance and poly-si depletion are contrasted to be dominating. These obstructions in device performance have been predominantly overcome by application of metal gates. The metal gates concept was first provided using tantalum gate to replace the polysilicon gate [18]. In continuation to the research, dual metal gate technology [19, 20] has been utilized in the design of FD SOI MOSFET. In which, use of two metal gates in place of single gate, gives a step-up potential at source side and hence no drop in threshold voltage due to inclusion of drain potential, and hence reduced SCEs. J. P. Colling had concluded the importance of multi-gate structures in SOI MOSFETs [19]. Kumar et al. had developed a model of FD SOI MOSFET using dual material gate and discussed the potential benefits of this technology [20]. Additionally, Priya et al. has given a concept of triple-metal-gate with recessed S/D technology in the design of FD SOI MOSFET [21]. This structure has been intensively designed to decrease the series resistance of S/D regions, which in turn improves the drive current capability of the device and hence enhanced circuit performance.

In dual metal gate technology two metal gates of different work functions are used. However, the major challenge is to find two metals with suitable work functions and a way to integrate them into a modern metallization process in MOS fabrication. So, the integration of multiple metal gates side by side has some serious fabrication complexities [22]. These complexities can be overcome by placing an insulator in between two metal gates. Recently, Wei et al. have discussed the incorporation of insulator in between two metal gates and the advantages over short channel effects, like DIBL [23]. However, none has discussed this dual metal insulated gate technique with source engineered FD SOI MOS technology for the design of ring oscillator circuit. It is, therefore, necessary to investigate the performance of DMIG technique in the design of source engineered FD SOI MOSFET for low power applications.

1.2 Contribution

In this work, the dual metal insulated gate technique in the design of source engineered FD SOI MOSFET has been employed for the first time. It has been assured that the device is performing at low power and successfully accommodating the SCEs as compared to other devices at this node [15–17]. Additionally, for the first time, a ring oscillator circuit has been designed with nano-scaled DMIG FD SOI MOSFETs for the analysis of delay, power consumption and oscillation frequency. This paper has been divided in following sections. First, the device structure and proposed fabrication feasibility of the device are discussed in Sect. 2. Then, the comparative analysis over DC characteristics and potential benefits of FD SOI MOSFETs has been taken into account in Sect. 3. Further, studied device based ring oscillator circuit has been analyzed on the basis of CMOS inverter as individual stage in Sect. 4. The overall contribution of the work is discussed in conclusion Sect. 5.

2 Device structure and specification

Figure 1 shows the cross sectional view of the proposed FD SOI MOSFET 'C' along with two different MOS structures, 'A' and 'B' [15], and the complete specifications are listed in Table 1. Where, L is the channel length and T_{ox} is front oxide thickness. The carrier concentrations are denoted as P_{sub}, N_{s+}, N_{s-} and N_d for substrate, highly doped source, lightly doped source and for drain region, respectively. The BOX and silicon film thickness are denoted as T_{BOX} and T_{si}. For the comparison purpose, all the three devices have been modelled with same parameters. The device A is the conventional structure of FD SOI MOSFET and device B has already been recognised at same technology node of 50 nm [15]. In device structures 'B' and 'C', N_{s+} has been taken up to $T_{si1}=2$ nm and N_{s-} concentration for $T_{si2}=10$ nm, such that $T_{si}=T_{si1}+T_{si2}$ [15]. The substrate voltage is considered as $V_{sub}=0$ for all three devices studied here. The device C

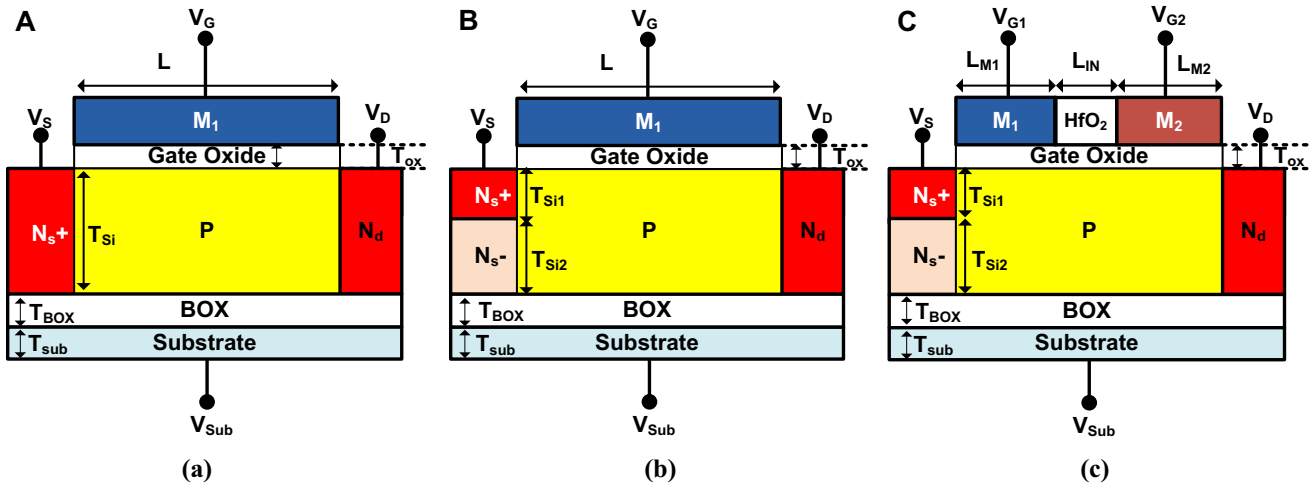

Fig. 1 Devices under consideration: **a** device A: conventional FD SOI MOSFET, **b** device B: referenced FD SOI MOSFET [15], **c** device C: proposed DMIG Source Engineered FD SOI MOSFET

is featured with two metal gates (M_1 and M_2) of materials molybdenum and titanium with work functions 4.6 eV and 4.4 eV, respectively, and insulated gap is of high-k dielectric HfO_2. The gate voltages V_{g_1} and V_{g_2} are kept equal in device C. Moreover, for the proposed device 'C', channel length (L) is equal to the sum of two metal gates and the insulator gap ($L = L_{M1} + L_{IN} + L_{M2}$), where L_{M1} and L_{M2} are the length of the two metal gates and are taken as 22 nm each, and L_{IN} is the insulator gap of 6 nm.

2.1 Fabrication feasibility of the proposed device

The device fabrication is experimentally feasible with the following steps as shown in Fig. 2. Moreover, as per the recent literatures, the fabrication of FD SOI MOSFETs is possible [24–30]. Very firstly, a SOI wafer will be prepared on a patterned Si sample using UNIBOND process with smart cut technology [24]. These processes involves H+ ion-implantation into a Si donor wafer followed by cleaning, bonding, smart-cut and anneal process as well. Then, the top silicon layer will be doped using boron implant to control the threshold of the device. This process is reported better as compared to SiMOX technology [24]. Then next step is the formation of multiple BOX profile N_s^+/N_s^- implantation at source side. The N_s^+/N_s^- implantation of (2 nm/10 nm) at source side could be done with active substrate ion-implantation technique [25] and also N_d implantation at drain side of 12 nm followed by annealing process for dopant activity. Then, the metal contact is formed over and above these S/D implantations. Then, the high-k gate dielectric (HfO_2) of 1 nm is grown over through active layer deposition method at defined temperature and pressure as discussed in [26]. After this step, two separated metal gates (M_1 and M_2) are deposited on either sides of the gate dielectric using normal evaporation method on the top of the gate dielectric considering E-beam lithography along with thermal anneal process and followed by deposition of HfO_2 inside the visible cavity through plasma active layer deposition [27–30]. There may be possibility of process induced damage, such that gate oxide is not completely etched and residual oxide is left or it may get damaged at the gate edge, resulting in dielectric edge damage. This may removed by the multi-step dielectric damage process after etching as suggested in [28]. Additionally, chemical mechanical polishing (CMP) is suggested to perfectly separate the two metal gates as described in [29, 30]. After the gate pattering, nano cavity can be produced similarly as per the fabrication steps in [29, 30]. Additionally, one more step is required to clear the HfO_2 gate dielectric over the G/S/D electrodes, i.e., reactive ion etching. Then acetone solution is used to remove the unwanted contact areas in sample and finally the sample will be ready for test [25, 27]. The complete device dimensions and doping levels are listed in Table 1.

2.2 Simulation setup

The electrical performance of these devices has been extensively examined using numerical ATLAS Silvaco simulator [31]. For the accurate estimation of the studied designs, various mathematical models have been included in the simulator. As for the majority career life time, Shockley–Read–Hall (SRH) generation and recombination model has been used. To accommodate the temperature dependency on mobility, the Lombardi mobility and constant voltage and temperature (CVT) model has been taken into account. FLDMOB model has been included to analyse effects of saturation velocity due to high transversal electric fields because of small dimensions. Additionally, Gummel Newton and

Table 1 Device parameters and specifications for the devices under study

Devices	Parameters								
	L (nm)	T_{ox} (nm)	P_{sub} (cm^{-3})	N_{s+} (cm^{-3})	N_{s-} (cm^{-3})	N_d (cm^{-3})	T_{Si} (nm)	T_{Si1} (nm)	T_{Si2} (nm)	T_{BOX} (nm)
Conventional FD SOI MOSFET 'A'	50	1	1×10^{16}	1×10^{20}	Not used	1×10^{20}	12	Not used	Not used	5–20
Referenced FD SOI MOSFET 'B' [15]	50	1	1×10^{16}	1×10^{20}	1×10^{17}	1×10^{20}	12	2	10	5–20
Proposed DMIG FD SOI MOSFET 'C'	50	1	1×10^{16}	1×10^{20}	1×10^{17}	1×10^{20}	12	2	10	5–20

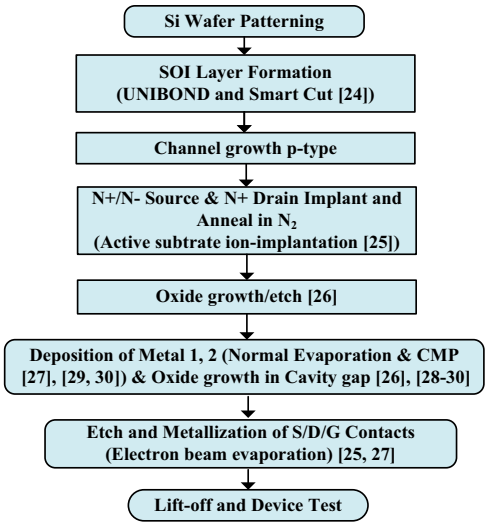

Fig. 2 Process flow of proposed DMIG source engineered FD SOI MOSFET

drift diffusion model has been chosen for current transport (on–off switching). In addition to this, the quantum confinement model needs to be included in nano-scaled devices. For this, the Bohm quantum potential (BQP) model is used here along with hydrodynamic model. In which, the semi-classical potential is converted into quantum potential in the same manner as the continuity equation. The provided meshing strategies in [31] have been utilized for the deep matrix calculations at each step of simulation.

3 DC characteristics of the proposed FD SOI MOSFET

Figure 3 shows the drain current versus gate voltage characteristics of the studied devices (A, B and C). From, Fig. 3a, it can be seen that the proposed device C is better as compare to other. As, the device C is offering low-off-state leakage current and sufficient drive current at drain bias of 0.1 V. This is due to the proposed DMIG technique which increases the average electric field under the gate M_1 and this automatically enhances the carrier life time of the carriers. That results in higher gate transport efficiency. Gate transport efficiency is average travelling velocity of electron through the channel which is directly related to the distribution of electric field in the channel. Hence, the gate controllability over the channel is improved in device C as compare to device A and B at sufficient drain bias. It is also worth here to mention that due to the source modification technique adopted in device B and C, the parasitic capacitance effects have been greatly reduced when a lightly doped N- layer has been introduced underneath the highly doped *N*+ layer in source region as compared to the conventional FD SOI MOSFET

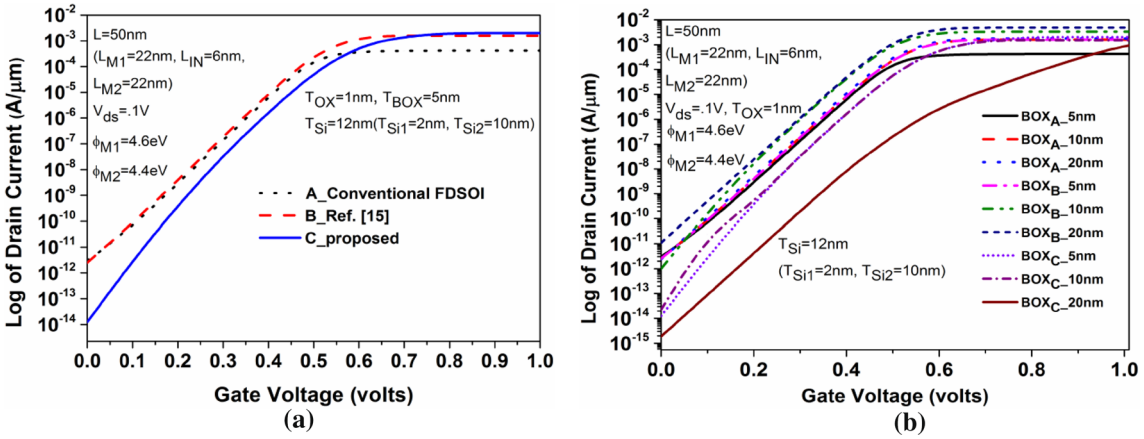

Fig. 3 Input (I_d vs. V_{gs}) characteristics **a** for the devices under study at fixed BOX thickness of 5 nm, **b** impact of BOX oxide thickness variation on I_d versus V_{gs} characteristics

(A). The switching ratio (I_{on}/I_{off}) is calculated maximum for device C as 10^{12}, which is quite enough to justify the immunity of the device C over various short channel effects.

It is also necessary to verify the device performance with certain design parameters variation. For a FD SOI MOSFET, proper selection of buried oxide thickness is necessary to conquer the off-state leakage. Figure 3b indicates the I_d versus V_{gs} characteristics of studied devices at different BOX oxide thickness. It can be concluded from the plot, as the BOX thickness is increased from 5 to 20 nm, the drive current is also incremented because of the enhanced lateral field. The drive current is found maximum for device C as 2.7 mA at BOX thickness of 20 nm due to the insulated gate technique.

Moreover, there is a trade-off in selection of BOX thickness as per the required application necessities. In this way, the proposed device is almost free from short dimension effects. This analysis has been listed in Table 2, in which the exact simulated extractions are mentioned clearly.

The main feature of the dual metal insulated gate technology is that it introduces a potential step in channel region of MOSFET. So, it is, therefore, necessary to verify the threshold voltage roll-off effect for the further conclusions. Figure 4a, b shows the graph of threshold voltage variation with device channel length for the devices taken into consideration for different drain voltages of 0.05 V and 0.1 V, respectively. The maximum slope method of threshold voltage extraction is used during TCAD simulations [31]. One can observe from the plots that there is no roll-off seen in the case of proposed device C and small roll-off in case of device B when V_{ds} is increased from 0.05 to 0.1 V. Whereas, device A shows the higher roll-off as compared to device B and C. This also justifies that the DMIG enabled device is free from drain electric field penetrations and offers lower voltage of operation as well. So, DMIG technology provides more flexibility to optimize the channel region under low work-function metal (M2) because of device threshold depends upon higher work-function metal (M1) and high-k insulator gap maintains the potential excursions'.

Threshold voltage variation with channel length at different buried oxide thickness is listed in Table 3. The threshold voltage is increased by decrease in BOX thickness which assures better immunity to short channel effect at small BOX thickness as compared to other reports [15–17]. Increasing BOX thickness reduces threshold voltage. So there is less consumption of gate voltage at thicker BOX layer.

The plot of sub-threshold slope versus channel length has been shown in Fig. 5 for the studied devices at T_{BOX}= 5 nm. The plot shows that the device C is approaching towards the ideal value of sub-threshold slope as compared to

Table 2 Detailed analysis of drive current (I_{on}), off-state leakage (I_{off}) and switching ratio (I_{on}/I_{off}) for the devices under study at different buried oxide thickness (T_{BOX})

Device	I_{on} (A)			I_{off} (A)			I_{on}/I_{off}		
	T_{BOX} = 5 nm	T_{BOX} = 10 nm	T_{BOX} = 20 nm	T_{BOX} = 5 nm	T_{BOX} = 10 nm	T_{BOX} = 20 nm	T_{BOX} = 5 nm	T_{BOX} = 10 nm	T_{BOX} = 20 nm
A	0.42×10^{-3}	1.5×10^{-3}	1.77×10^{-3}	3×10^{-12}	2.5×10^{-12}	2.38×10^{-12}	0.14×10^{9}	0.6×10^{9}	0.74×10^{9}
B	1.59×10^{-3}	3.28×10^{-3}	4.78×10^{-3}	2.5×10^{-12}	1.2×10^{-12}	1.08×10^{-11}	0.63×10^{9}	2.73×10^{9}	4.42×10^{9}
C	2.03×10^{-3}	2.5×10^{-3}	2.7×10^{-3}	1.25×10^{-14}	2.25×10^{-14}	1.89×10^{-15}	1.6×10^{11}	0.66×10^{11}	1.42×10^{12}

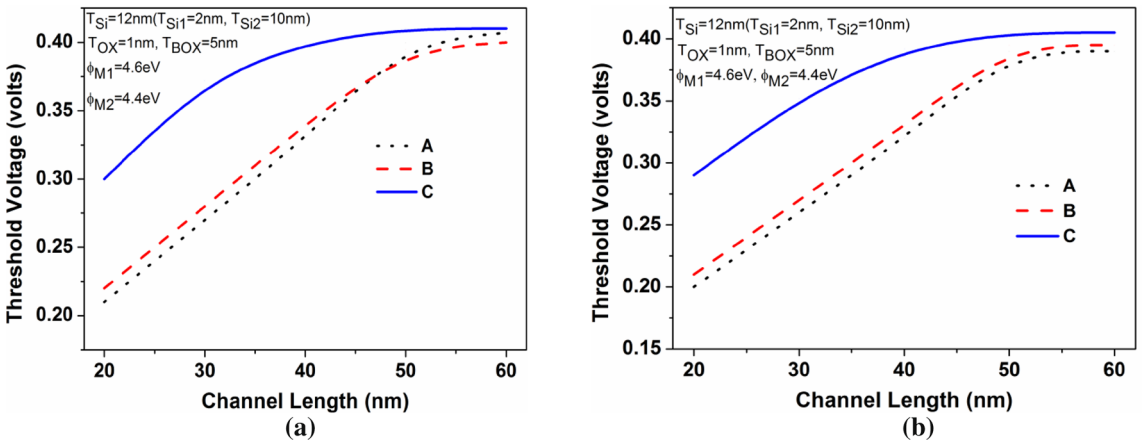

Fig. 4 Threshold voltage variation with channel length: **a** at V_{ds} = .05 V, **b** at V_{ds} = 0.1 V

Table 3 Threshold voltage variation at different buried oxide thickness with variation in drain voltage (V_{ds}) at L = 50 nm

Device	Threshold voltage (V)					
	V_{ds} = 0.05 V			V_{ds} = 0.1 V		
	T_{BOX} = 5 nm	T_{BOX} = 10 nm	T_{BOX} = 20 nm	T_{BOX} = 5 nm	T_{BOX} = 10 nm	T_{BOX} = 20 nm
A	0.391	0.382	0.322	0.407	0.365	0.319
B	0.395	0.398	0.339	0.401	0.372	0.322
C	0.405	0.403	0.397	0.410	0.403	0.402

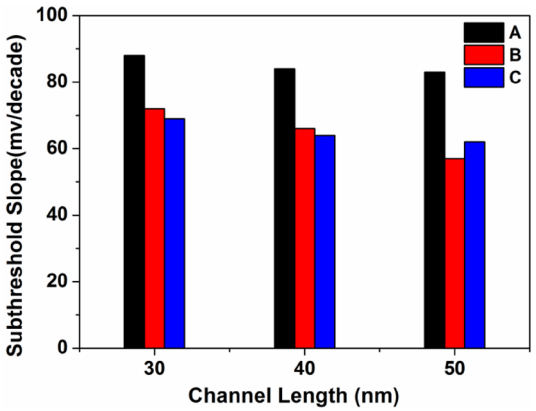

Fig. 5 Effect of channel length scaling on sub-threshold slope for all devices under study at T_{BOX} = 5 nm

device A and B. This dictates that the proposed device C can be scaled down till 30 nm and also as per analysis Table 4, the proposed device have scope of further scaling down till 20 nm. The analysis of sub-threshold slope with variation in BOX thickness has also been extracted by two-dimensional numerical simulations here and listed in Table 4. The channel length of device C is scaled down as follows L = 50 nm (L_{M1} = 22 nm, L_{IN} = 6 nm, L_{M2} = 22 nm), L = 40 nm (L_{M1} = 17 nm, L_{IN} = 6 nm, L_{M2} = 17 nm), L = 30 nm (L_{M1} = 13 nm, L_{IN} = 4 nm, L_{M2} = 13 nm) and L = 20 nm (L_{M1} = 8 nm, L_{IN} = 4 nm, L_{M2} = 8 nm).

It is observed from the extraction results that there is a less variability in device C as the BOX thickness is increased to 20 nm. This is due to the suppression of various parasitic effects because of dual metal insulated gate technique with source engineered FD SOI MOSFET. The source

Table 4 Sub-threshold slope with variation in BOX thickness (T_{BOX} in nm) at different channel length

Device	Sub-threshold Slope (mV/decade)											
	L = 20 nm			L = 30 nm			L = 40 nm			L = 50 nm		
	T_{BOX} = 5	T_{BOX} = 10	T_{BOX} = 20	T_{BOX} = 5	T_{BOX} = 10	T_{BOX} = 20	T_{BOX} = 5	T_{BOX} = 10	T_{BOX} = 20	T_{BOX} = 5	T_{BOX} = 10	T_{BOX} = 20
A	93	97	108	88	92	102	84	87	98	83	84	86
B	81	85	94	72	76	82	66	68	70	57	62	63
C	78	83	89	69	73	79	64	66	65	62	63	63

engineering will result in variation of built in potential of the device that will off-flow the minority carriers' conduction during weak inversion and will cause the device leakage free. Also the DMIG with source engineered results in suppression of trans-capacitances. So, these two techniques will enhance the device performance and the studied device can be used for high density ICs.

Moreover, the reported subthreshold-slope for device B is 57 mV/decade. However, the proposed device offers better drive current and excellent switching (I_{on}/I_{off} ratio) performance as compared to device B, which dominates the short channel performance in a device. So, this must be considered as a trade-off depending upon the requirements. The performance of the proposed device has also been verified in terms of DIBL and compared against recent literatures [15, 23] as shown in Fig. 6. It is find the proposed device exhibits better performance due to the utilization of DMIG and source engineering both as compared to [15] and [23].

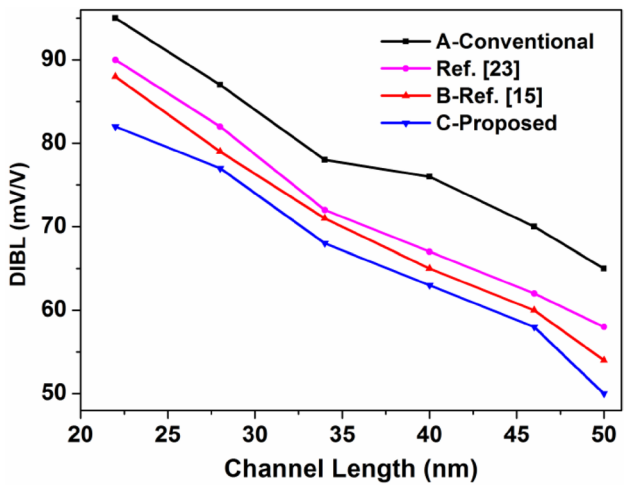

Fig. 6 Comparison of different MOSFETs with proposed FD SOI MOSFET in terms of DIBL

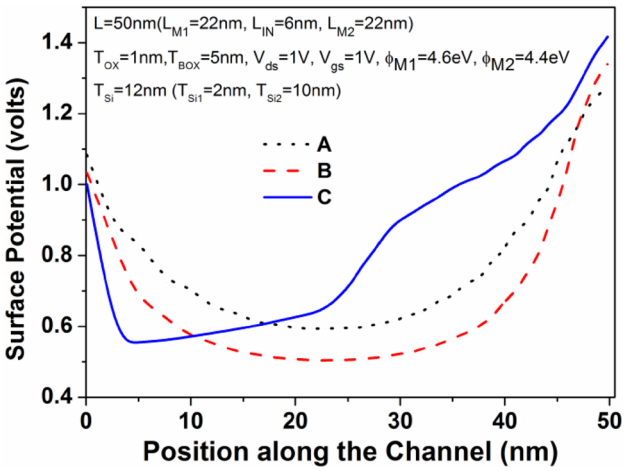

Fig. 7 Surface potential profile versus channel length of the studied MOSFETs (cutline at $T_{si}=2$ nm)

3.1 Potential benefits of the proposed FD SOI MOSFET

Further to verify the results obtained above, a brief discussion over the surface potential profile, channel electron concentration, electric field and the contour plot of conduction current density have also been taken into consideration. Figure 7 shows the surface potential variation along the channel for the devices under study. In proposed device C, it has been found that the location of the minima surface potential is moved more along the source side of the channel due to the inclusion of HfO_2 gap in between two metal gates as compared to device A and B. This step-like function profile clearly indicates that the weak inversion is taking place at the source side of the channel. This will result in more uniform electric field in the channel area as the electric field peak will be located towards the source end. Hence, the source side of the channel region is screened from the changes in the drain potential, i.e., the drain voltage is not affecting the gate controllability over the conduction. Hence, the proposed device with DMIG and source engineering screen-off the drain bias effects twice as compare to other technologies at this node. The position of minima along with the corresponding potentials is listed in Table 5.

It is also necessary to demonstrate the performance of the proposed device further by observing the electron concentration under the channel area. The comparative study of carrier concentration for the devices under consideration is shown in Fig. 8. One can observe from the figure that the channel concentration is more uniform and optimum in case of proposed MOSFET and decreasing beyond source to drain edge. This characteristics itself explains the suppression of drain penetration towards gate control. It is also worth here to mention that the continuous/unceasing concentration has been recorded in the channel area under the high-k gap. This evidence itself supports the working of the proposed device with inclusion of high-k that there are various benefits in considering high-k gap.

Table 5 Minima position and value of surface potential along the channel

Devices	Minima position (nm)	Minimum surface potential (V)
A	21.62	0.59372
B	16.21	0.52787
C	4.83	0.54395

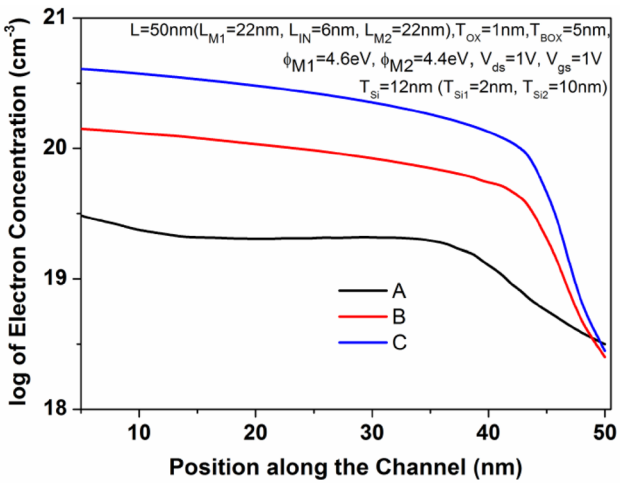

Fig. 8 Comparison of different MOSFETs with proposed FD SOI MOSFET in terms of channel electron concentration (cutline-$T_{si}=2$ nm)

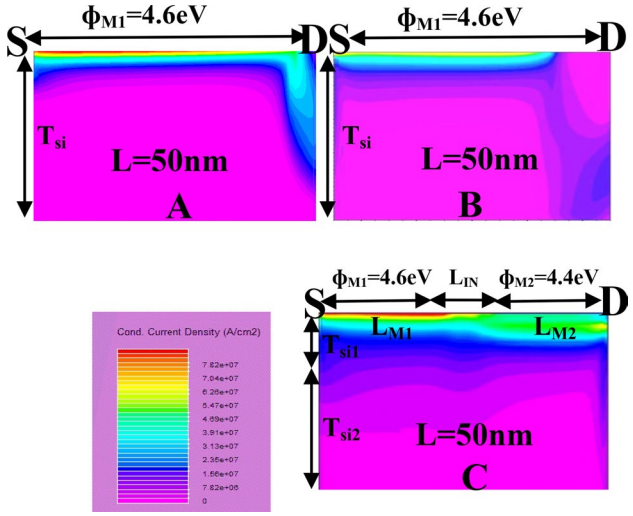

Fig. 10 Contour plot of conduction current density (A/cm^2) of the studied MOSFETs A, B and C at $V_{ds}=1$ V, $L=50$ nm ($L_{M1}=22$ nm, $L_{IN}=6$ nm, $L_{M2}=22$ nm,), $T_{BOX}=5$ nm, $T_{ox}=1$ nm and $T_{si}=12$ nm ($T_{si1}=2$ nm, $T_{si2}=10$ nm)

In addition to this, the plot of electric field along the channel length is shown in Fig. 9. Similarly, it also supports the potential profile as the maxima peak of the electric field is observed more nearer towards source in case of device C followed by device B and A, respectively. So, the device has better short channel immunity.

At last, the contour plots of conduction current density inside the channel at $L=50$ nm is presented in Fig. 10. It is evident that the proposed device exhibits more uniform current density as compared to device A and B inside the channel. The electrical performance comparison of different MOS structure available in the literature has also been done in Table 6. One can find that the proposed MOS structures offers lowest off-state leakage and better switching ratio of 10^{11} at specified dimensions.

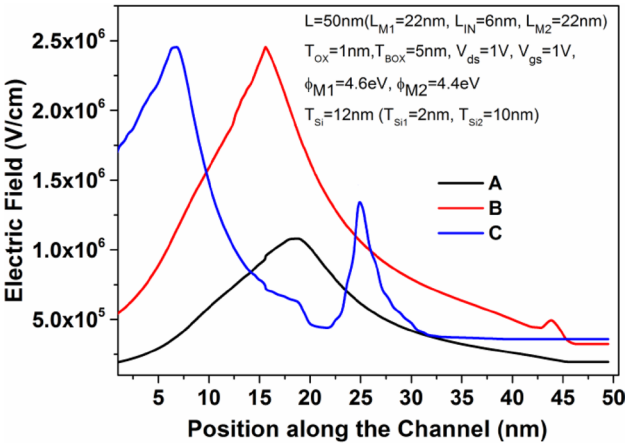

Fig. 9 Electric filed (V/cm) behaviour of the devices taken under study (cutline at $T_{si}=2$ nm)

As per the above discussion, it has been clarified that the studied device C has excellent immunity over various small dimension effects. It is also worth here to mention that the DMIG based MOS device will reduce the fabrication complexity due to insertion of insulator gap as compared to conventional DMG technology based MOSFETs. Additionally, the line-edge roughness effect [22] will be overcome by DMIG based MOSFETs.

Till now, a comparative study of the devices under consideration has been presented and the evidences clearly explain the significance of the proposed device C when it is compared with devices A and B [15] at the same technology node. It is, therefore, necessary to analyse this device further at circuit level. In next section, ring oscillator circuit has been analysed on the basis of CMOS inverter designed with the proposed DMIG based FD SOI MOSFET.

4 Ring oscillator circuit

In this section, high performance and power efficient ring oscillator circuit has been designed using DMIG based source engineered FD SOI MOSFET. Ring oscillator consists of odd number of delay stages in feedback form as shown in Fig. 11. So, it is necessary to evaluate the performance of individual delay stages. Here, all three delay stages are assumed to be identical and output load capacitances are taken as equal to each other with value ($C_{L1}=C_{L2}=C_{L3}=C_L$). Moreover, the delay calculation in a CMOS inverter essentially depends upon the output load capacitance. The accurate value of the output load capacitance can be calculated

Table 6 Electrical performance comparison of different MOSFETs with proposed FD SOI MOSFET

References	L (nm)	I_{on} (mA)	I_{off}	V_{th}	T_{ox} (nm)	Subthreshold-slope (mv/decade)	I_{on}/I_{off}
SOI-FinFET [7]	50	1	10 pA	0.27	2	78.16	10^8
FD SOI [32]	50	0.1	1 pA	0.30	1	60.00	10^8
MS FDSOI [15]	50	0.1	0.8 fA	0.38	1	57	10^9
FD SOI [33]	50	3	80 fA	0.30	1	60	10^{10}
FDSOI [34]	50	0.08	5 pA	0.32	2	–	10^8
Proposed	50	2.03	0.125 fA	0.40	1	62	10^{11}

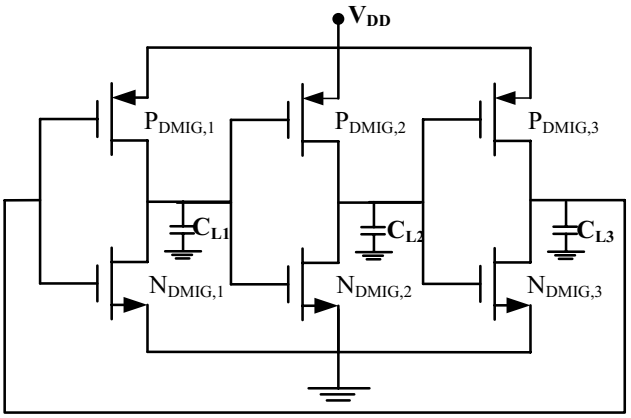

Fig. 11 Three stage ring oscillator circuit designed using proposed DMIG FD SOI MOSFET

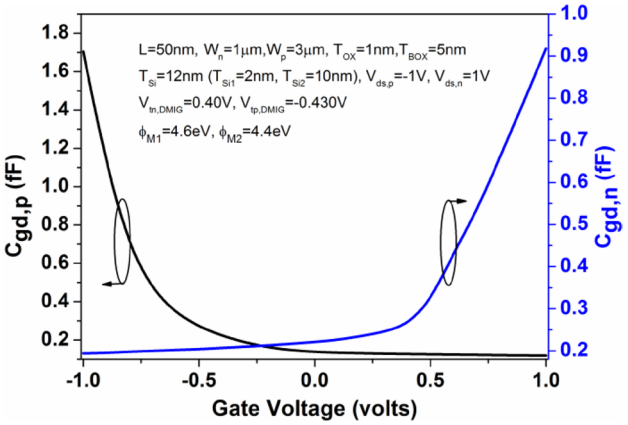

Fig. 12 Plot of $C_{gd,p}$ and $C_{gd,n}$ with variation in V_{gs} for proposed MOSFET for $L=50$ nm, $V_{ds,p}=-1$ V, $V_{ds,n}=1$ V

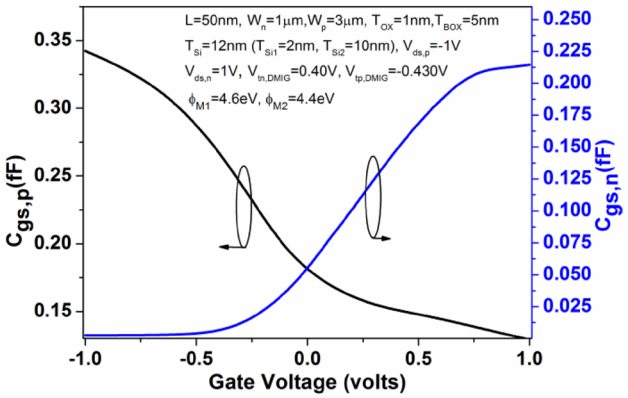

Fig. 13 Characteristics of $C_{gs,p}$ and $C_{gs,n}$ versus V_{gs} for proposed MOSFET for $L=50$ nm, $V_{ds,p}=-1$ V, $V_{ds,n}=1$ V

by combining the overall parasitic capacitances between the output node and the ground [35].

In nanoscaled transistors, basically the parasitic capacitances are C_{gs}, C_{gd}, C_{sb} and C_{db}. Moreover, the source to bulk capacitance (C_{sb}) has almost negligible effect on transient characteristics of CMOS inverter, since the source-substrate potential is kept zero in case of PMOS and NMOS both. Moreover, the gate to drain parasitic capacitance (C_{gd}) the gate to source capacitance (C_{gs}), and the drain to bulk parasitic capacitance (C_{db}) will be present in calculation.

The plots of $C_{gd(n/p)}$, $C_{gs(n/p)}$ and $C_{db(n/p)}$ are shown in Figs. 12, 13, and 14. It is clear from the plot that the resulting optimum values of $C_{gd,p}$, $C_{gd,n}$, $C_{gs,p}$, $C_{gs,n}$, $C_{db,p}$ and $C_{db,n}$ are 1.70 fF, 0.918 fF, 0.21 fF, 0.342 fF, 0.056 fF, and 0.031 fF, respectively, for $L=50$ nm. So, the maximum value of output load capacitance ($C_L=C_{gd,p}+C_{gd,n}+C_{gs,p}+C_{gs,n}+C_{db,p}+C_{db,n}$) could be approximated as 3.257 fF for $L=50$ nm and further it slightly decreases with scaling in channel lengths. Similarly, the calculated value of C_L is found as 2.80 fF and 2.63 fF for $L=40$ nm, 30 nm, respectively. Since, lesser change in parasitic capacitances is observed at $L=40$ nm, 30 nm and as it is always advisable to investigate the device performance at circuit level by considering optimum case of parasitic effects. So, we have considered the maximum value of parasitic load capacitance $C_L=3.25$ fF to analyze the parasitic behaviour of the proposed device at lower dimensions. Now, the transient and DC analysis of the proposed individual inverter stage has been performed using the numerical simulator ATLAS Silvaco [31].

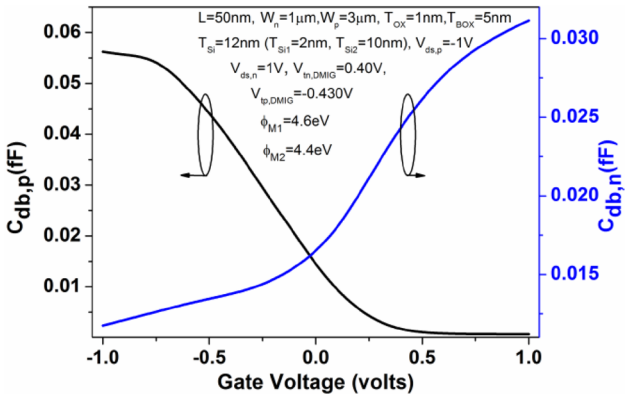

Fig. 14 Characteristics of $C_{db,p}$ and $C_{db,n}$ versus V_{gs} for proposed MOSFET for $L = 50$ nm, $V_{ds,p} = -1$ V, $V_{ds,n} = 1$ V

4.1 DC analysis of individual inverter stages

The voltage transfer characteristics of the DMIG source engineered FD SOI MOSFET based inverter circuit is shown in Fig. 15a, b. The operation of the proposed inverter can be discussed as follows. From, Fig. 15a, it is clear that the PMOS device is in the *ON* state when the input voltage (V_{in}) is below the threshold voltage of NMOS transistor ($V_{tn_{DMIG}}$) and the output voltage will result in V_{DD}. Now, as the input voltage is slightly above $V_{tn_{DMIG}}$, the conduction of NMOS transistor starts in saturation region, and the output voltage will begin to decrease. As the output voltage decreases further, PMOS transistor will conduct in saturation mode. Now as the output voltage becomes less than $V_{in} - V_{tn_{DMIG}}$, NMOS transistor will work in linear region. Finally, as the voltage exceeds the $V_{dd} + V_{tp_{DMIG}}$, the pMOS turns off. The TCAD extracted values of $V_{tn_{DMIG}}$ and $V_{tn_{DMIG}}$ are 0.40 V and −0.430 V, respectively. It is also clear from the plot that the characteristics of the inverter is almost centred around $V_{dd}/2$, which is significant in the implementation of the proposed inverter with high density ICs such that high thermal stability.

Figure 15b shows the effect of supply voltage scaling on voltage transfer characteristics of the device. Since, the modern era is running around the optimization of low power enabled integrated circuits. Here, the values of $V_{tn_{DMIG}}$ and $V_{tp_{DMIG}}$ are 0.214 V and −0.226 V, respectively. From, Fig. 15b, it is clear that the voltage transfer characteristics of the proposed MOSFET attains the similar nature even if the supply voltage is scaled to $V_{dd}/2$ and also the switching threshold ($V_{m_{DMIG}}$) is found good. This assures the acceptable performance of the proposed CMOS circuit even at lower supply voltages. Moreover, switching threshold is the point where both the transistors (NMOS and PMOS) of CMOS inverter work in saturation region. Also at that point, it is assumed that the current in both the transistors is same.

The exact value of switching threshold has been calculated from Eq. (1). Where,$k_{p_{DMIG}}$ and $k_{n_{DMIG}}$ are the saturation point transconductance with device width of $W_p = 3$ μm, $W_n = 1$ μm for PMOS and NMOS, respectively, and calculated in similar manner as suggested in [35]. After solving, it is clear that the theoretical value of switching threshold is in a good agreement with the simulator. For the supply voltage of 1 V, $V_{m_{DMIG}(model)} = 0.445$ V, $V_{m_{DMIG}(simulated)} = 0.460$ V, and for $V_{dd} = 0.5$ V, $V_{m_{DMIG}(model)} = 0.216$ V, $V_{m_{DMIG}(simulated)} = 0.240$ V.

$$V_{m_{DMIG}} = \frac{V_{tn_{DMIG}} + \left(\sqrt[2]{\frac{k_{PDMIG}}{k_{n_{DMIG}}}} \times \left(V_{dd} + V_{tp_{DMIG}}\right)\right)}{\left(1 + \sqrt[2]{\frac{k_{PDMIG}}{k_{n_{DMIG}}}}\right)} \quad (1)$$

The impact of BOX variation on the VTC of DMIG FD SOI MOSFET has been shown in Fig. 16. It is found that the variation in BOX thickness have significant impact on circuit

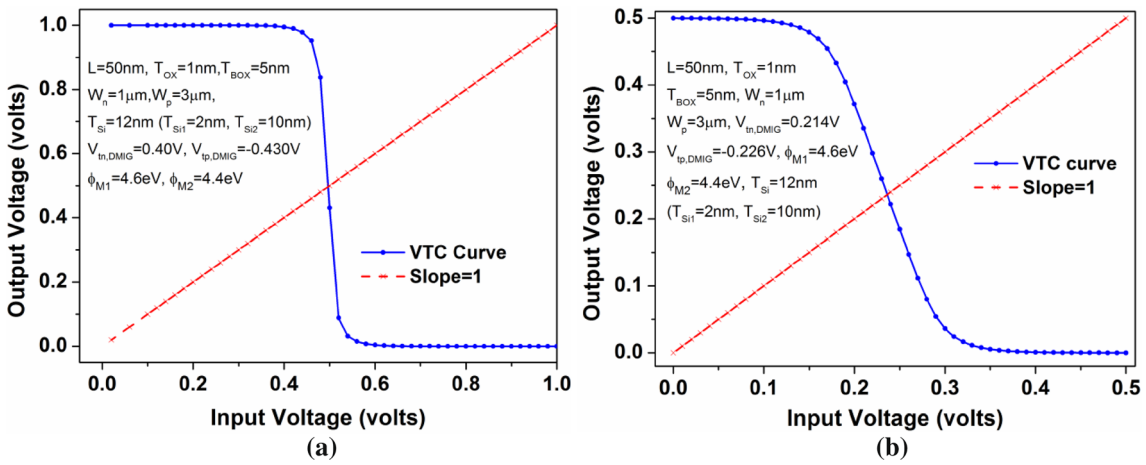

Fig. 15 VTC of individual Inverter designed with DMIG FD SOI MOSFET: **a** at supply voltage = 1 V, **b** at supply voltage = 0.5 V

performance. As the BOX thickness has been increased from 5 to 10 nm, the circuit resembles almost same VTC. However, as the BOX thickness is made 20 nm, the VTC take a shift towards right. This will affect the noise margin level of the circuit.

4.2 Noise margins (NMs)

The amount of noise that a circuit can tolerate is regarded as the noise margin (NM). Beyond this, the logic circuit could not work properly, even reliability issue takes place. So, it is necessary to make the NMs as high as possible. However, very high NMs results in large voltage excursions that leads to larger delay and more power dissipation. It is, therefore, necessary to maintain a trade-off among NMs, delay and power. The calculation of different NMs has been done on the basis of Eqs. (2 and 3). Where $NM_{l_{DMIG}}$ and $NM_{H_{DMIG}}$ are low and high NMs, respectively. Further, $V_{IL_{DMIG}}$ and $V_{OL_{DMIG}}$ in Eq. (2) are low level input and output voltages, respectively, and $V_{IH_{DMIG}}$ is high level input and $V_{OH_{DMIG}}$ is high level output voltages in Eq. (3).

$$NM_{l_{DMIG}} = V_{IL_{DMIG}} - V_{OL_{DMIG}} \tag{2}$$

$$NM_{H_{DMIG}} = V_{OH_{DMIG}} - V_{IH_{DMIG}} \tag{3}$$

It is worth here to mention that the value of $V_{OL_{DMIG}}$ can be itself assumed as so low that tends to 0 and $V_{OH_{DMIG}}$ is equal to V_{dd}.

The respective values of NMs have been note down from the VTC curve shown in Fig. 15a. The mathematical expression for the calculation of $V_{IL_{DMIG}}$, $V_{IH_{DMIG}}$ in Eqs. (4 and 5) are taken from [35]. After calculations, the values are $V_{IL_{DMIG}}=0.402$ V (simulation: 0.430 V), $V_{IH_{DMIG}}=0.442$ V (simulation: 0.510 V), $V_{OL_{DMIG}}=0$ and $V_{OH_{DMIG}}=V_{DD}=1$ V.

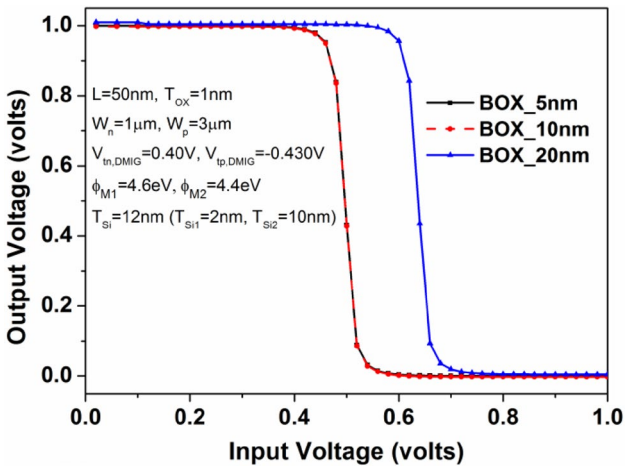

Fig. 16 VTC of individual Inverter designed with DMIG FD SOI MOSFET at different BOX oxide thickness

So, from Eqs. (2 and 3), $NM_{l_{DMIG}}$ and $NM_{H_{DMIG}}$ are 0.402 V (simulation: 0.430 V) and 0.558 V (simulation: 0.490 V), respectively.

$$V_{IL_{DMIG}} = \frac{2V_{out} + \frac{k_{n_{DMIG}}}{k_{P_{DMIG}}} \times V_{tn_{DMIG}} + V_{tp_{DMIG}} - V_{DD}}{\left(1 + \frac{k_{n_{DMIG}}}{k_{P_{DMIG}}}\right)} \tag{4}$$

$$V_{IH_{DMIG}} = \frac{V_{DD} + V_{tp_{DMIG}} + \frac{k_{n_{DMIG}}}{k_{P_{DMIG}}} \times \left(2V_{out} + V_{tn_{DMIG}}\right)}{\left(1 + \frac{k_{n_{DMIG}}}{k_{P_{DMIG}}}\right)} \tag{5}$$

$$\tau_{phl_{DMIG}} = \frac{C_L}{K_n\left(V_{DD} - V_{tn_{DMIG}}\right)}\left[\frac{2V_{tn_{DMIG}}}{\left(V_{DD} - V_{tn_{DMIG}}\right)} + \ln\left(\frac{4\left(V_{DD} - V_{tn_{DMIG}}\right)}{V_{DD}} - 1\right)\right] \tag{6}$$

$$\tau_{plh_{DMIG}} = \frac{C_L}{K_p\left(V_{DD} - \left|V_{tp_{DMIG}}\right|\right)}\left[\frac{2\left|V_{tp_{DMIG}}\right|}{\left(V_{DD} - \left|V_{tp_{DMIG}}\right|\right)} + \ln\left(\frac{4\left(V_{DD} - \left|V_{tp_{DMIG}}\right|\right)}{V_{DD}} - 1\right)\right] \tag{7}$$

$$\tau_{p_{DMIG}} = \frac{\tau_{phl_{DMIG}} + \tau_{plh_{DMIG}}}{2} \tag{8}$$

4.3 Transient analysis

The transient analysis of the proposed inverter circuit has been discussed here on the basis of propagation delays. Both the dynamic power dissipation and frequency/speed is affected by the propagation delay. So, the timing analysis is of the main concern for IC designers. Propagation delay is defined as the time required in a circuit to produce an output as soon as the input is applied. Basically, propagation delay of CMOS inverter is the average of two types of propagation delays that must be encountered to study the timing constraints of the proposed circuit. These delays depend on the transition from low to high and vice versa. The first one is $\tau_{phl_{DMIG}}$,which is calculated on the basis of transition from high to low (1–0), and for low to high (0–1) transition, $\tau_{plh_{DMIG}}$ is considered.

By definition, $\tau_{phl_{DMIG}}$ is the time delay between the $V_{50\%}$-transition of the rising input voltage and $V_{50\%}$-transition of the falling output voltage [35]. Similarly, $\tau_{plh_{DMIG}}$ is the time

delay between the $V_{50\%}$-transition of the falling input voltage and $V_{50\%}$-transition of the rising output voltage. Moreover, in Fig. 17, we have mentioned $\tau_{phl_{DMIG}}$ and $\tau_{plh_{DMIG}}$, as these are responsible for delay in high–low transition and low–high transition, respectively.

The calculation of these delays has been governed here on the basis of simulation result shown in Fig. 17 and verified against the model as per Eqs. (6 and 7) [35]. Moreover, overall delay is being approximated as $\tau_{p_{DMIG}}$ from Eq. (8), which is average of $\tau_{plh_{DMIG}}$ and $\tau_{phl_{DMIG}}$. It is clear from Fig. 17 that the proposed inverter offers almost negligible delay. The individual delay stage calculations at different channel length for fixed BOX thickness (5 nm) is listed in Table 7. One can find from Table 7 that lesser delay is seen at channel length of 50 nm, and also there is further scope of channel length scaling as lower delay recorded at scaled dimensions. Additionally, the mathematical results are found in good agreement with the numerical simulations. The electrical performance parameters and inverter stage delay of proposed MOS structure have also been compared and contrasted with the available state-of-the-arts and presented in Table 8. It is clear from the table that the proposed device offers excellent performance than others [36, 37].

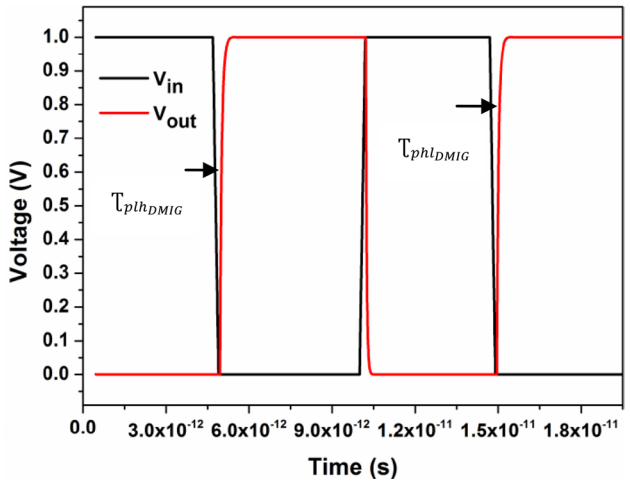

Fig. 17 Transient analysis of the proposed DMIG FD SOI MOSFET at 50 nm channel length

4.4 Power dissipation

Power dissipation ($P_{D_{DMIG}}$) is the main concern of today's high density ICs. For a CMOS inverter, it is calculated as the sum of static and dynamic power consumption. The associated off-state leakage in the devices is responsible for static power consumption. Moreover, the charging and discharging of capacitor in working condition at load is responsible for dynamic power dissipation. This can be formulated as in Eq. (9). The first part of this equation is due to static power dissipation and second part is due to dynamic.

$$V_{dd}I_{leak_{DMIG}} + \alpha C_L V_{dd}^2 f_{out_{DMIG}} \tag{9}$$

where $I_{leak_{DMIG}}$ is the off-state leakage of the studied DMIG device, α is the switching activity factor of CMOS inverter and assumed as 1, and $f_{out_{DMIG}}$ is output signal frequency. The output load capacitance of individual inverter delay stage is termed as C_L ($C_L = C_{L1} = C_{L2} = C_{L3}$) and is taken as 3.25 fF as per the discussion in Sect. 4.1. It is worth here to mention that as $I_{leak_{DMIG}}$ is affected with the channel length scaling and buried oxide thickness, and $f_{out_{DMIG}}$ will depend upon the threshold voltage of operation. So, the power dissipation will become a crucial factor for device designers in current trends of nanometers scaling.

Here for the analysis, power dissipation for the variation in channel length at different buried oxide thickness is shown in Fig. 18. One can observe from Fig. 18 that as the channel length is increased from 30 to 50 nm, the power consumption is getting reduced. This explains the similar scaling performance constraints as discussed in previous Sect. 3. As the increment in channel length will automatically

Table 8 Comparison of electrical performance parameters and inverter delay of different MOSFETs

References	L (nm)	I_{on}/I_{off}	Subthreshold-slope (mV/decade)	Inverter delay (ps)
FD SOI [36]	50	10^{10}	77	15
AM-CGAA-MOSFET [37]	50	10^5	62	3.225
Proposed	50	10^{11}	62	1.98

Table 7 Individual inverter stage delay at different channel length for BOX oxide thickness of 5 nm at $V_{dd} = 1$ V

Channel length (nm)	Simulated (ps)			Calculated (ps)		
	$\tau_{phl_{DMIG}}$	$\tau_{plh_{DMIG}}$	$\tau_{p_{DMIG}}$	$\tau_{phl_{DMIG}}$	$\tau_{plh_{DMIG}}$	$\tau_{p_{DMIG}}$
50	1.81	2.15	1.98	1.80	2.13	1.96
40	1.70	1.91	1.80	1.54	1.89	1.71
30	1.52	1.76	1.64	1.41	1.76	1.58

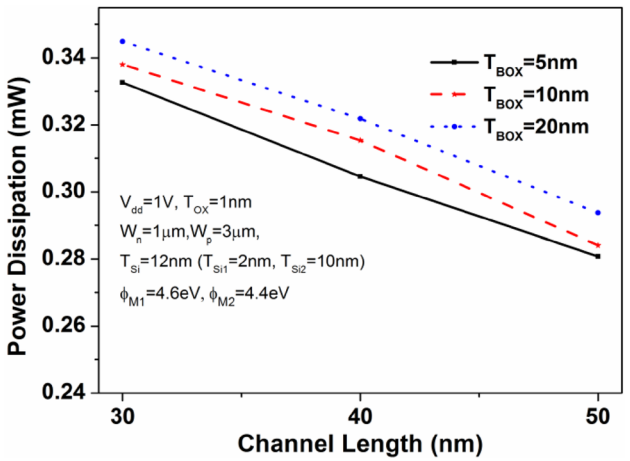

Fig. 18 Power dissipation of individual inverter stage at different BOX thickness with variation in channel length for $V_{dd} = 1$ V

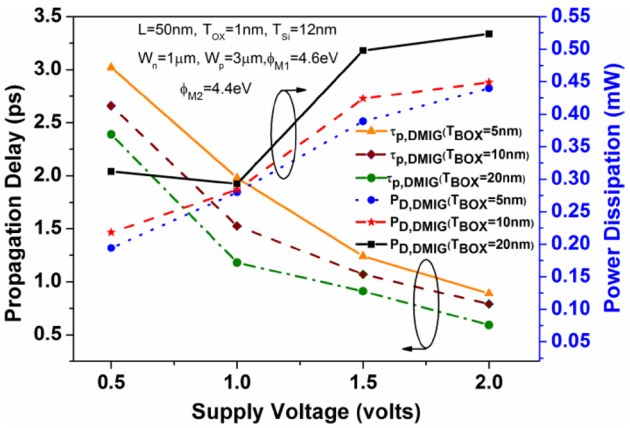

Fig. 19 Propagation delay and power dissipation at different supply voltage of operation at $L = 50$ nm

result in lesser off-state leakage and hence reduced power consumption.

Moreover, the drive current and frequency of output signal will vary with buried oxide thickness at fixed channel length and will increase power consumption further. However, the designed CMOS inverter is offering lesser power dissipation as compare to [38]. From, Fig. 19, as the supply voltage is increment from 0.5 to 2 V, propagation delay decreases, and also follows the proportional relationship with BOX thickness variation. However, power dissipation increments at higher V_{DD}, and also increases as the BOX thickness varied from 5 to 20 nm.

4.5 Oscillation frequency of ring oscillator

In this section, the oscillation frequency (f_{osc}) of the proposed ring oscillator circuit has been calculated on the basis of Eq. (10). Where, $\tau_{P_{DMIG}}$ indicates the propagation delay of individual inverter stage and N is the number of inverter stages.

$$f_{osc} = \frac{1}{2N\tau_{P_{DMIG}}} \tag{10}$$

where N is the total no of stages.

Here, three stages of identical inverters have been taken for the design of ring oscillator circuit. So, same delay is considered as per the Eq. (9) for all three inverter stages. The calculation of f_{osc} for the different channel length is listed in Table 9. It has been found that the ring oscillator circuit operates in GHz frequency range and as the channel length is getting reduced, oscillation frequency increases. This happens due to increment in drive current of the studied device at lower channel length. This ultimately dictates the significance of the scaling of MOSFETs in nano-scaled regime. Also the proposed device is in good agreement with analytical results with maximum deviation of 4–10%.

However, in literature, very few have discussed the circuit analysis of the nano-scaled devices. Table 10 represents the comparison of oscillation frequency for studied ring oscillator circuit with available state-of-arts. It is found that the proposed device offers comparable oscillation frequency.

Table 9 Oscillation frequency of 3-stage ring oscillator at different channel length for BOX oxide thickness of 5 nm

Channel length (nm)	Oscillation frequency	
	Simulated (GHz)	Calculated (GHz)
50	84.18	85.03
40	92.50	97.46
30	101.62	105.48

Table 10 Comparison of proposed ring oscillator circuit with available state-of-the-arts normalized for 3-stage design

References	Device for ring oscillator	Oscillation frequency (GHz)
[39]	FinFET (3-stage)	97.58
[40]	DG MOSFET (3-stage)	42.60
[41]	CMOS (3-stage)	41.10
[42]	IDUDGMOSFET (3-stage)	86.40
Proposed	DMIG SE FD SOI ($L = 50$ nm)	84.18
	DMIG SE FD SOI ($L = 40$ nm)	92.50
	DMIG SE FD SOI ($L = 30$ nm)	101.62

5 Conclusion

This paper presents the comprehensive analysis of ring oscillator circuit designed with nano-scaled SOI MOSFETs based CMOS inverter for low power high density ICs. For this, first the impact of DMIG technique on the performance of source engineered FD SOI MOSFET has been taken under study. It has been found that the proposed device is performing at low power and successfully accommodating the SCEs as compared to other devices at this node. The proposed structure exhibits a step-like potential profile with its minima very close to the source side of the channel and results in the lesser DIBL. In addition to this, the channel electron concentration is found uniform below insulator gap and results in better conduction current density. Additionally, the proposed device offers off-state leakage of 0.125 fA, which is quite enough to off-flow the leakage during switch-off condition in a circuit, and the drive current of 2.03 mA at optimized BOX thickness of 5 nm for 50 nm channel length. Hence, the switching ratio in order of 10^{11} suggests that the device could be analysed for high speed applications. Further, the designed CMOS inverter's VTC characteristics signifies that the proposed inverter can be utilized for high density ICs with enhanced thermal stability as the high to low transition is almost centred around $V_{dd}/2$. Additionally, the studied inverter follows the supply voltage scaling trends significantly with high noise margin. The power dissipation for the designed inverter circuit is found as 0.280 mW at $T_{BOX} = 5$ nm and $L = 50$ nm. In continuation, the designed ring oscillator is offering individual inverter delay of 1.98 ps at $T_{BOX} = 5$ nm and $L = 50$ nm, which is almost 86.80% and 38.60% lower as calculated in [36, 37], respectively. Additionally, the oscillation frequency is calculated as 84.18 GHz, 92.50 GHz and 101.62 GHz at $L = 50$ nm, 40 nm, and 30 nm, respectively. These results itself explain the significance of the studied device in the design of these circuits. So, the studied nano-scaled device could be suggested for the design of high density ICs in low power and high performance applications.

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References

1. H.R. Erfani-Jazi, N. Ghaderi, A divider-less, high speed and wide locking range phase locked loop. Int. J Electron. Commun. AEU **69**, 722–729 (2015). https://doi.org/10.1016/j.aeue.2014.12.015
2. A.E. Oualkadi, J.-M. Paillot, H. Guegnaud, R. Allam, CMOS RF switched capacitor bandpass filter tuned by ring VCO. Int. J. Electron. Commun. AEU **59**, 352–358 (2005). https://doi.org/10.1016/j.aeue.2004.11.008
3. S. Ahmad, N. Alam, M. Hasan, Robust TFET SRAM cell for ultra-low power IoT applications Int. J Electron. Commun. AEU **89**, 70–76 (2018). https://doi.org/10.1016/j.aeue.2018.03.029
4. N. Gupta, R. Chaujar, Influence of gate metal engineering on small signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. Appl. Phys. A **122**(8), 717 (2016). https://doi.org/10.1007/s00339-016-0239-9
5. W.H. Krautschneider, A. Kohlhase, H. Terletzki, Scaling down and reliability problems of gigabit CMOS circuits. Microelectron. Reliab. **37**(1), 19–37 (1997). https://doi.org/10.1016/0026-2714(96)00236-3
6. K.L. Wang, W. Lynch, Scenarios of CMOS scaling. in 5th IEEE International Conference on Solid-State and IC Technology, pp. 12–16. (1997). https://doi.org/10.1109/icsict.1998.785772
7. M. Saremi, A. Afzali-Kusha, S. Mohammadi, Ground plane fin-shaped field transistor (GP-FinFET) for low leakage power circuits. Microelectron. Eng. **95**, 74–82 (2012). https://doi.org/10.1016/j.mee.2012.01.009
8. N. Trivedi, M. Kumar, S. Haldar, S.S. Deswal, M. Gupta, R.S. Gupta, Charge plasma technique based dopingless accumulation mode junctionless cylindrical surrounding gate MOSFET: analog performance improvement. Appl. Phys. A **123**, 564 (2017). https://doi.org/10.1007/s00339-017-1176-y
9. J.P. Colinge, *Silicon-on-Insulator Technology*, 2nd edn., Materials to VLSI (Kluwer Academic Publishers, Amsterdam, 1997). ISBN 978-1-4757-2611-4
10. U. Khan, B. Ghosh, M.W. Akram, A.K. Salimath, A comparative study of SELBOX-JLT and SOI-JLT. Appl. Phys. A **117**(4), 2281–2288 (2014). https://doi.org/10.1007/s00339-014-8661-3
11. K.K. Young, Short channel effect in fully depleted SOI MOSFETs. IEEE Tran. Electron. Dev. **36**(2), 399–401 (1989). https://doi.org/10.1109/16.19942
12. K. Suzuki, S. Pidin, Short channel single-gate SOI MOSFET model. IEEE Trans. Electron. Dev. **50**(5), 1297–1305 (2005). https://doi.org/10.1109/TED.2003.813450
13. Y. Nakajima, H. Tomita, K. Aoto, N. Ito, T. Hanajiri, T. Toyabe, T. Morikawa, T. Sugano, Characterization of trap states at silicon on-insulator (SOI)/Buried oxide (BOX) interface by back gate transconductance characteristics in SOI MOSFETs. Jpn. J. Appl. Phys. Regul. Rap. Short Notes **42**(4B), 2004–2008 (2003)
14. K. Cheng, A. Khakifirooz, Fully depleted SOI (FDSOI) technology. Sci. China Inf. Sci. **59**(061402), 1–15 (2016). https://doi.org/10.1007/s11432-016-5561-5
15. V.K. Mishra, R.K. Chauhan, Performance analysis of modified source and TDBC based fully-depleted SOI MOSFET for low power digital applications. J. Nano Optoelectron. **12**(1), 59–66 (2017). https://doi.org/10.1166/jno.2017.2000
16. N.A. Srivastava, V.K. Mishra, R.K. Chauhan, Analytical modelling of surface potential of modified source FD-SOI MOSFET. in IEEE International Conference on Emerging Trends in Communication Technologies (ETCT), pp. 1–4. (2016). https://doi.org/10.1109/etct.2016.7882990
17. S. Mukherjee, S. Roy, A. Dutta, C.K. Sarkar, Study of effect of back oxide thickness variation in FDSOI MOSFET on analogue circuit performance. IET Circ. Dev. Syst. **10**(6), 497–503 (2016). https://doi.org/10.1049/iet-cds.2016.0234
18. T. Ushiki, M. C. Yu, K. Kawai, T. Shinohara, K. Ino, M. Morita, T. Ohmi, Reduction of plasma-induced gate oxide using low-energy large-mass ion bombardment in gate-metal sputtering deposition. in Proceedings of International Reliability Physics Symposium, Reno, Nevada, pp. 307–11. (1998). https://doi.org/10.1109/relphy.1998.670661

19. J.P. Colinge, Multi-gate SOI MOSFETs. microelectronics. Engineering **84**(9–10), 2071–2076 (2007). https://doi.org/10.1016/j.mee.2007.04.038
20. M.J. Kumar, A. Chaudhary, Two dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. IEEE Trans. Electron. Dev. **51**(4), 569–574 (2004). https://doi.org/10.1109/TED.2004.823803
21. A. Priya, R.A. Mishra, A two dimensional analytical modeling of surface potential in triple metal gate (TMG) fully-depleted recessed-source/drain (Re-S/D) SOI MOSFET. Superlattice Microstruct. **92**, 316–329 (2016)
22. Y.C. Yeo, Metal gate technology for nanoscale transistors-material selection and process integration issues. Thin Solid Films **462–463**, 34–41 (2004). https://doi.org/10.1016/j.tsf.2004.05.039
23. S. Wei, G. Zhang, Z. Shao, L. Geng, C.-F. Yang, Analysis of a high-performance ultra-thin box silicon-on-insulator MOSFET with the lateral dual-gates: featuring the suppression of DIBL. Microsyst. Technol. **3**, 150 (2017). https://doi.org/10.1007/s00542-017-3532-4
24. W.-J. Cho, C.-G. Ahn, K. Im, J.-H. Yang, J. Oh, I.-B. Baek, S. Lee, Fabrication of 50-nm gate SOI n-MOSFETs using novel plasma-doping technique. IEEE Electron. Dev. Lett. **25**(6), 366–368 (2003). https://doi.org/10.1109/led.2004.829007
25. J. Luo, J. Chen, Q. Wu, Z. Chai, T. Yu, X. Wang, TDBC SOI technology to suppress floating body effect in PD SOI p-MOSFETs. IEEE Electron. Lett. **48**(11), 652–653 (2012)
26. C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, F. Andrieu, L. Tosti, S. Barnola, T. Salvetat, X. Garros, M. Cassé, F. Allain, N. Loubet, L. Pham-Nguyen, E. Deloffre, M. Gros-Jean, R. Beneyton, C. Laviron, M. Marin, C. Leyris, S. Haendler, F. Leverd, P. Gouraud, P. Scheiblin, L. Clement, R. Pantel, S. Deleonibus, T. Skotnicki, FDSOI devices with thin BOX and ground plane integration for 32 nm node and below. Solid State Electron. **53**, 730–734 (2009). https://doi.org/10.1016/j.sse.2009.02.009
27. W. Long, H. Ou, J.M. Kuo, K.K. Chin, Dual-material gate (DMG) field effect transistor. IEEE Trans. Electron. Dev. **46**(5), 865–870 (1999). https://doi.org/10.1109/16.760391
28. R. Narang, K.V.S. Reddy, M. Saxena, R.S. Gupta, M. Gupta, A dielectric-modulated tunnel-FET-based biosensor for label-free detection: analytical modeling study and sensitivity analysis. IEEE Trans. Electron. Dev. **59**(10), 2809–2817 (2012). https://doi.org/10.1109/ted.2012.2208115
29. J.H. Ahn, J.Y. Kim, M. Im, J.W. Han, Y.K. Choi, A nanogap-embedded nanowire field effect transistor for sensor applications: Immunosensor and humidity sensor. In Proceedings of 14th International Conference on Miniaturized Systems for Chemistry and Life Sciences, pp. 1301–1303 (2010)
30. M. Im, J.H. Ahn, J.W. Han, T.J. Park, S.Y. Lee, Y.K. Choi, Development of a point-of-care testing platform with a nanogap-embedded separated double-gate field effect transistor array and its readout system for detection of avian influenza. IEEE Sens. J. **11**(2), 351–360 (2011). https://doi.org/10.1109/JSEN.2010.2062502
31. Silvaco Int, *Atlas User's Manual* (Silvaco Int, Santa Clara, 2015)
32. W. Yeh, C. Lin, T. Chou, K. Wu, J. Yuan, The impact of junction doping distribution on device performance variability and reliability for fully depleted silicon on insulator with thin box layer MOSFETs. IEEE Trans Nanotechnol. **12**(2), 330–337 (2015). https://doi.org/10.1109/TNANO.2015.2394247
33. V.K. Mishra, R.K. Chauhan, Area efficient layout design of CMOS circuit for high-density ICs. Int. J. Electron. **105**(1), 73–87 (2017). https://doi.org/10.1080/00207217.2017.1340978
34. S. Roy, S. Mukherjee, A. Dutta, C.K. Sarkar, Effect of back oxide thickness of FDSOI on SRAM performance. Superlattice Microstruct. **98**, 316–324 (2016)
35. S.-M. Kang, Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design* (McGraw-Hill, New York, 2003)
36. A. Vandooren, S. Egley, M. Zavala, T. Stephens, L. Mathew, M. Rossow, A. Thean, A. Barr, Z. Shi, T. White, D. Pham, J. Conner, L. Prabhu, D. Triyoso, J. Schaeffer, D. Roan, B.-Y. Nguyen, M. Orlowski, J. Mogab, 50 nm Fully depleted SOI CMOS technology with HfO_2 gate dielectric and TiN gate. IEEE Trans. Nanotechnol. **4**(2), 324–328 (2003). https://doi.org/10.1109/TNANO.2003.820502
37. S.R. Panda, Device and circuit performance of Si-based accumulation mode CGAA CMOS inverter. Mater. Sci. Semicond. Process. **66**, 87–91 (2017)
38. D. Bianchi, F. Quaglia, A. Mazzanti, F. Svelto, Analysis and design of a high voltage integrated class-B amplifier for ultrasound transducers. IEEE Trans. Circ. Syst. I **61**(7), 1942–1951 (2014). **Regular Papers**
39. N. Collaert, A. Dixit, M. Goodwin, K.G. Anil, R. Rooyackers, B. Degroote, L.H.A. Leunissen, A. Veloso, R. Jonckheere, K.D. Meyer, M. Jurczak, S. Biesemans, A functional 41-stage ring oscillator using scaled FinFET devices with 25-nm gate lengths and 10-nm fin widths applicable for the 45-nm CMOS node. IEEE Electron. Dev. Lett. **25**(8), 568–570 (2004)
40. S.K.A. Kulkarni, A novel voltage-controlled ring oscillator based on nanoscale DG-MOSFETs. in IEEE International Conference on Microelectronics, pp. 417–420 (2008)
41. R.C. Shah, M. Abdullah, Optimal design of ring oscillator and differential LC using 45 nm CMOS technology. Int. J. Innov. Res. Sci. Technol. **2**(10), 1–5 (2016)
42. S. Mukherjee, S. Roy, K. Koley, A. Dutta, C.K. Sarkar, Design and study of programmable ring oscillator using IDUDGMOSFET. Solid State Electron. **117**, 193–198 (2016)