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Temperature and SiO_2/4H-SiC interface trap effects on the electrical characteristics of low breakdown voltage MOSFETs

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Abstract
The temperature and carrier-trapping effects on the electrical characteristics of a 4H silicon carbide (4H-SiC) metal–oxide–semiconductor field effect transistor (MOSFET) dimensioned for a low breakdown voltage (BV_{DS}) are investigated. Firstly, the impact of the temperature is evaluated referring to a fresh device (defects-free). In particular, the threshold voltage (V_{th}), channel mobility (μ_{ch}), and on-state resistance (R_{ON}) are calculated in the temperature range of 300 K to 500 K starting from the device current–voltage characteristics. A defective MOSFET is then considered. A combined model of defect energy levels inside the 4H-SiC bandgap (deep and tail centers) and oxide-fixed traps is taken into account referring to literature data. The simulation results show that the SiO_2/4H-SiC interface traps act to increase R_{ON}, reduce μ_{ch}, and increase the sensitivity of V_{th} with temperature. In more detail, the deep-level traps in the mid-gap have a limited effect in determining R_{ON} once the tail traps contributions have been introduced. Also, for gate biases greater than about $2V_{th}$ (i.e., $V_{GS} > 12$ V) the increase of mobile carriers in the inversion layer leads to an increased screening of traps which enhances the MOSFET output current limiting the R_{ON} increase in particular at low temperatures. Finally, a high oxide-fixed trap density meaningfully influences V_{th} (negative shifting) and penalizes the device drain current over the whole explored voltage range.

1 Introduction

Metal–oxide–semiconductor field effect transistors (MOSFETs) in silicon carbide (SiC) are very attractive devices in modern power electronics [1]. They are widely appreciated for their high efficiency, low on-state resistance (R_{ON}), and noticeable switching capabilities. Typical SiC MOSFETs are designed to support high blocking voltages (BV_{DS}) ranging from 600 to 1700 V [2–4]. Recent papers, however, have also investigated low breakdown voltage 4H-SiC MOSFETs to be used for photovoltaic (PV) module-level applications enabling operation in harsh conditions with considerable lifetime [5–10]. Power optimizers in PV modules are generally rated for voltages in the order of 100–200 V.

The main technological issue of an SiC-based MOSFET is the effective quality of the silicon oxide (SiO_2) interface that could make the device much less efficient. Defects occurring at the SiO_2/4H-SiC interface, in fact, heavily affect the device current capability [11–14]. In more detail, the interface trap effects tend to decrease the carrier mobility in the channel region through the enhanced scattering mechanisms of free carriers. At the same time, traps increase the R_{ON} value and the sensitivity of the threshold voltage (V_{th}) with temperature.

In this context, the aim of the paper is to investigate, by means of a careful numerical simulation study, the electrical characteristics of a 4H-SiC MOSFET designed for low-voltage ratings ($BV_{DS} = 150$ V) over a wide range of temperatures. Without loss of generality with respect to different designs dimensioned for higher blocking voltages, explicit interface trap effects due to a detailed density of states in the inversion region and a fixed trap density in the oxide are considered referring to literature data. A preliminary study at room temperature, which neglects defect and trap effects, was presented in Refs. [5, 6] emphasizing the use of fast and rugged 100-V-class switches.

The obtained results clarify the role of interface traps in reducing carrier mobility in the channel region (μ_{ch}). Also, V_{th} decreases as a function of both trap density and temperature. In particular, a high oxide-fixed trap density

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meaningfully influences V_{th}. Finally, this analysis indicates that deep-level traps at the 4H-SiC interface have only a limited effect in determining the MOSFET R_{ON} once the tail traps contributions have been introduced. The R_{ON} value is 200 kΩ μm^2 for a defective device at $V_{GS}=10$ V, $V_{DS}=1$ V, and $T=300$ K. This result is compared to the state-of-the-art of a commercial Si-MOSFET with the same BV_{DS} supporting the opportunity to explore the use of 4H-SiC also for low-voltage applications where efficiency, robustness, miniaturization, and temperature control are critical targets.

2 MOSFET structure

The schematic cross-section of the considered vertical n-channel 4H-SiC MOSFET single-cell is shown in Fig. 1. The different geometrical parameters are labeled as follows: W_{cell} is the cell width, W_G is the gate contact width, L_{ch} is the device channel length, W_J is the distance between the base regions, X_{N+} is the n+-source junction depth, X_P is the p-base junction depth, W_{drift} is the n-drift region thickness, W'_{drift} is the base-to-substrate distance, and W_{sub} is the starting substrate thickness. The source contact shorts the source and base regions to prevent the switch-on of the parasitic substrate(n$^+$)–epilayer(n)–base(p)–source(n$^+$) bipolar junction transistor. The reference geometrical and doping parameters used during the simulations are summarized in Table 1.

From Table 1, the distance between the n$^+$-source region and the n-epilayer (i.e., X_P–X_{N+}) is 0.8 μm. The epilayer thickness ensures a BV_{DS} value close to 150 V.

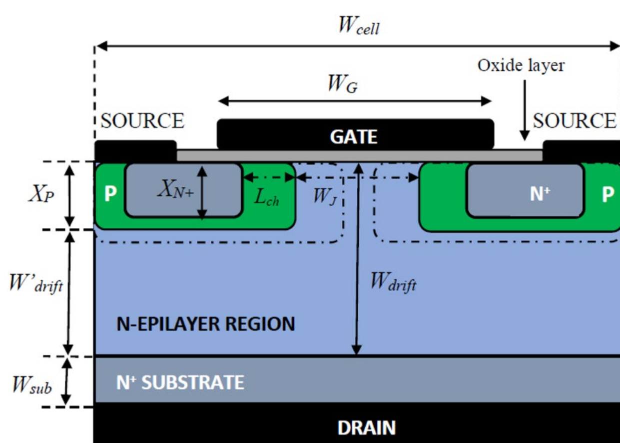

Fig. 1 Cross-sectional view of the n-channel 4H-SiC MOSFET single-cell. The drawing is not to scale

Table 1 MOSFET reference parameters (Fig. 1)

Design parameters	Values
Silicon oxide thickness, t_{ox} (μm)	0.08
Source thickness, X_{N+} (μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_P (μm)	1.3
Base-to-base distance, W_J (μm)	7
Epilayer thickness, W_{drift} (μm)	1.8
Base-to-substrate distance, W'_{drift} (μm)	0.5
Substrate thickness, W_{sub} (μm)	100
Gate contact width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
N$^+$-source doping, N_D (cm^{-3})	1×10^{18}
P-base doping, N_A (cm^{-3})	1×10^{17}
N-drift doping, N_{drift} (cm^{-3})	3×10^{15}
N$^+$-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

Although simplified for simulation purposes, the proposed structure is in principle compatible with a manufacturing process based on doping by ion implantation [15–17].

3 Physical models

The numerical simulation analysis was performed using the Atlas-Silvaco TCAD physical simulator [18]. The device structure was fine meshed wherever appropriate and in particular around the p–n junctions and the surface channel region under the SiO_2/4H-SiC interface. The total number of mesh points was about 32,000 and the mesh spacing was scaled down to 0.5 nm at the interfaces.

The key physical models taken into account include the material bandgap temperature dependence, apparent bandgap narrowing effect, Auger and Shockley–Read–Hall recombination phenomena, incomplete doping activation, impact ionization, and carrier lifetime and carrier mobility expressions depending on temperature and doping concentration [19–24]. Moreover, Fermi–Dirac statistics and multidimensional dependent anisotropic effects as well as scattering mechanisms that degrade the channel mobility were considered during the simulations.

Parameters details about the simulation setup for 4H-SiC-based devices are reported in recent manuscripts of ours where the models prediction capabilities are also supported by experimental results obtained on implanted diodes over wide ranges of current and temperature [25–30].

In this paper, to address the defect and trap effects at the SiO_2/4H-SiC interface, we solve Poisson's equation in the channel region in the form

$$\nabla \cdot (\varepsilon \nabla \Psi) = q\left(n - p - N_D^+ + N_A^-\right) - Q_T, \quad (1)$$

where an overall trapped charge contribution Q_T is considered in addition to the ionized donor (N_D^+) and acceptor (N_A^-) impurity concentrations to describe the variation of the electrostatic potential ψ with the local (total) charge density.

According to [31], the incomplete ionization of impurities is given by

$$N_{A,D}^{-,+} = N_{A,D}\left(\frac{-1 + \sqrt{1 + 4g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{E_{A,D}}{kT}}}}{2g_{v,c}\frac{N_{A,D}}{N_{V,C}(T)}e^{\frac{E_{A,D}}{kT}}}\right), \quad (2)$$

where N_D and N_A are the substitutional n-type and p-type doping concentrations, N_C and N_V are the electron and hole density of states varying with temperature, $g_c = 2$ and $g_v = 4$ are the degeneracy factors of the conduction and valence band, and $E_D = 100$ meV and $E_A = 200$ meV are the donor and acceptor energy levels assuming nitrogen and aluminum as doping species, respectively.

The interface density of states (DoS) in the 4H-SiC inversion layer is modeled by the following expression [32, 33]:

$$D_{it}(E) = D_{it,T} + D_{it,M}, \quad (3)$$

where $D_{it,M}$ is a Gaussian distribution of deep states in the mid-gap and $D_{it,T}$ is the sum of two exponentially decaying band tail states close to the conduction and valence band-edges, respectively. In more detail, we can write

$$D_{it,T} = D^0_{t,TC}\exp^{[(E-E_C)/U_C]} + D^0_{t,TV}\exp^{[(E_V-E)/U_V]}, \quad (4)$$

$$D_{it,M} = D^0_{t,M}\exp^{[(E-E_M)/W_M]^2}, \quad (5)$$

where E_C and E_V are the conduction and valence band energies, U_C and U_V are characteristic energy decays, $D^0_{t,TC}$ and $D^0_{t,TV}$ are the band edge intercept densities, W_M takes into accounts the spectral width of the mid-gap Gaussian distribution, and E_M is the energy value of the defect density peak $D^0_{t,M}$.

In Eq. (3) each term acts either as donor-like or acceptor-like level for free carriers [18]. In other words, a donor-like center is positively charged (ionized) when empty and neutral when filled (with an electron), while an acceptor-like center is negatively charged (ionized) when filled and becomes neutral when empty.

The total charge Q_t is therefore expressed by

$$Q_t = q(D^+_{it,D} - D^-_{it,A}), \quad (6)$$

where referring to the terms $D_{it,M}$ and $D_{it,T}$ introduced above, $D^+_{it,D}$ and $D^-_{it,A}$ are the ionized densities for donor-like and acceptor-like traps, respectively. In particular, each ionized density depends upon the trap density and the relative probability of ionization that is in the form of

$$F_{t,D} = \frac{v_{th}\sigma_n + e_p}{v_n(\sigma_p + \sigma_n) + (e_n + e_p)}, \quad (7)$$

$$F_{t,A} = \frac{v_{th}\sigma_p + e_n}{v_p(\sigma_p + \sigma_n) + (e_n + e_p)}. \quad (8)$$

Here, v_n and v_p are the carrier thermal velocities, and σ_n and σ_p are the trap capture cross sections for electrons and holes, respectively. Finally, e_n and e_p are the trap emission rates given by

$$e_n = v_n\sigma_n n_i \exp\left(\frac{E - E_i}{kT}\right), \quad (9)$$

$$e_p = v_p\sigma_p n_i \exp\left(\frac{E_i - E}{kT}\right), \quad (10)$$

where E_i is the intrinsic Fermi level and n_i is the intrinsic carrier concentration.

The fundamental DoS parameters used during the simulations are listed in Table 2 [18, 33, 34]. In particular, the trap density reference values are assumed as in Ref. [33].

Finally, the Caughey–Thomas expression describes the temperature-dependent carrier mobility as

$$\mu_{n,p} = \mu^{\min}_{0n,p}\left(\frac{T}{300}\right)^{\alpha_{n,p}} + \frac{\mu^{\max}_{0n,p}\left(\frac{T}{300}\right)^{\beta_{n,p}} - \mu^{\min}_{0n,p}\left(\frac{T}{300}\right)^{\alpha_{n,p}}}{1 + \left(\frac{T}{300}\right)^{\gamma_{n,p}}\left(\frac{N}{N^{crit}_{n,p}}\right)^{\delta_{n,p}}}, \quad (11)$$

where the $\mu_{0n,p}$ terms are the carrier mobilities assumed at room temperature, N is the local doping concentration, $N^{crit}_{n,p}$ is the doping concentration at which the mobility is halfway between its maximum and minimum value, and α, β, γ, and δ are process-dependent coefficients [35]. This model was experimentally validated for SiC in Ref. [36].

Table 2 DoS parameters

Parameters	Band tail states	Mid-gap states
Energy level (eV)	0.47	1.55
Density (cm^{-2} eV^{-1})	6×10^{13}	2.3×10^{11}
$U_{C,V}$ (eV)	0.01, 0.23	–
W_M (eV)	–	0.1
$\sigma_{n,p}$ (cm^2)	1×10^{-16}, 1×10^{-14}	1×10^{-16}, 1×10^{-14}
$v_{n,p}$ (cm/s)	1.9×10^{7}, 1.2×10^{7}	1.9×10^{7}, 1.2×10^{7}

The expected mobility reduction due to the carrier saturated drift velocity ($v_{sat}=2\times10^7$ cm/s) was modeled for high electric fields by using

$$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1+\left(E\frac{\mu_{n,p}}{v_{sat}}\right)^{\kappa_{n,p}}\right]^{\frac{1}{\kappa_{n,p}}}}, \quad (12)$$

where E is the electric field in the direction of the current flow, and $\kappa_n=2$ and $\kappa_p=1$ [18]. In addition, mobility degradation effects that had taken place in the inversion layer can be written as

$$\mu_{n,p}(E_\perp) = \frac{\mu_{n,p}}{\sqrt{1+\frac{E_\perp}{E_{n,p}^{crit}}}}, \quad (13)$$

where $E_{n,p}^{crit}$ is an adjustable parameter, and $E_\perp$ is the perpendicular electric field component which originates different scattering mechanisms involving surface-phonons, surface-roughness, and Coulombic scattering [18].

4 Results and discussion

4.1 *I–V–T* characteristics in absence of trap effects

A first set of simulations was addressed to clarify the dependence of BV_{DS} on thickness (W_{drift}) and doping (N_{drift}) of the device epitaxial layer. In particular, with the MOSFET in off-state ($V_G=0$ and grounded source) V_{DS} was gradually increased until the drain leakage current density reached a maximum value of 10 mA/cm^2. Starting from $W_{drift}=10$ µm and $N_{drift}=1\times10^{16}$ cm^{-3}, we calculated BV_{DS} close to 900 V. This value corresponds to a critical electric field of 1.9 MV/cm. Then, W_{drift} was reduced down to 1.8 µm as summarized in Table 3. It must highlighted that BV_{DS} is strictly dependent on W_{drift} which in fact determines the effective distance W'_{drift} between the base junction and the substrate, i.e., $W_{drift} - X_P$ in Fig. 1.

By decreasing N_{drift} from 1×10^{16} cm^{-3} to 1×10^{15} cm^{-3} we observed a maximum reduction of BV_{DS} on the order of 10%. For example, for $N_{drift}=3\times10^{15}$ cm^{-3} we obtained $BV_{DS}=150$ V for $W_{drift}=1.8$ µm and $BV_{DS}=850$ V for $W_{drift}=10$ µm as in Ref. [6]. It is worth noting that N_{drift} has only a limited impact in determining BV_{DS} for $W_{drift}\leq3$ µm.

Table 3 BV_{DS} as a function of W_{drift} for $N_{drift}=1\times10^{16}$ cm^{-3}

BV_{DS} (V)	W_{drift} (µm)
900	10
750	7
600	5
350	3
200	2
155	1.8

The 4H-SiC MOSFET in Table 1 is a structure considered free of interface defects and traps (fresh device). The current density curves $I_D - V_{DS}$ and $I_D - V_{GS}$ calculated at different temperatures for the half-cell in Fig. 1 (active area 7.5 µm^2) are shown in Figs. 2 and 3, respectively.

As expected, the drain current decreases harshly when increasing temperature. This effect is determined by the temperature dependence of carrier mobility in the inversion layer and the overall increase of the device on-state resistance.

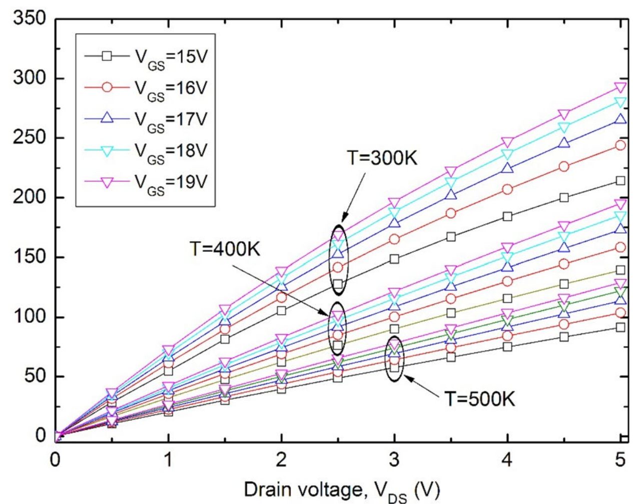

Fig. 2 Forward $I_D - V_{DS}$ characteristics for the device in Table 1 at $T=300$ K, $T=400$ K, and $T=500$ K

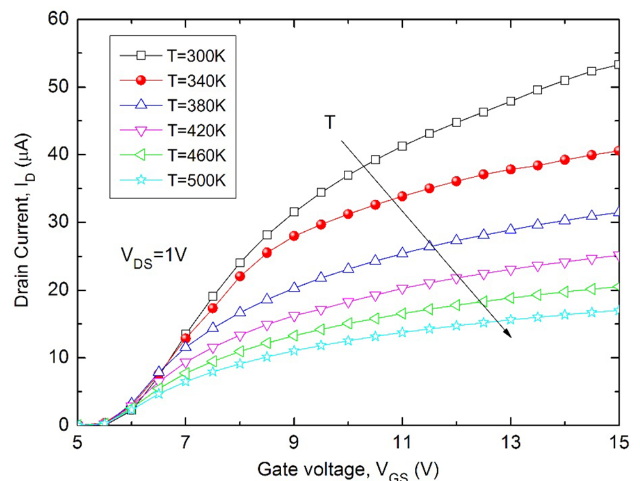

Fig. 3 $I_D - V_{GS}$ curves for the device in Table 1 at different temperatures

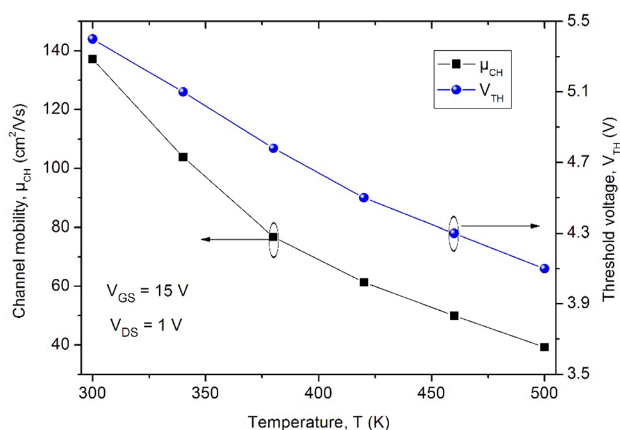

Fig. 4 Channel mobility and device threshold voltage as a function of the temperature

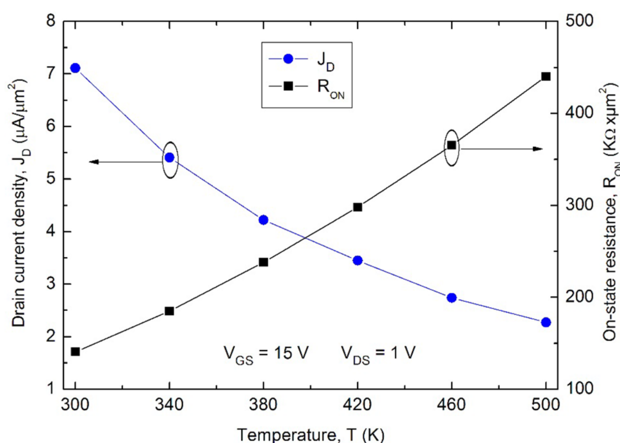

Fig. 5 On-state resistance and drain current density as a function of the temperature

In more detail, the degradation of the total carrier mobility behavior in the channel region is shown in Fig. 4. Here, the temperature dependence of the threshold voltage is also reported by imposing during the simulations a subthreshold current in the limit of 10 nA. The plot is traced by taking a cut-line of the device structure for $V_{GS} = 15$ V and $V_{DS} = 1$ V.

The decrease of V_{th} and μ_{ch} with temperature is due to the increase of the 4H-SiC intrinsic carrier concentration. These variations determine different values of the device transconductance which results 25 s at $T = 300$ K and decreases to about 10 s at $T = 500$ K in the considered range of V_{GS}.

From Fig. 3, the drain current density for $V_{GS} = 15$ V and $V_{DS} = 1$ V at $T = 300$ K is 7.11 μA/μm^2 ($I_D = 53.32$ μA). The corresponding MOSFET R_{ON} is therefore calculated as close to 140 kΩ μm^2. The R_{ON} behavior as a function of the temperature is shown in Fig. 5. Here, the R_{ON} increase with temperature is mainly due to the decrease of carrier mobility in the inversion layer as well as in the drift region [37]. In other words, the increased temperature limits the current components in these two regions.

4.2 Analysis of trap effects at the SiO_2/4H-SiC interface

4.2.1 Tail traps

Introducing in the model a constant value of deep traps in the mid-gap, i.e., $D^0_{t,M} = 2.3 \times 10^{11}$ cm^{-2} eV^{-1} [33], Fig. 6 depicts the device $I_D - V_{GS}$ characteristics in semi-logarithmic scale calculated for a different band tail trap density at $T = 300$ K, $T = 400$ K, and $T = 500$ K. In particular, in Eq. (4) we have assumed the band edge intercept density in the range from 10^{12} cm^{-2} eV^{-1} to 10^{14} cm^{-2} eV^{-1} [33, 38]. In addition, it is important to note that the traps with energetic states close the valence band can be neglected once the contribution $D^0_{t,TC} \exp^{[(E-E_C)/U_C]}$ has been considered. In this study, in fact, when the device is forward biased, even in weak inversion condition, the Fermi level increasingly moves in the upper half of the bandgap.

From Fig. 6, similarly to the fresh device, V_{th} tends to decrease as the temperature increases. For $V_{GS} > V_{th}$, the saturated value of I_D is almost the same until the tail trap density is in the limit of 10^{13} cm^{-2} eV^{-1}. Then, for example for $D^0_{t,TC} = 10^{14}$ cm^{-2} eV^{-1}, the device current capabilities are meaningfully penalized at any V_{DS} bias level.

When a positive V_{GS} is applied, the acceptor defect states are able to trap a great number of electrons from the inversion layer, thus making them immobile and excluding them from carrier transport mechanisms. In addition, at each temperature, these filled traps cause Coulomb scattering phenomena of mobile charges that determine in turn a reduced drain current and a positive shift of the threshold voltage. The more the temperature increases, the more the number of filled traps decreases; hence V_{th} decreases as stated above.

The MOSFET R_{ON} behaviors as a function of V_{GS} for both a fresh and a defective device are shown in Fig. 7. The R_{ON} of a heavily defective device dramatically increases for increasing temperature in particular at low biases ($V_{GS} \leq 12$ V) as a consequence of the mobility degradation induced by traps [39]. For $V_{GS} > 12$ V, however, the increase of mobile carriers leads to an increased screening of traps which supports the MOSFET output current limiting the R_{ON} increase especially at low temperatures.

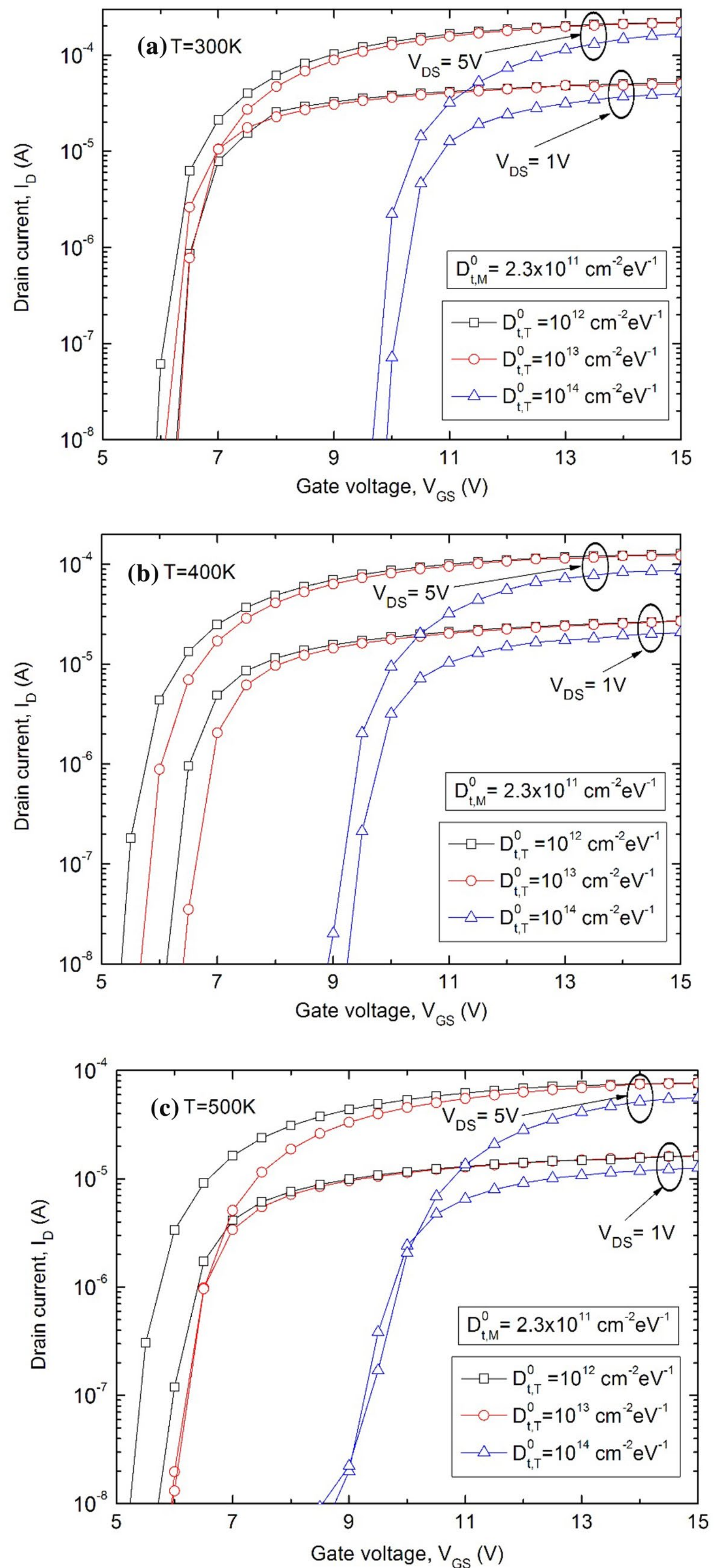

Fig. 6 $I_D - V_{GS}$ characteristics as a function of the tail trap density at **a** $T = 300$ K, **b** $T = 400$ K, and **c** $T = 500$ K

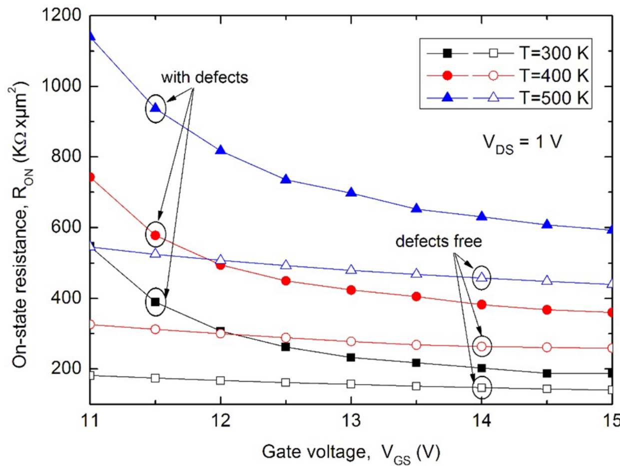

Fig. 7 R_{ON} as a function of V_{GS} at different temperatures for fresh (open symbols) and defective (solid symbols) device. $D^0_{t,T}=10^{14}$ cm^{-2} eV^{-1}, $D^0_{t,M}=2.3\times10^{11}$ cm^{-2} eV^{-1}

4.2.2 Deep-level traps

The MOSFET I_D-V_{GS} characteristics for two different distributions of deep-level traps (not exceeding a peak value of 10^{12} cm^{-2} eV^{-1} [38]) are shown in Fig. 8. A fixed band edge intercept density $D^0_{t,T}=10^{13}$ cm^{-2} eV^{-1} was assumed during the simulations.

In this case, the trap effects mostly occur at the beginning of the I_D curves determining, once again, an increase in the device threshold voltage. In other words, since the tail traps contribution has been introduced, the effect of the trapped charge in the deep-level traps on the slope of the I_D curves in Fig. 8 is negligible and, in fact, for $V_{GS}>10$ V the drain current appears not affected. This result is shown in more detail in Fig. 9 by plotting the R_{ON} behaviors as a function of V_{GS} at different temperature ($11\le V_{GS}\le15$ V).

4.2.3 Oxide-fixed traps

Moving from the developed analysis on the interface-trapped charges which are related to the defect energy levels inside the 4H-SiC bandgap, in order to determine the effective MOSFET current capability, in this section we have involved in the model an oxide-fixed trap effect as shown in Fig. 10. In particular, we have considered a thin film of fixed traps located in the oxide next to the SiO_2/4H-SiC interface with a charge density $N_{fix}=1.3\times10^{12}$ cm^{-2} [33].

The oxide-fixed traps, which have a density strictly dependent on the 4H-SiC surface oxidation process, became scattering centers that influence the device threshold voltage as shown in Fig. 11. Here, the carrier mobility degradation in the inversion layer is also reported.

From Fig. 11, it is clear that the MOSFET threshold voltage significantly decreases in presence of an explicit oxide-fixed trap density. These centers, in fact, by acting as positive charges produce a band bending at the semiconductor interface even without the application of a positive bias voltage at the gate contact [40, 41]. In other words, the band bending for a p-type MOSFET tends to induce a depletion region (channel region) before V_{GS} is applied. This effect obviously reduces V_{th} at any operation temperature. In addition, due to the Coulombic scattering [42], the effective carrier mobility in the inversion layer is degraded as well.

The comparison of the defective device in Fig. 10 ($D^0_{t,T}=10^{13}$ cm^{-2} eV^{-1}, $D^0_{t,M}=10^{12}$ cm^{-2} eV^{-1}, and $N_{fix}=1.3\times10^{12}$ cm^{-2}) and the fresh one in Fig. 3 in terms of R_{ON} at different temperatures is shown in Fig. 12.

Here, the datasheet value $R_{ON}=216$ kΩ μm^2 for a Si-based commercial MOSFET rated for 150 V at $V_{GS}=10$ V and $T=300$ K is also reported [43]. This value is slightly higher than that calculated for the proposed device at the same bias level, namely $R_{ON}=200$ kΩ μm^2. In presence of an oxide-fixed trap effect, the R_{ON} behavior tends to increase over the whole explored V_{GS} range in particular at the higher temperatures that increasingly contribute to limit the drain current.

5 Conclusion

The temperature and carrier-trapping effects on the electrical characteristics of a 4H-SiC MOSFET have been predicted by means of numerical simulations. A combined model of defect energy levels inside the 4H-SiC bandgap (tail and deep-level traps) and oxide-fixed traps has been considered. The trap densities have been assumed referring to literature data. The device exhibits an epilayer thickness of 1.8 μm and a breakdown voltage of 150 V.

Starting from a defect-free structure we have calculated an on-state resistance close to 140 kΩ μm^2 ($V_{GS}=10$ V, $V_{DS}=1$ V, and $T=300$ K), which increases up to 200 kΩ μm^2 for a defective device. This result is comparable to that of a commercial Si-based MOSFET rated for the same voltage range. The MOSFET threshold voltage and carrier mobility in the channel region decrease as a function of both temperature and trap density. In particular, the oxide-fixed traps have a severe impact on the threshold voltage.

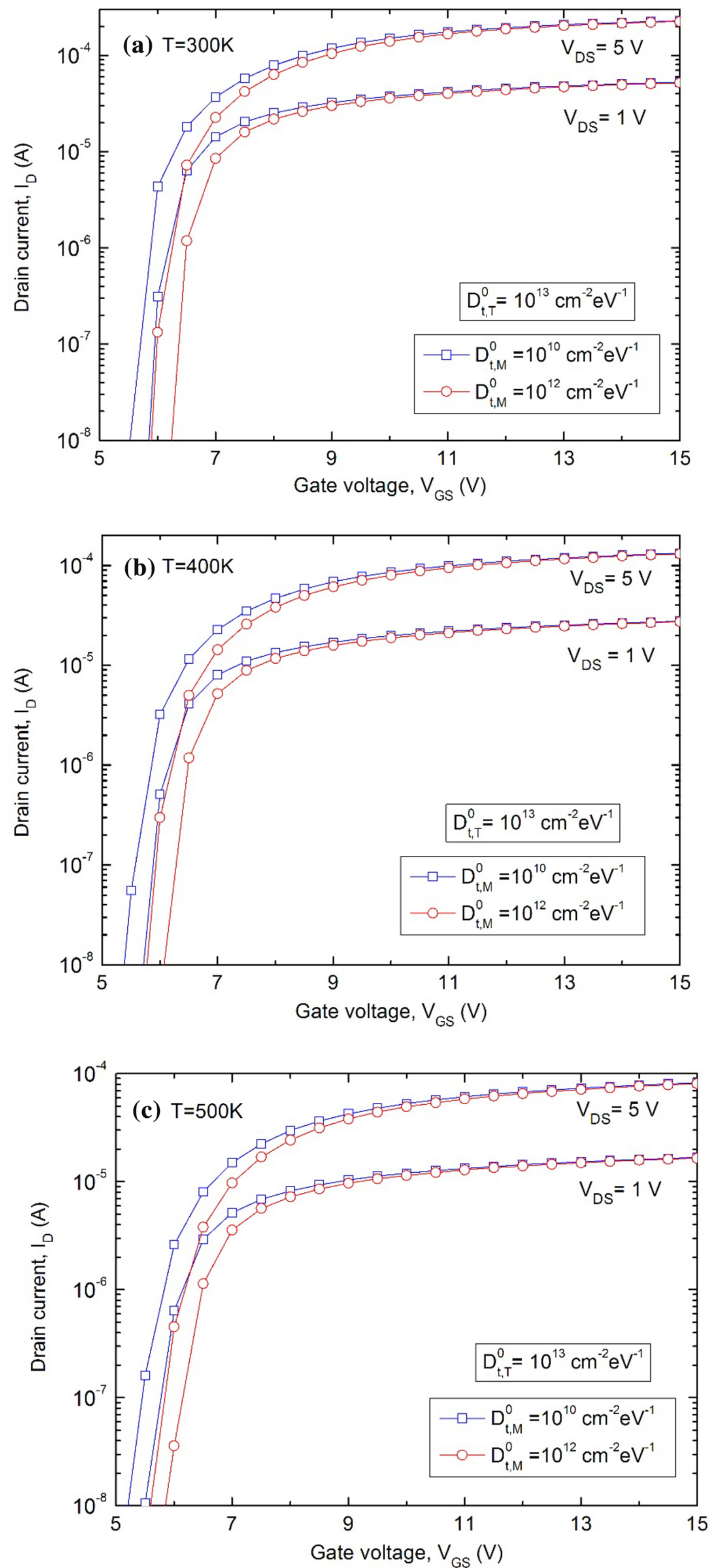

Fig. 8 $I_D - V_{GS}$ characteristics as a function of the deep-level trap density at **a** $T = 300$ K, **b** $T = 400$ K, and **c** $T = 500$ K

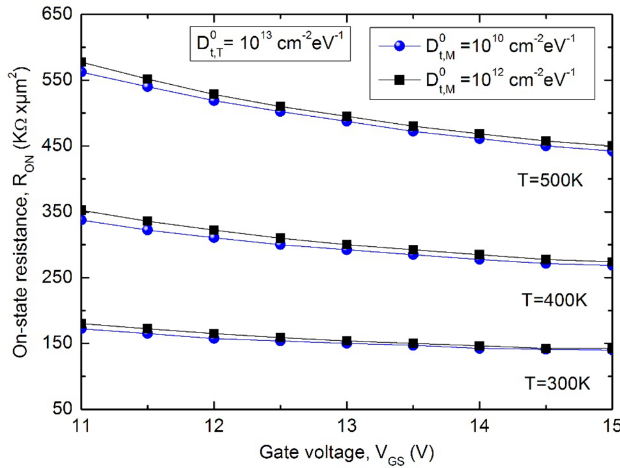

Fig. 9 R_{ON} as a function of V_{GS} for different deep-level trap densities in the temperature range of 300–500 K. $V_{DS}=1$ V

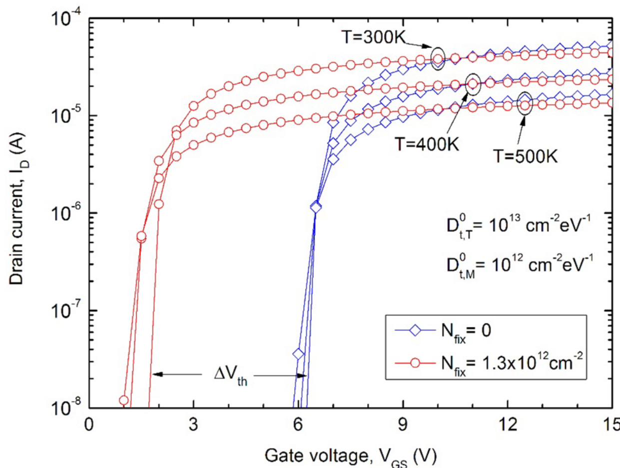

Fig. 10 $I_D - V_{GS}$ characteristics for an oxide-fixed trap density at different temperatures. $V_{DS}=1$ V

The presented analysis could turn useful to support the design of low breakdown voltage 4H-SiC-based MOSFETs seeing that the pure experimental characterization of the device reliability is very expensive and time consuming.

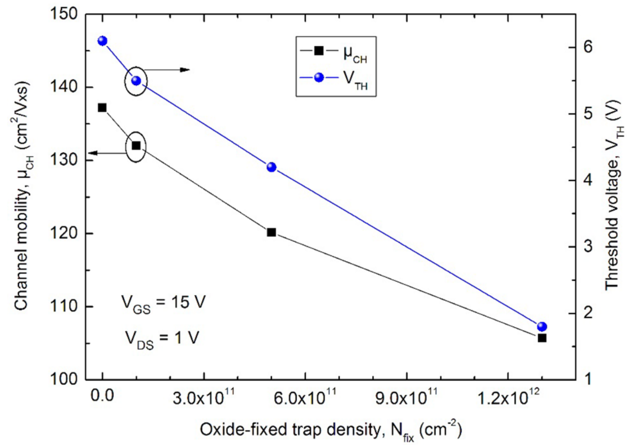

Fig. 11 Channel mobility and device threshold voltage as a function of the oxide-fixed trap density at $T=300$ K

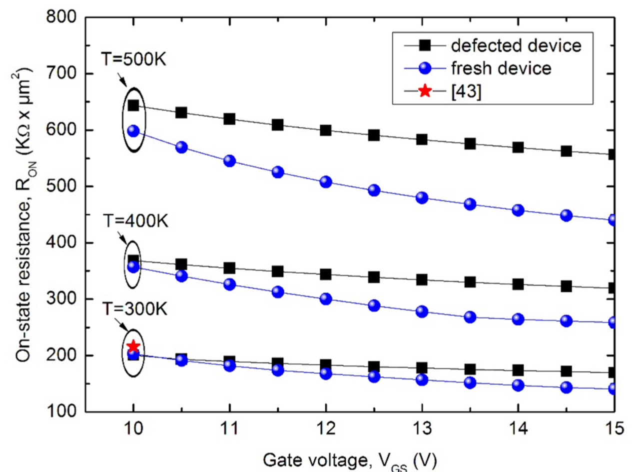

Fig. 12 R_{ON} behaviors as a function of V_{GS} at different temperatures

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