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Solution-processed flexible non-volatile resistive switching device based on poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3] thiadiazol-4, 8-diyl)]: polyvinylpyrrolidone composite and its conduction mechanism

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Abstract

Recently, solution-processed resistive switches for wearable electronics have got tremendous attention and are required for different applications due to their easy process and fabrication. Hence, this paper proposes the solution-processed resistive switching memory device based on two polymers, poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4, 8-diyl)] (F8BT) and polyvinylpyrrolidone (PVP) composite, which is fabricated on a flexible indium–tin–oxide (ITO)-coated polyethylene terephthalate (PET) substrate through spin coating technology. The fabricated device demonstrates a perfect non-volatile bipolar resistive switching through small operating voltage sweeping of ± 1.5 V, and its high-resistance state (HRS) and low-resistance state (LRS) are 92678.89 Ω and 337.85 Ω, respectively. To verify the non-volatility and long-term stability, the device is checked for more than 700 endurance cycles. During these cycles, the variations of HRS and LRS are 48 Ω and 37.35 Ω, respectively. The retention time is checked for more than 60 days, and the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio is 274.31. The bendability is carried out up to bending diameters < 10 mm, and FESEM is used for the morphological characteristics of the device. Conduction mechanism of the proposed device is supported by space charge-limited conduction (SCLC) which is explained by the log–log I–V slope-fitting curve. The results insure that the F8BT:PVP composite-based resistive switching device is to be a potential candidate for the future flexible and low-power non-volatile resistive switching memory device.

Abbreviations

F8BT	Poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4, 8-diyl)]
PVP	Polyvinylpyrrolidone
ITO	Indium–tin–oxide
PET	Polyethylene terephthalate
Ag	Silver
THF	Tetrahydrofuran
HRS	High-resistance state
LRS	Low-resistance state
V	Voltage
I–V	Current–voltage
SCLC	Space charge-limited conduction

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1 Introduction

After the theoretical model of memristor proposed by Leon Chua in 1971 [1] and physical realization by HP research group in 2008 [2], the memristor was considered to be the fourth fundamental circuit element that relates electric charge and magnetic flux. Some researchers also named memristor as a resistive switching device that remembers its previous state of resistance even after removal of external power. Resistive switching devices got tremendous attention because of their usage in different applications such as digital logic design [3], non-volatile memory [4–6], neuromorphic research [7–9], and flexible frequency selective filters [10]. To replace the traditional transistor, the memristors have the potentials due to their simple structure, low cost, easy to fabricate, small size, flexibility, and high integration. Due to these exceptional characteristics, many researchers are motivated towards memristors to realize it as a commercial electronic component. Mainly, three categories of research are going on nowadays such as changing and

investigating the active layer materials [11], fabricated technology [12], and device structure [13].

Fabrication technologies play an important role in the solution-processed electronic devices for the proper and uniform active layer disposition. To fabricate the printed electronic devices, many fabrication technologies are available, i.e. chemical solution deposition (CSD) [14, 15], chemical vapor deposition (CVD) [16, 17], e-beam evaporation deposition [18], and molecular beam epitaxy (MBE) [19]. All the mentioned fabrication processes have not only high-quality insulating layer deposition but also have some hereditary limitations such as high-temperature environment, high capital cost, radiation effects on human life, infeasible for mass production, and long processing time. To overcome these limitations, further researches are going on into such technologies for the proper disposition of solution-processed electronic devices and their applications. The method used in this work is a spin coating technology, which is the simplest and easiest fabrication technology for solution-processed devices.

Furthermore, the solution-processed device structure also plays an important role and gets tremendous attention in resistive switching devices. Utilizing different structures, i.e. staked structure [20], heterojunction structure [11], and single active layer structure [8], the performance of the resistive switching devices can be improved. Recently, different research groups are studying photoconductive materials to enhance the electromagnetic phenomena in resistive memory devices to enhance their $R_{\text{off}}/R_{\text{on}}$ ratio due to enhancement of the electric/magnetic current between top and bottom electrodes [21–23]. Besides, different materials, i.e. nanowire, meta materials, nanoparticles, graphene for metadevices and metasurfaces, are utilized for such structures to improve the performance in different applications [24–36].

The various materials such as polymers [37], organic and inorganic [38], semiconductor [39], and insulators [40] are widely applied for memristor's realization. In the research topics for the materials of the active layer, there are three categories such as a single material active layer [41], a heterojunction of two materials as an active layer [11], and a composite of multiple materials used for different applications [42–48]. Among these topics, the composite of materials has got tremendous attention because of its hybrid properties [49]. The various composites using the various materials have been explored and investigated for memory applications [17, 50]. However, more study and research are still required to improve the stability, off/on resistance ratio, low power and flexibility. To improve these characteristics, we select the two polymer materials, poly[(9,9-di-n-octyl-fluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4, 8-diyl)] (F8BT) and polyvinylpyrrolidone (PVP) for designing the composite active layer for memristor because the polymeric materials have low cost, low-power consumption, light weight, low-temperature processing, large-area applications, and easy to fabricate. Furthermore, these are environment friendly, too [51].

In this paper, we propose a new resistive switching device based on composite of two polymers, Poly[(9,9-di-n-octyl-fluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4, 8-diyl)] (F8BT) and polyvinylpyrrolidone (PVP), for insensitive device against endurance cycles. It is fabricated on a flexible ITO-coated PET substrate by all-printed approach using spin coater at 1700 rpm. The Ag epoxy is used to fabricate the top electrode of the proposed memory device. Resistive switching properties are measured by current–voltage (*I–V*) curves and the proposed memory device demonstrates rewritable, non-volatile, and bipolar resistive switching during small operating voltage sweeping of ± 1.5 V. To verify the non-volatility and long-term stability, the device is checked for more than 700 endurance cycles, and the variations of high-resistance state (HRS) and low-resistance state (LRS) are just 48 Ω and 37.35 Ω, respectively. A bendability test on various bending diameters was carried out to show the mechanical robustness of the fabricated device, and FESEM was also used for its morphological characteristics. The proposed device shows the stable and repeated results of electrical and mechanical characterization, and it proves this F8BT:PVP composite can be a potential candidate for the future flexible and low-power non-volatile memory devices.
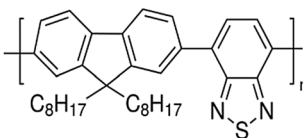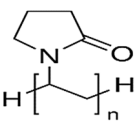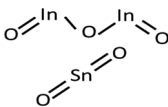
2 Materials and methods

2.1 Materials

F8BT powder with average MW ~ 20,000, PVP average MW ~ 25,000, tetrahydrofuran (THF) solvent, Ag epoxy and ITO-coated PET with thickness around 100 µm was purchased from Sigma-Aldrich Korea. The surface resistivity of the ITO is 50 Ω/sq. All materials were used without further purifications. Furthermore, the insulator behaviors of the materials depend on the dielectric constant and bandgap between HOMO and LUMO. If we have higher bandgap and dielectric constant, we can trap more number of charge carriers in an active layer. These phenomena can be confirmed by electromagnetic modeling of dielectric mixtures [52]. The electromagnetic modeling of the material totally depends on the frequency and effective permittivity. Table 1 shows the chemical formula, molecular structure and the chemical properties of all the above-mentioned materials that are utilized in the fabrication of device.

2.2 Ink formation

To make the composite ink solution for the fabrication of active layer, F8BT and PVP powder were dispersed in 3 ml

Table 1 Materials and their properties

Material	Chemical formula	Molecular structure	Chemical properties	Solubility
F8BT	$(C_{35}H_{42}N_2S)_n$		Average $M_{w} \sim$ 20,000 P-type mobility $= 4 \times 10^{-3}$ cm^2/V s Organic semiconductor	THF
PVP	$(C_6H_9NO)_n$		Average $M_{w} \sim$ 25,000 white to light yellow, hygroscopic, amorphous powder	THF
Ag	Ag	Ag	Resistivity 1×10^{-4} ohm cm Viscosity 90,000 cps	Thinner: butyl carbitol acetate
ITO	$In_2O_3 \cdot (SnO_2)_x$		Resistivity 50 ohm/sq Transmittance 80%	Coated on PET substrate

THF solvent in ratios of 1:1, 2:1, and 3:1. Three different ratios of F8BT were used to optimize the blending ratio for a high OFF/ON resistance ratio. To make homogenous suspensions, the composite solutions were bath sonicated for 1 h at room temperature. The composite solutions were then centrifuged for 40 min at 1000 rpm to remove the big chunks and particles. The supernatants were removed and then these were used as the final solutions for the fabrication of the active layer for the proposed memory device. Figure 1 shows the chemical structure of F8BT and PVP polymers along with their composite ink in THF.

2.3 Device fabrications

Prior to beginning with fabrication, the ITO-coated PET substrate was rinsed with ethanol and few dips in distilled water to remove the ethanol. Afterward, the substrate was UV–ozone treated for 5 min. The F8BT:PVP composite layers with different ratios were deposited through the spin coater at 1700 rpm for 60 s on ITO-coated PET substrate and cured for 90 min at 120 °C. Here, the ITO acts as the bottom electrode of the proposed device and at the end, top electrodes were deposited by the Ag epoxy and cured for 1 h at 100 °C. All fabrication steps of proposed memory devices are illustrated sequentially in the flow diagram of Fig. 2.

2.4 Surface morphology

The active layer of the memory device was analyzed with FESEM Jeol JSM-7600F for surface morphology characterization. Figure 3a shows the SEM image of the PVP layer on 100-nm scale with 50,000× zoom. Similarly, the F8BT layer is analyzed on a 100-nm scale as shown in Fig. 3b with the same 50,000× zoom, where Fig. 3c shows the SEM image of the composite of F8BT and PVP with 3:1 ratio, respectively. Figure 3d shows the SEM image of the Ag top electrode at 200-nm scale, where we can see that the active layer film and Ag is uniformly deposited and sintered properly without cracks and pores. The proposed resistive switching device is based on thin composite film sandwiched between the top and bottom electrodes. Such (bottom electrode/thin composite film/top electrode) structure was used because of easy fabrication and high-density integration. Furthermore, the composite was utilized to improve the resistive switching property of the proposed device because the blending of PVP in F8BT increases the charge trapping in the active

Fig. 1 Chemical structure of F8BT and PVP polymers along with the composite ink of F8BT:PVP in THF solvent
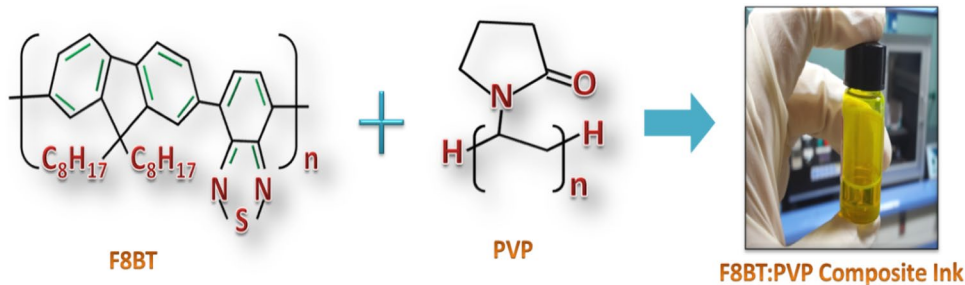
layer that results in increase of the R_{off}/R_{on} ratio, device stability, and retention time. The device comparison is given in Table 2. In thin film technology, the surface morphology plays an important role. For stable results, the film should be uniform without pores and cracks. If the thin film has crack or some pores, then the device will be short even after

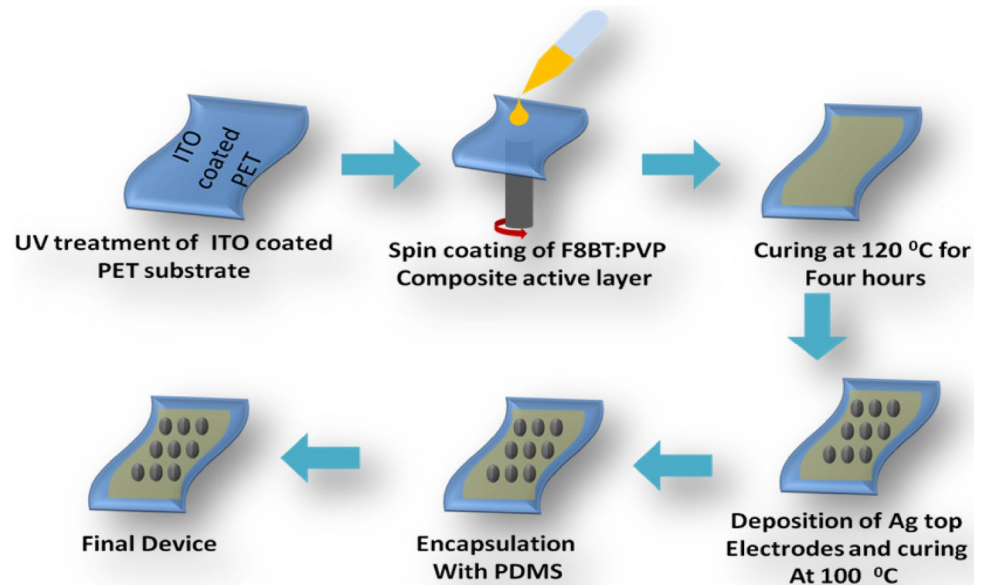**Fig. 2** Flow diagram for the complete fabrication process

Fig. 3 FESEM images for the surface morphology and uniform deposition of all polymeric thin films, **a** PVP, **b** F8BT, **c** composite of F8BT and PVP, and **d** Ag top electrode, where inset is the cross-sectional SEM image of the proposed device
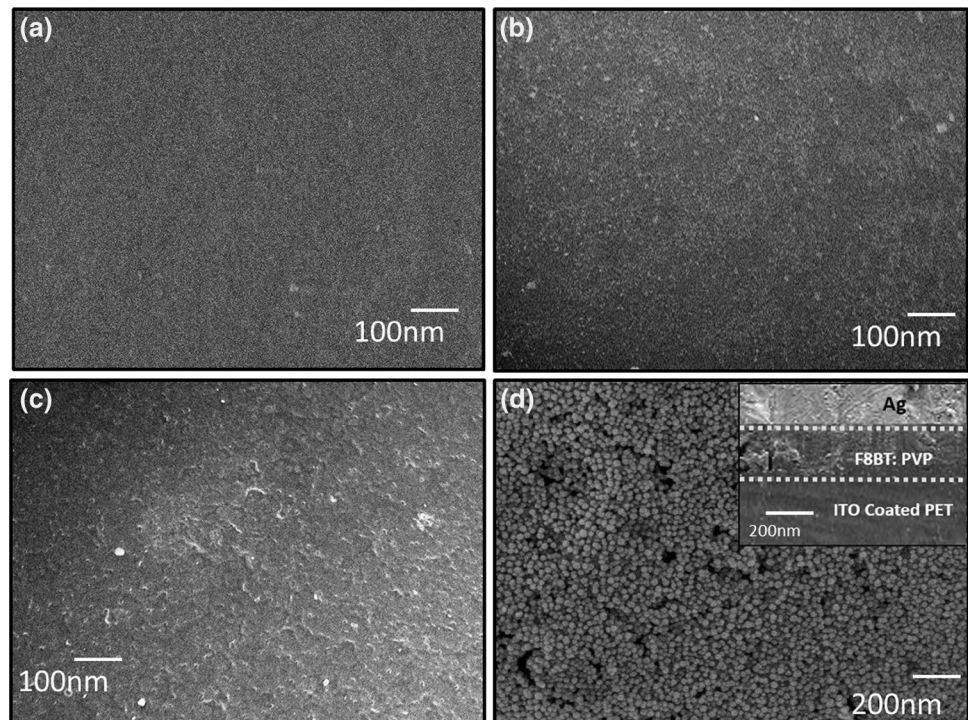
Table 2 Comparison of F8BT:PVP composite-based memory and F8BT memory device

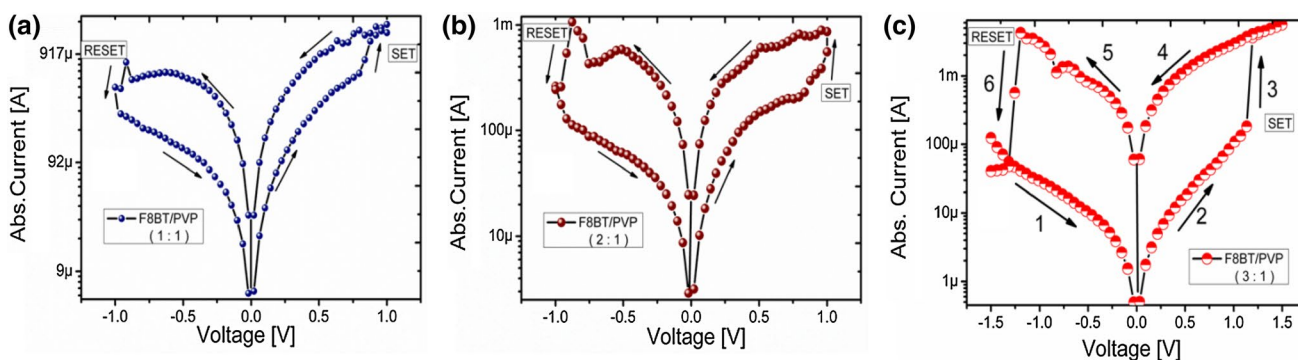| Active layer	Operating voltage	R_{off}/R_{on} ratio	Endurance	Retention Time	Ref.
F8BT:PVP	± 1.5 V	274.31	700 cycles	60 days	This work
F8BT	± 6 V	10	100 cycles	–	53

Fig. 4 Electrical characterization of the proposed memory device with different ratios of the F8BT and PVP to optimize the blending ratio for a high OFF/ON ratio. Typical log *I–V* characteristic curve with F8BT:PVP of **a** 1:1, **b** 2:1, and **c** 3:1

sweeping of small voltage and the device will be destroying. And also if the film is not uniform, the results will be inconsistent from device to device. Therefore, the surface of the thin film should be without cracks and pores and should be uniform all over the area. The ratio of two materials for the composite film affect the surface morphology, but two polymers with the same solvent are utilized in our study which results in the proper and uniform fabrication of the composite thin film. For further analysis, the cross-sectional SEM image with magnification level of 200 nm was analyzed, which insures that all films are properly fabricated and uniform as the inset image shown in Fig. 3d.

3 Results and discussion

3.1 Characterizations

Agilent B1500A Semiconductor Device Analyzer was used for the electrical characterizations of the ITO/

F8BT:PVP/Ag resistive switching device. To measure the resistive switching device, it was placed in the probe station and probes were connected across the device as bottom and top electrodes. Before applying a double-sweep voltage, the proposed device was passed through electroforming practice by applying a positive sweep voltage of 0–5 V to accomplish a stable resistive switching as shown in Fig. 5a. After the successful electroforming, double-sweep voltage was applied across both the top and bottom electrodes and a bipolar resistive switching was observed as shown in Fig. 5b. Solution-processed memory devices sustain and remember their previous state of resistance when current or voltage is applied. Therefore, *I–V* properties of resistive memory device provide valuable set of information that includes R_{off}/R_{on} ratio, current density, operating voltage, HRS, LRS and its stability. To optimize the blending ratio of composite with best performance, we fabricated three devices with different ratios, i.e. 1:1, 2:1 and 3:1 of F8BT and PVP, respectively. All three devices were placed in the probe station, and sweep voltages were
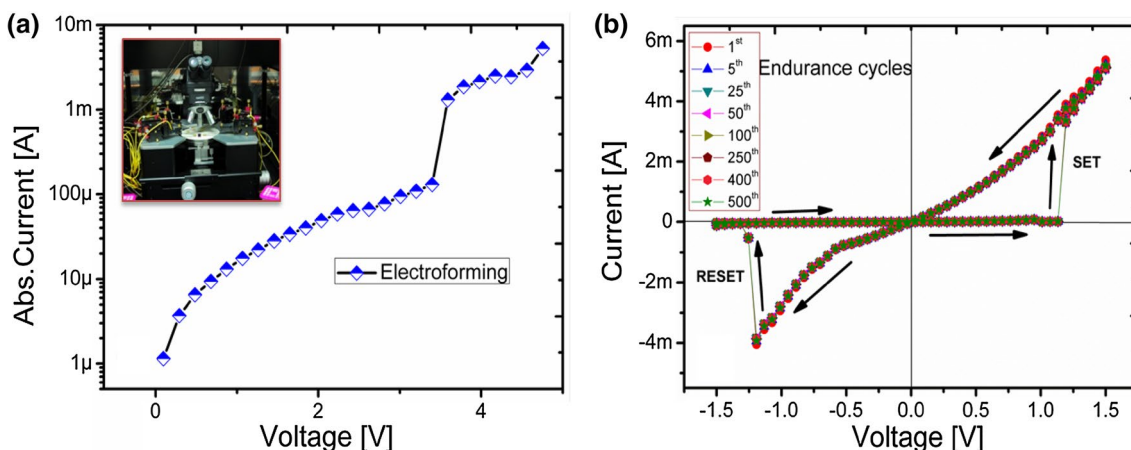

Fig. 5 Electrical characterization. **a** Electroforming curve before applying double-sweep voltage and **b** bipolar *I–V* curves showing stability for more than 500 cycles

applied for electroforming and after successful electroforming, double-sweep voltage was applied for resistive switching.

A compliance of 10 mA was applied to avoid the possible device breakdown. At the initial stage, the device is at HRS and as the magnitude of the positive voltage increased, the current through the active layer also increased resulting in switching from HRS to LRS at a specific voltage know as SET process. The device with 1:1 blending ratio switches from HRS to LRS at $+0.75$ V as shown in Fig. 4a with R_{OFF}/R_{ON} of 30 while the device with 2:1 ratio switches from HRS to LRS at $+0.86$ V with R_{OFF}/R_{ON} of 73 as shown in Fig. 4b. At the end, we checked the device with 3:1 ratio and its switch from HRS to LRS at $+1.0102$ V with R_{OFF}/R_{ON} of 274.31 as shown in Fig. 4c. From this analysis, we select the best blending ratio of 3:1 of F8BT and PVP.

To continue with the optimized ratio of 3:1, we have fabricated the device for further analysis. The device was biased with a double-sweep voltage from -1.5 to $+1.5$ V with a current compliance of 10 mA, and a resistive switching behavior was observed with two different resistive states of LRS and HRS as shown in Fig. 5b. The resistance of the HRS state was observed to be 92678.89 Ω and that of the LRS state is 337.85 Ω. The device exhibited endurance cycles more than 500 cycles that confirms the device stability against endurance as shown in Fig. 5b. It shows insensitivity by the endurance cycles that almost symmetric I–V curves are obtained. The insensitivity is an important factor to be considered in the solution-processed resistive switching devices as mostly some materials show sensitivity towards Joule heating, due to which the device can sustain for very small number of endurance cycles. In contrast, the composite thin films show insensitivity towards Joule heating due to their hybrid and updated properties. The proposed device shows more than 500 endurance cycles without degradation or variations which confirms its insensitivity as shown in Fig. 5b.

Furthermore, the fabrication consistency of the solution-processed resistive switching devices is also a very important factor for reproduction as mostly in such cases there is high variation from device to device. To confirm the consistency of the proposed solution-processed resistive switching device, we fabricated five devices under the same parameters and conditions. On checking and measuring the I–V behavior and stable resistive switching behavior with the same SET and RESET voltages, same HRS and LRS were obtained, which showed stable fabrication consistency. The memory window between HRS and LRS is also very important for the exact detection to read storage data. The ratio of HRS to LRS is known as R_{off}/R_{on} ratio, and if the device has a high R_{off}/R_{on} ratio, it will be easy to distinguish between HRS and LRS states which results in easy read. The reset occurred around -1.0102 V and the set occurred around $+1.0102$ V. During the voltage sweep from -1.5 to $+1.5$ V, the device did not go into saturation as evident in Fig. 5b.

Figure 6a shows the absolute current–voltage graph of the devices on semi-log scale, which indicates that the devices exhibit bipolar resistive switching as their currents pass through 0 V. Resistive state of the device starts from "1" (HRS) and passes through "2" followed by "3" which is a transition from HRS to LRS; the LRS state remains in "4" and then the sweep voltage goes back and passes through "5" which is the LRS state and at -1.0102 V it goes again to HRS through "6" and completes the resistive switching cycle. As shown in Fig. 6b, the endurance test of the fabricated resistive switching was checked for 700 biasing cycles and the inset is the zoomed graphs of both HRS and LRS. The maximum resistance variations in LRS and HRS are 37.35 Ω and 48 Ω, respectively, as revealed
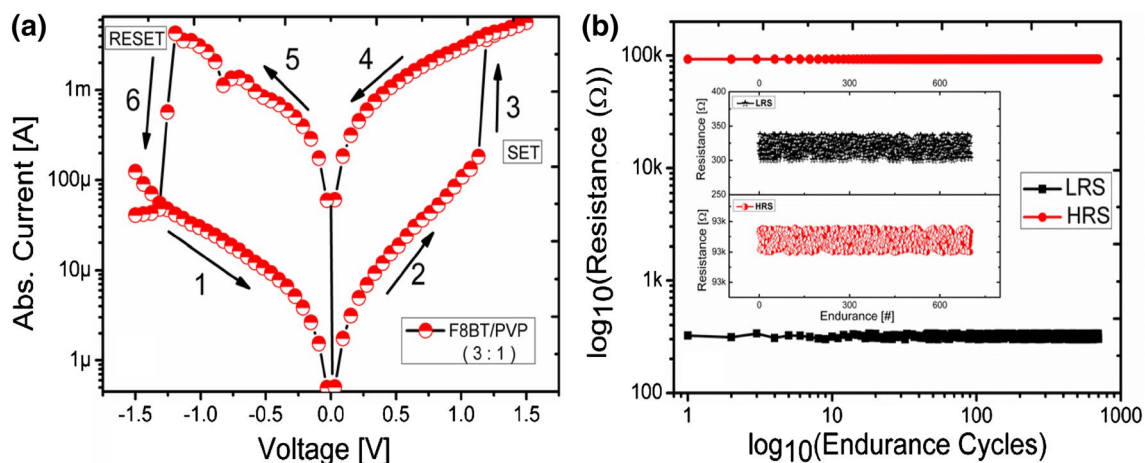

Fig. 6 **a** Typical log I–V characteristic curve of the memristor showing bipolar resistive switching with ratio 3:1 of F8BT:PVP. **b** HRS and LRS states of resistive switch for 700 endurance cycles, showing excellent repeatability and stability
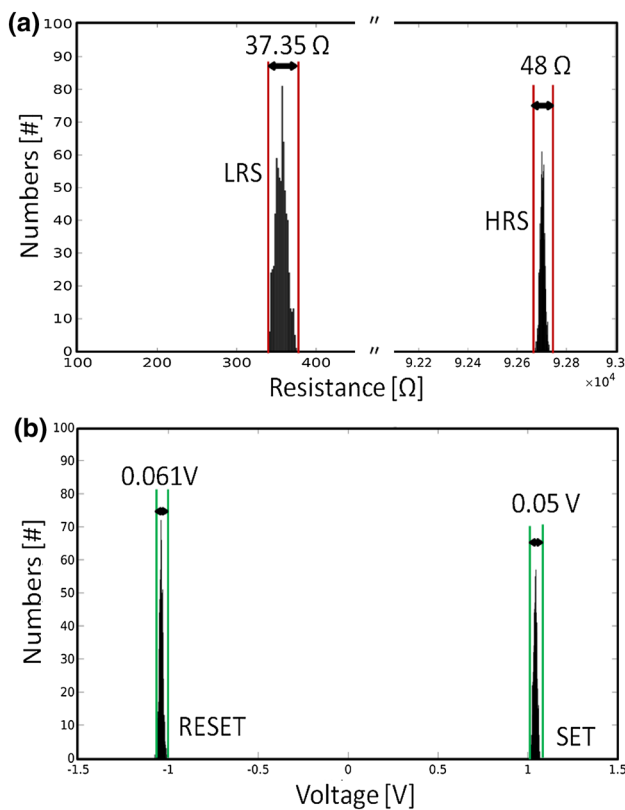
Fig. 7 a Histograms of HRS and LRS for 700 cycles. **b** Histograms of SET and RESET voltages for 700 cycles that prove the stability of the device

by the histogram in Fig. 7a, which shows that LRS and HRS are very insensitive against endurance cycles. The proposed device also shows excellent stability via SET and REST as shown in Fig. 7b. The maximum variations in SET and RESET voltages are 0.05 V and 0.061V, respectively. From this analysis, we can say that the device is stable along both resistances (HRS and LRS) and also along SET–RESET voltages.

Figure 8a shows the reading of the previous state, which is the evidence of its application for non-volatile memory. The switching voltages to the HRS and the LRS are ± 1.0102 V, and the non-volatility of the proposed device is also measured for more than 60 days as shown in Fig. 8b, and a small change occurred in HRS and LRS resistance states that the device shows a stable and non-volatile characteristics. Here, although the resistance drift occurs in both HRS and LRS, the R_{off}/R_{on} ratio was not affected much. The mechanical characteristics were analyzed by bending it on different diameters from flat 20 mm down to 10 mm diameter using the homemade bending machine as shown in the inset of Fig. 8c. It was found that minimum bending diameter was 10 mm as shown in Fig. 8c; bending beyond

10 mm, the device got open-circuited due to the breakage of top electrode.

3.2 Conduction mechanism

The switching mechanism of the fabricated device can be explained with the help of a log–log *I–V* slope-fitting curve as reported in PVP [50], F8BT [53] and composites [20]. According to charge trap mechanism, HRS has very less amount of charge carrier, which does not allow the flow of current. During voltage sweep, charge carrier starts entering the active layer, and at threshold voltage, the active layer (F8BT:PVP composite) has maximum number of charge carrier and memory device shift from HRS to LRS state. To bring back the memory device in HRS state, the opposite voltage sweep is applied and at negative threshold voltage, the decrease in charge carrier and emptied at the end. The *I–V* graph is plotted in log–log scale to find the slope of HRS and LRS. As shown in Fig. 9, LRS shows fitted slope ~ 1.21 (blue-marked region), which indicates the ohmic conduction region and current is directly proportional to voltage ($I \propto V$). However, HRS as off state has two different slope regions. To explain this conduction mechanism, we divided the HRS into region (I) ohmic conduction region $I \propto V$ with slope ~ 1.23 (blue-marked region) and region (II) Child's law region with slope ~ 2.53 (green-marked region). The state transition region with slope ~ 56.9 (red-marked region) is the transition from HRS to LRS and the memory device undergoes in SET process (HRS to LRS). In region (I), a small electric field is created due to the applied voltage and charge carrier starts accumulating at the Ag electrode and the device shows ohmic behavior with slope ~ 1.23 (blue-marked region) from 0 to 0.4 V. In region (II), electrons near the top Ag electrode show mutual repulsion and the charge carrier starts entering the F8BT:PVP composite film and the device transforms from ohmic conduction to space charge-limited conduction (SCLC). According to Child's law, due to these charge carriers, the device shows a slope of ~ 2.53 (green-marked region). In region (III), all charges get trapped in the F8BT:PVP composite film due to trap charge-limited conduction (TCLC). Current and voltage increase proportionally ($I \propto V^n$) and the device undergoes SET process with slope ~ 56.9 (red-marked region).

3.3 Towards marketplace commercialization and applications

Emerging demand of flexible non-volatile memories is under high investigation to replace the conventional charge storage-based devices. For this, one of the promising candidates is the resistive switching memory due to its ease of fabrication and high integration, which is based on a switching mechanism controlled by current or voltage. Resistive switching
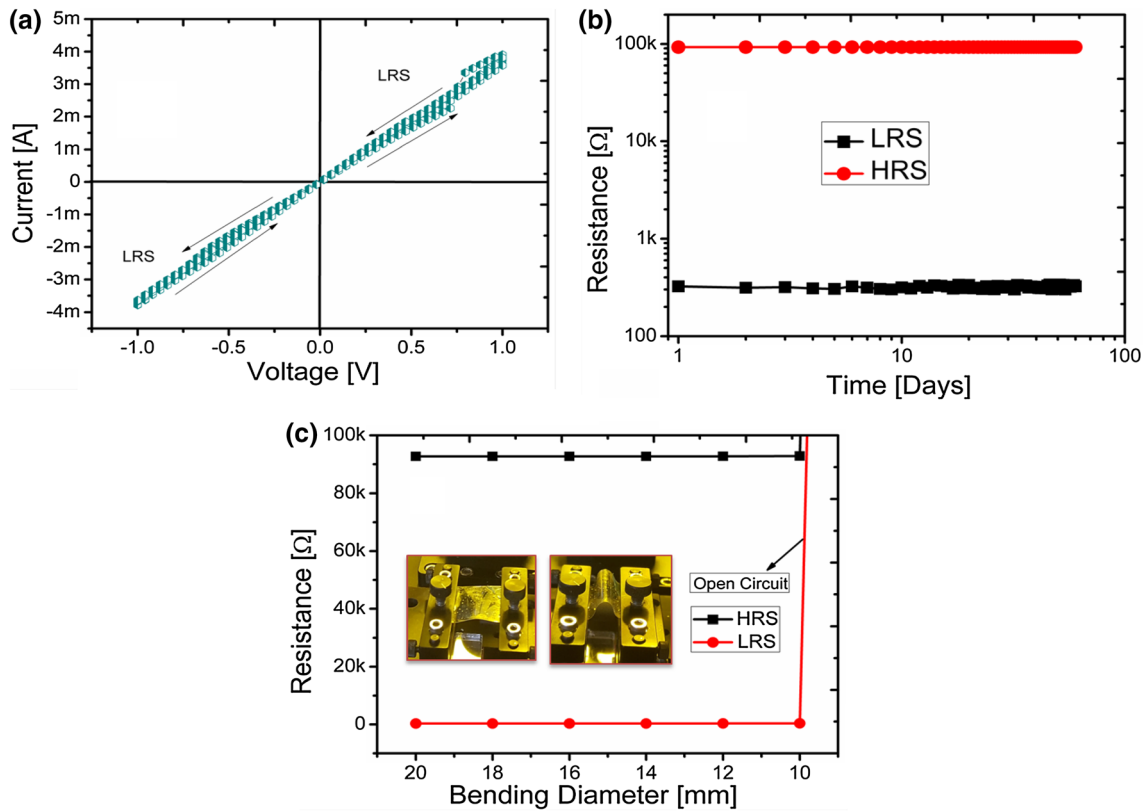
Fig. 8 **a** Device stability in its previous state, i.e. LRS for long time without going back to HRS within read voltage. **b** Retention time analysis for more than 60 days. **c** Bending test down to 10 mm to prove its flexible nature
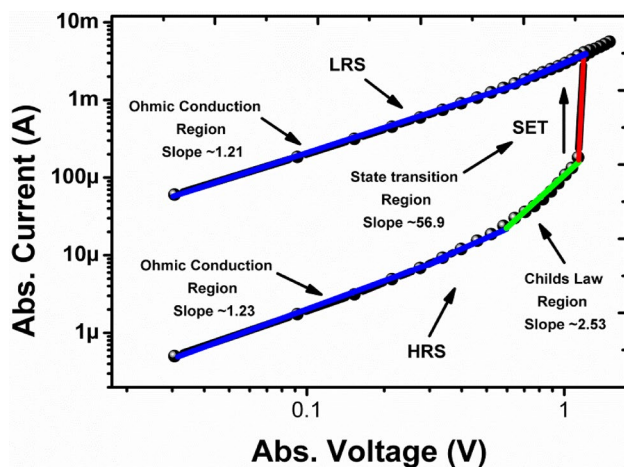

Fig. 9 Double-logarithmic *I*–*V* curve showing the slopes for HRS and LRS with different values of slope

devices switch between HRS and LRS depending on the material nature integrated into the memory element. Therefore, material engineering for such devices got tremendous attention and are widely investigated. Resistive switching devices can be used in many applications, i.e. logic gates,

neuromorphic, frequency selector, and non-volatile memory. But there are few issues and challenges that should be overcome. Mostly, these devices are not that stable due to the materials' sensitivity to other factors such as temperature, humidity, and light, which also affect the endurance stability of the device. In the proposed resistive switching device, the composite of two polymers (F8BT and PVP) is used as an active layer, which is stable towards externally affecting parameters but still there is more improvement needed regarding stability, endurance, and long retention time. Therefore, there is a long way to go for the commercialization of flexible and low-power non-volatile memory devices in future for customized applications.

4 Conclusion

In the paper, flexible resistive switching device with insensitivity against endurance cycles based on poly[(9,9-di-n-octyl-fluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4, 8-diyl)] and polyvinylpyrrolidone (F8BT:PVP) composite was realized. The proposed device has operated as non-volatile and bipolar resistive switch at small operating voltage of ± 1.5 V. It was switched from HRS to LRS at $+1.0102$ V and again to HRS

at − 1.0102 V. Their HRS and LRS values are 92678.89 Ω and 337.85 Ω, respectively. Non-volatility and long-term stability of the device were checked for more than 700 endurance cycles. The retention time of the device was measured for more than 60 days, and the OFF/ON ratio was 274.31. Bendability test at various bending diameters was carried out to show the mechanical robustness of the fabricated device. FESEM was used to study the morphological characteristics of the device. A limitation of the proposed method is that by this method we cannot fabricate the crossbar array as there is a limitation of the spin coater technology while fabricating the top electrode. There is still window for the improvement in the solution-processed resistive switching devices such that long retention time, endurance cycles stability, and flexibility for the future customized wearable electronic applications. However, the remarkably stable and repeated results on electrical and mechanical characterizations show that the proposed composite can be utilized as a potential candidate for the future flexible and low-power non-volatile memory devices.

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