



# Memory improvement in lead-free BiFeO<sub>3</sub> ferroelectric with high-k Al<sub>2</sub>O<sub>3</sub> buffer layer for non-volatile memory applications

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## Abstract

We report the deposition of ferroelectric lead-free BiFeO<sub>3</sub> perovskite film on Si (100) substrate by RF magnetron sputtering using Al<sub>2</sub>O<sub>3</sub> as buffer layer. X-ray diffraction and multiple-angle ellipsometric analysis show the pure ferroelectric phase and maximum refractive index of the BiFeO<sub>3</sub> film at the annealing temperature of 500 °C. For different annealing temperature of Al<sub>2</sub>O<sub>3</sub> film, amorphous film structure and refractive index in the range 1.7–1.77 has been observed. Metal–ferroelectric–metal (MFeM), metal–ferroelectric–silicon (MFeS), metal–insulator–silicon (MIS) and metal–ferroelectric–insulator–silicon (MFIS) structure have been fabricated with BiFeO<sub>3</sub> ferroelectric and Al<sub>2</sub>O<sub>3</sub> insulator layer to investigate the electrical characteristics. Improvement in the memory window from 2.3 V in MFeS structure to 4.8 V in MFeIS structure has been observed with 10 nm buffer layer at the annealing temperature of 500 °C. The MFe<sub>(100 nm)</sub>I<sub>(10 nm)</sub>S structure annealed at 500 °C shows the breakdown voltage of 38 V and no degradation in the polarization charge upto the read-write cycles of 10<sup>8</sup>.

## 1 Introduction

In the last two decades, continuous scaling of flash memory has brought it to its physical limit that has led to the requirement of an alternating non-volatile memory (NVM) technology. Single-transistor-based ferroelectric memory also known as ferroelectric field effect transistor (Fe-FET) has emerged as one of the promising candidate to meet the NVM requirements such as small size, high speed, ease of operation, and low operating voltage. In single-transistor-based ferroelectric memory, the ferroelectric film polarization controls the channel between source drain and the channel resistivity shows the device ON/OFF state. The FeFET was proposed in late 1960s [1–3] and the first FeFET was fabricated by Wu et al. [4]. Further, an improved structure with the insulator layer sandwiched between ferroelectric and silicon substrate, i.e. metal–ferroelectric–insulator-field-effect-transistor (MFIS-FET) was demonstrated by Sugibuchi et al. [5]. The research on the development of MFIS-FET was slowed down during that period due to the technological challenges. In the last two decades, with the advancement in

process and deposition technologies, the research and development of the MFIS-FET is now on surge for the future NVM [6].

Ferroelectricity in perovskite materials has revolutionized the research and developments towards the non-volatile memory. Perovskite-type materials having chemical formula ABO<sub>3</sub> has been widely investigated for pyroelectric, piezoelectric and ferroelectric applications [7]. Different lead-based and bismuth-based perovskite materials such as BaTiO<sub>3</sub>, PbTiO<sub>3</sub>, SrTiO<sub>3</sub>, PbZrO<sub>3</sub>, PZT, SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub>, and SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> have been widely investigated and their ferroelectric properties have been explored over the years. Lead-based perovskite shows large polarization but suffers from fatigue and is toxic in nature [8], whereas the bismuth-based perovskites are fatigue free and even non-toxic [9]. Bismuth ferrite (BiFeO<sub>3</sub>) has been developed in 1970s [10], when the atomic structure was investigated by C. Michel et al. [11] and the dielectric hysteresis in single-crystal BiFeO<sub>3</sub> was first reported by Teague et al. [12]. Since then BiFeO<sub>3</sub> has been studied as an important multiferroic material. Many researches have been done to explore the electrical properties of pure BiFeO<sub>3</sub> deposited by solid-state reaction [13], microwave-assisted sol–gel [14–16], pulsed laser [17], chemical synthesis [18], etc. Ca-doped [19], La-doped [20], Zn-doped [21], and different transition metal-doped [22] BiFeO<sub>3</sub> thin films have also been investigated for ferroelectric and multiferroic applications. In the recent

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years, as an alternative to FLASH memory, the integration of perovskite thin films on silicon for non-volatile memory (NVM) applications have been promoted. BiFeO<sub>3</sub>, due to the large polarization [23] and multiferroic property [24, 25], has emerged as an important candidate for the NVM application. In the direct integration of BiFeO<sub>3</sub> on silicon, due to ferroelectric–silicon lattice mismatch and silicon diffusion into BiFeO<sub>3</sub> [26], the ferroelectric properties of BiFeO<sub>3</sub> degraded, resulting into larger leakage current and low memory characteristics. To reduce the gate leakage current and suppress the ferroelectric–silicon interdiffusion, a High-k dielectric layer sandwiched between ferroelectric and silicon substrate has been proposed. Various studies have been done with different insulator layers such as CeO<sub>2</sub>/YSZ [27], ZrO<sub>2</sub> [28, 29], HfO<sub>2</sub> [30], BaTiO<sub>3</sub>, and SrTiO<sub>3</sub> [31] and the improved ferroelectric properties have been observed.

In the present study, it is perhaps the first investigation to integrate Al<sub>2</sub>O<sub>3</sub> thin film deposited by sputtering between the ferroelectric and silicon substrate. The selection of insulator layer (Al<sub>2</sub>O<sub>3</sub>) is based upon its high band gap, large conduction band offset [32], high dielectric constant ( $k \sim 8\text{--}10$ ), thermodynamically stability with silicon [33], amorphous even at high processing temperatures [34] and low-interface defect density with silicon [35, 36]. Sputtering deposition technique has been used for the deposition of ferroelectric and insulator film in the current study as it produces high-quality oxide film and widely accepted in R&D industries.

## 2 Experimental procedure

p-type silicon wafer of orientation  $\langle 100 \rangle$  and resistivity 1–5  $\Omega\text{-cm}$  has been used as the substrate for thin film deposition and device fabrication. Single-side-polished silicon wafer of 2" diameter and thickness 275  $\mu\text{m}$  has been selected for cost-effective device fabrication. Ultrasonic bath and standard cleaning method developed by Radio Corporation of America (RCA), RCA-1 and RCA-2, has been carried out to remove the particle, organic and inorganic impurities from the silicon wafer. Oxide removal in buffer HF and nitrogen drying has been carried out prior to the loading of silicon wafer into the vacuum chamber. 99% pure BiFeO<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub> sputtering targets of diameter 2" and thickness 4 mm procured from M/s Testbourne Ltd., UK., have been used for the thin-film deposition. 100-nm thick ferroelectric film is deposited and kept constant throughout the experiment. The ferroelectric film deposition has been carried out at the power density of 9.87 W/cm<sup>2</sup> with deposition rate of  $\approx 6$  nm/min. Insulator layer of three different thicknesses 5, 10, and 15 nm has been deposited at the power density of 4.93 W/cm<sup>2</sup> and at the deposition rate of 2 nm/min. The sputtering has been carried out in a dual target system, the chamber has been pumped at the vacuum of  $5 \times 10^{-5}$  mbar

and the process has been carried out at the pressure of  $1.0 \times 10^{-2}$  mbar in the presence of argon plasma flowing at the rate of 15 standard cubic centimeters per minutes (scm). The deposition of BiFeO<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub> stack has been carried out without breaking the plasma to obtain high-quality ferroelectric/insulator interface.

After the individual film and stack deposition, the annealing has been carried out at 400, 500, and 600 °C in a computer-controlled furnace equipped with quartz tube. The annealing has been done for 30 min in the presence of high-purity nitrogen flowing at the rate of 20 sccm. Structural characterization (film thickness, refractive index and crystal orientation) has been carried out by multiple-angle ellipsometry using the SENTECH 400adv ellipsometer operated at 632.8 nm HeNe laser and X-ray diffraction using Cu-K $\alpha$  laser operated at 1.54 Å wavelength. Electrical characterization (capacitance–voltage (C–V), current density–voltage (J–V), PUND, pulse I–V, endurance and breakdown voltage) has been carried out using Keithley 4200 Semiconductor characterization system. The fabricated MFeM, MFeS, MIS and MFeIS structure design is shown in Fig. 1.

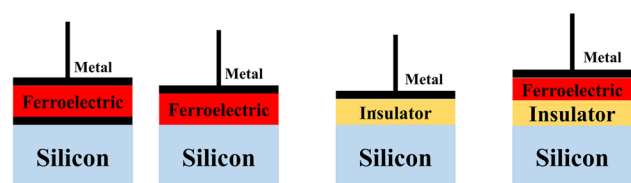
MFeM structure has been fabricated on silicon substrate with 100-nm top and bottom electrodes deposited by RF sputtering. Top metal contacts in all the structures have been deposited using a high-quality stainless steel shadow mask of 100- $\mu\text{m}$  circular opening.

## 3 Results and discussion

### 3.1 Structural characterization

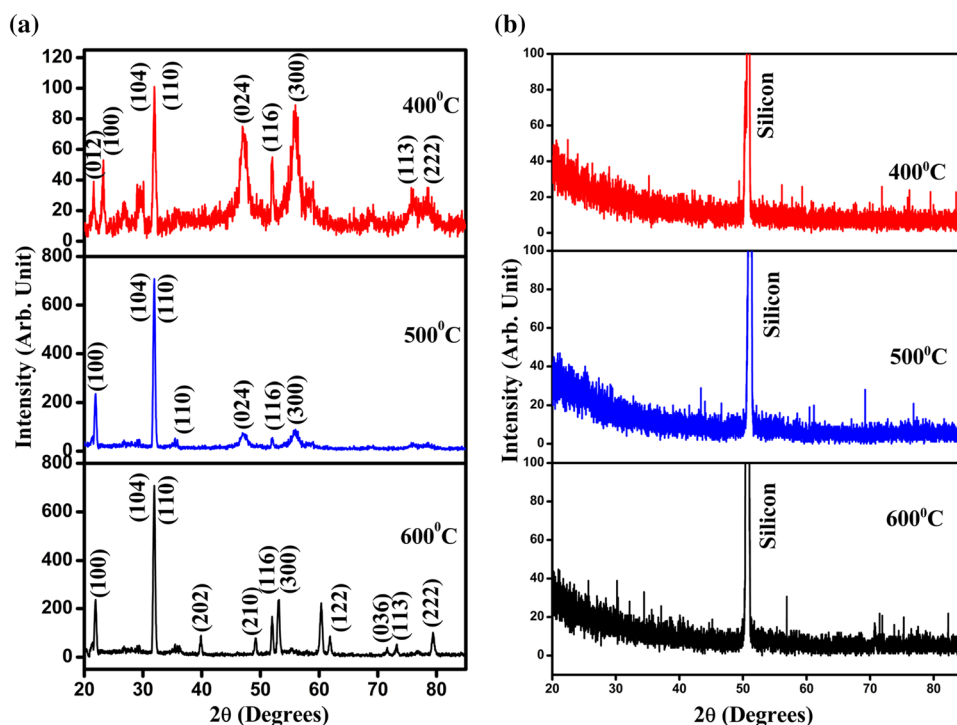
Figure 2a, b shows the XRD patterns of the 100 nm BiFeO<sub>3</sub> and 10 nm Al<sub>2</sub>O<sub>3</sub> film annealed at 400, 500 and 600 °C. Same annealing temperature selection for both the films has been done to minimize the processing steps during stack formation.

Result shows that the BiFeO<sub>3</sub> film annealed at 500 °C crystallizes well in a perovskite phase with the dominant peak (104), (110) at  $2\theta \approx 32^\circ$  and (100) at  $2\theta \approx 22^\circ$ . At the annealing temperature of 400 °C, several high-intensity peaks indicate amorphous and multiferroic film structure. The film perovskite phase reduces and several low-intensity



**Fig. 1** MFeM, MFeS, MIS and MFeIS structures for electrical characterization

**Fig. 2** XRD patterns of **a** BiFeO<sub>3</sub>, and **b** Al<sub>2</sub>O<sub>3</sub> films annealed at 400, 500 and 600 °C

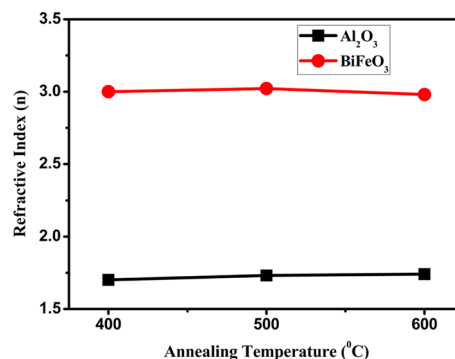


peaks were observed at 600 °C, indicating the change in the ferroelectric property.

XRD pattern of Al<sub>2</sub>O<sub>3</sub> film annealed at different temperature shows no dominant intensity peak indicating the amorphous nature. Amorphous film structure is the basic requirement of the buffer layer [37] as it provides a barrier to charge leakage resulting into lower leakage current in comparison with the crystalline film. In the crystalline film, the leakage current increases due to the extra leakage path through the grain boundaries. Also, amorphous films form excellent quality interface with silicon. The amorphous film could improve the electrical performance of the device by configuring its interface bonding to minimize the number of defect states. This reduces the interface defects, which acts as the leakage path or charge trapping sites [38, 39].

Multiple-angle ellipsometry for the angle range 60–80° in the step size of 5° shows the refractive index of BiFeO<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub> film annealed at 400, 500 and 600 °C (Fig. 3).

The refractive index of Al<sub>2</sub>O<sub>3</sub> film increases from 1.7 to 1.77 with the annealing temperature 400–600 °C, and increase in the refractive index is attributed to the Al<sub>2</sub>O<sub>3</sub> atom rearrangement with annealing temperature and change in film structure towards crystallinity [40, 41]. For the BiFeO<sub>3</sub> film, maximum refractive index of 3.02 has been observed at the annealing temperature of 500 °C, which is attributed to the crystallized ferroelectric film, also confirmed from the XRD result. After structural characterization, electrical characteristics of the ferroelectric, insulator and film stack have been obtained.



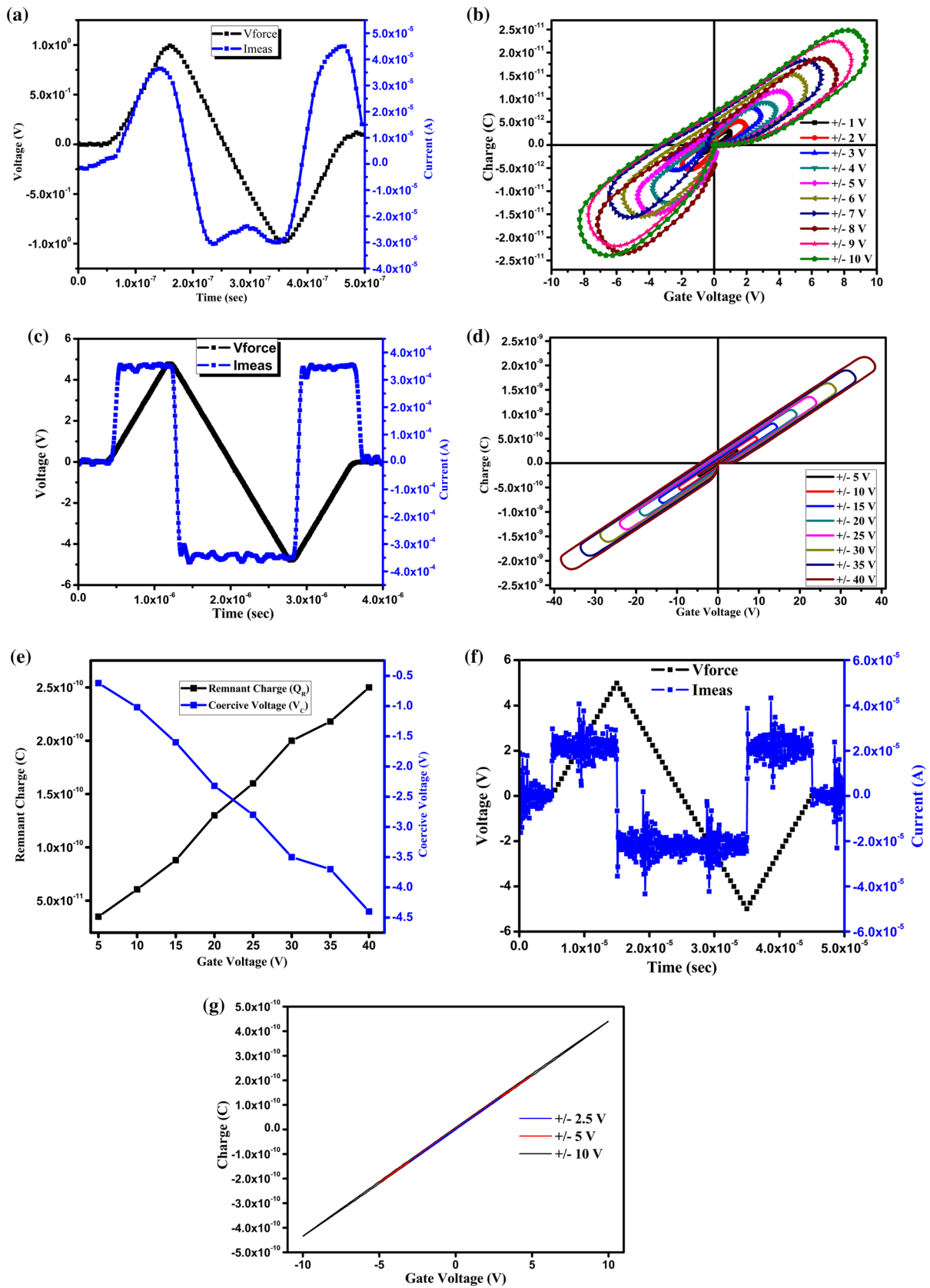
**Fig. 3** Refractive index of BiFeO<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub> film annealed at 400, 500 and 600 °C

## 3.2 Electrical characterization

### 3.2.1 MFeM structures

MFeM structures annealed at 400, 500, and 600 °C were electrically characterized to obtain the pulse IV and hysteresis characteristics, shown in Fig. 4.

For the charge versus voltage measurement, voltage in the form of positive and negative V-shaped pulse has been applied across the MFeM structure and the corresponding current was simultaneously measured. The total current was then sampled to determine the charge across the ferroelectric film. Figure 4a, b shows the pulse IV and hysteresis curve for the ferroelectric film annealed at 400 °C. The pulse IV curve



**Fig. 4** **a** Sample input triangular waveform and current response for the MFeM structure annealed at 400 °C, **b** charge versus gate voltage characteristic of MFeM structure for different input voltage sweep and anneal at 400 °C, **c** input triangular wave and corresponding current for the MFeM structure annealed at 500 °C, **d** charge versus gate voltage characteristic for the MFeM structure annealed at 500 °C, **e** remnant charge and coercive voltage for MFeM structure annealed at 500 °C, **f** input triangular waveform and corresponding current for the MFeM structure annealed at 600 °C, **g** charge versus gate voltage for the MFeM structure annealed at 600 °C

shows the current following the applied voltage in a resistive manner. This resistive nature of the film is attributed to the amorphous crystal structure. The film also shows the irregular and unsaturated hysteresis loop when measured for the voltage range from  $\pm 1$  to  $\pm 10$  V; the irregular hysteresis loop is due to the resistive and multiferroic characteristic of the annealed film. Low remnant charge ( $7.3 \times 10^{-12}$  C) and coercive voltage of  $-3.35$  V have been observed for the voltage sweep of  $\pm 10$  V. MFeM structure with ferroelectric film annealed at 500 °C shows the pure ferroelectric property and, therefore, characterized for the large voltage range from  $\pm 5$  to  $\pm 40$  V (Fig. 4c, d). Significant remnant charges are observed for the structure and plotted in Fig. 4e. The remnant charge increases from  $3.5 \times 10^{-11}$  for 5 V to  $2.5 \times 10^{-10}$  for 40 V voltage magnitude. The hysteresis loop found shrinking for the ferroelectric film annealed at 600 °C, which is due to the decrease in film crystallinity and ferroelectric properties.

### 3.2.2 MFeS structure

The ferroelectric film has been deposited on the silicon substrate, annealed at different temperature, MFeS structure fabricated and J–V and C–V characteristics were obtained, shown in Fig. 5.

Leakage current density of order  $10^{-4}$  A/cm<sup>2</sup> at  $-10$  V and  $10^{-6}$  A/cm<sup>2</sup> at 10 V has been observed at the annealing temperature of 400, 500 and 600 °C. Higher current density at negative gate bias is due to the substrate injection from p-type silicon. Pore and void defects in the ferroelectric film act as the leakage current path, resulting in the relatively high current density in the MFeS structures. With the applied gate voltage, current density increases gradually, which may originate from the gradual release of oxygen vacancy from the complex defects.

The voltage ( $C/C_{ox} - V$ ) characteristic (Fig. 5b) has been measured for the voltage sweep from accumulation to inversion and back to accumulation for the voltage range of  $\pm 10$  V at 100 KHz. The MFeS structure shows the maximum memory window of 2.03 V at the annealing temperature of 500 °C. The memory window reduces to 1.38 V with an increase in the annealing temperature to 600 °C. The memory window indicates the difference between flatband

voltages during the voltage sweep. Maximum memory window is due to the crystallized perovskite film even indicated from the XRD and ellipsometric data. Low memory window observed in the MFeS structures might be due to the following reasons: (1) charge injection into the ferroelectric layer from silicon substrate or metal electrode, (2) interface trap states or defects in the ferroelectric layer and ferroelectric/silicon interface, and (3) voltage drop across the interfacial native SiO<sub>2</sub> layer. To address these causes of low memory window MFeIS structure has been fabricated. Optimization and investigation of the buffer Al<sub>2</sub>O<sub>3</sub> layer has been done by fabricating the MIS capacitor structures.

### 3.2.3 MIS structure

Al<sub>2</sub>O<sub>3</sub> thin film of 10 nm has been deposited on the silicon substrate and annealed at 400, 500, and 600 °C. The structures were then electrically characterized (current density and capacitance were measured) to investigate the effect of annealing temperature on the buffer layer parameters, shown in Fig. 6.

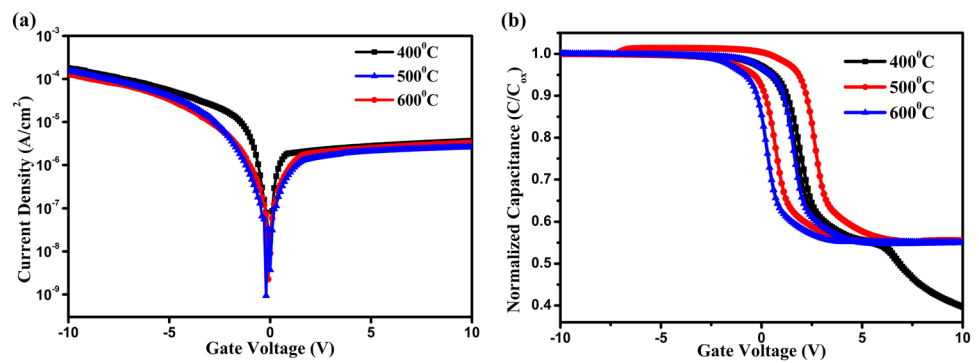
Symmetric leakage current density of the order  $10^{-2}$  A/cm<sup>2</sup> has been observed for the Al<sub>2</sub>O<sub>3</sub> film. The symmetric current is due to the amorphous nature of the deposited film at different annealing temperature even evident from the XRD data. Similar C–V characteristic has been observed for the MIS capacitor with Al<sub>2</sub>O<sub>3</sub> film annealed at different temperature. The results shows that for the annealing temperature selected in this study, the insulator film remains amorphous.

### 3.2.4 MFeIS structure

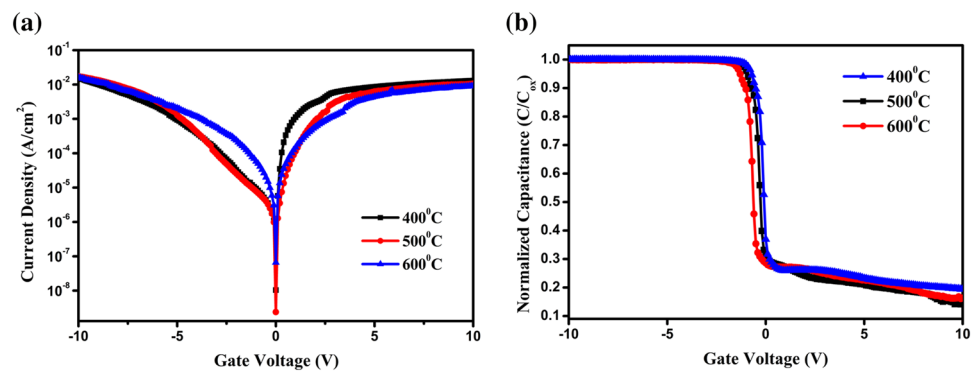
From the structural and electrical characterization of the ferroelectric film, the perovskite nature and maximum memory window has been confirmed at the annealing temperature of 500 °C. Also, amorphous nature of the insulator layer at 500 °C has been evident from the structural and electrical characterization. Based on the findings, annealing temperature of 500 °C has been selected as the reference temperature for further study. For the MFeIS structures, stack of buffer layer (5, 10 and 15 nm) and ferroelectric layer (100 nm) has been deposited and annealed together at 500 °C in nitrogen ambient for 30 min. J–V and C–V measurements were carried out to investigate the device electrical characteristics, shown in Fig. 7.

Leakage current density in the range of  $10^{-4}$ – $10^{-6}$  A/cm<sup>2</sup> has been observed for the MFeIS structure annealed at 500 °C with buffer layer of 5, 10 and 15 nm thickness. As apparent from the obtained characteristics, introduction of buffer layer significantly reduces the substrate injection into the ferroelectric layer leading to the reduced leakage current. At high gate voltage direct tunneling and trap-assisted

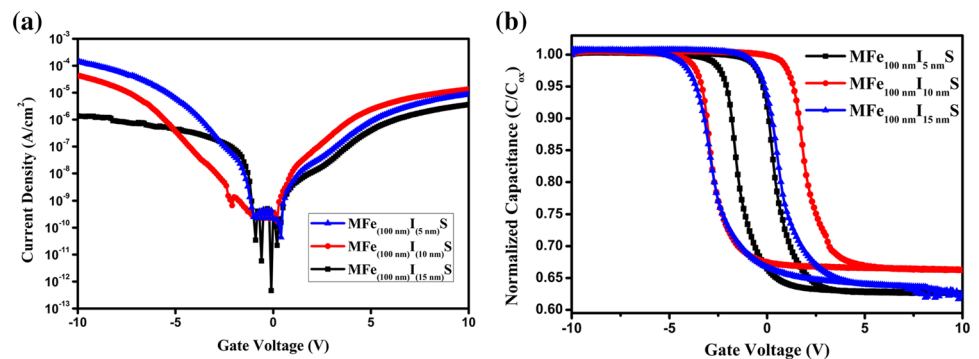
**Fig. 5** **a** J–V and **b** C–V characteristic of the MFeS structure annealed at 400, 500, and 600 °C



**Fig. 6** **a** J–V and **b** C–V characteristics of MIS capacitors annealed at 400, 500 and 600 °C



**Fig. 7** **a** J–V and **b** C–V characteristics of MFeIS structure with 5, 10 and 15 nm buffer layer



conduction is the dominant current conduction mechanism. Fowler–Nordheim tunneling mechanism has been observed at lower gate voltages. Maximum memory window of 3.49 and 4.75 V has been observed for the MFeIS structure with 5 and 10 nm buffer layer, respectively. In the MFeIS structure, memory window depends on the inter-reaction and interdiffusion between the ferroelectric and silicon layer. It is important that the introduced dielectric layer act as a potential barrier to inhibit the charge injection from the silicon substrate to the ferroelectric layer. Along with that, the buffer layer should be sufficiently thick to prevent the inter-reaction between the ferroelectric layer and silicon substrate. Low memory window detected in case of 5-nm buffer

layer is due to the insufficient buffer layer thickness which is unable to prevent the diffusion of ferroelectric to silicon substrate. Direct contact of ferroelectric layer with silicon provides a leakage path for the current to flow and reduced memory window. The 10-nm buffer layer is thick enough to prevent the ferroelectric–silicon interdiffusion and loss of ferroelectric properties, hence improved memory window. An interesting result has been observed for 15-nm buffer layer, where the memory window reduced from 2.03 V in MFeS capacitor to 1.89 V in MFeIS capacitor. Reduced memory window is attributed to the higher voltage drop of the applied gate voltage across the 15-nm buffer layer compared to 10-nm buffer layer. For the MFeIS capacitor with

10-nm buffer layer, PUND and endurance characterization has been carried out and the results obtained are shown in Fig. 8.

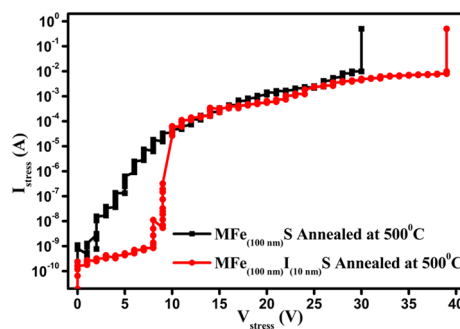
PUND and Psw–Qsw characteristics shows the ferroelectric property of MFeIS structure with no charge degradation upto 10<sup>8</sup> read–write cycles.

A ramp voltage has been applied to investigate the breakdown voltage of the MFeS and MFeIS devices showing maximum memory window, the results obtained are shown in Fig. 9.

MFe<sub>(100 nm)</sub>S and MFe<sub>(100 nm)</sub>I<sub>(10 nm)</sub>S structures annealed at 500 °C show the breakdown voltages of 29 and 39 V, respectively. Enhancement in the breakdown voltage with the buffer layer is due to increase in total dielectric plus ferroelectric thickness, improved Si–Al<sub>2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub>–BiFeO<sub>3</sub> interfaces.

## 4 Conclusion

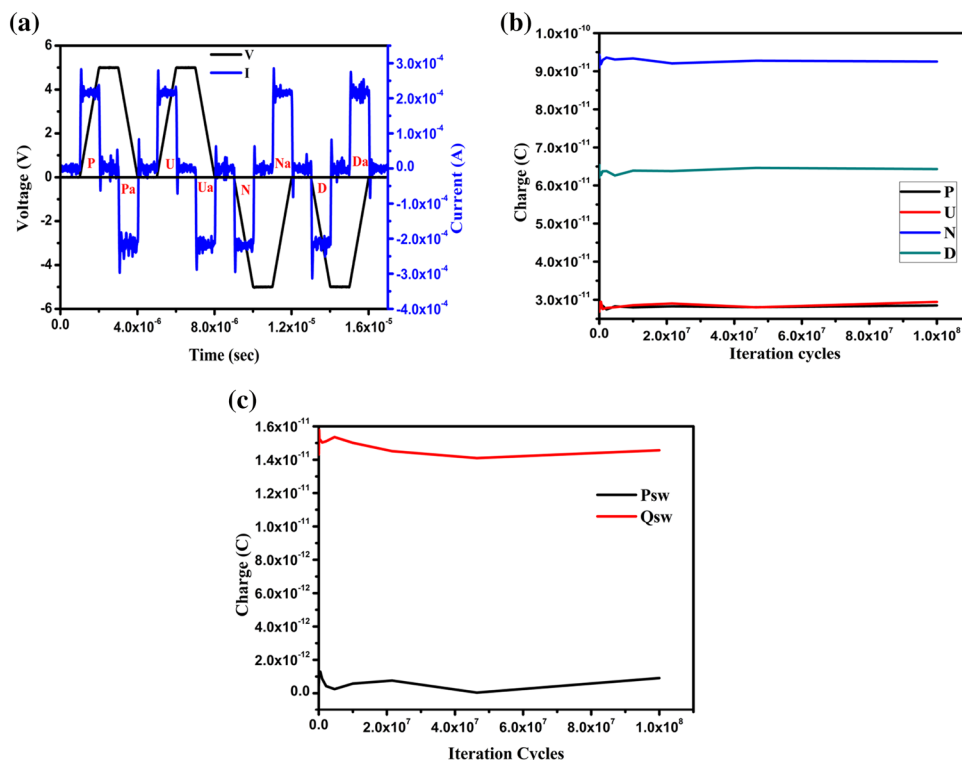
In this work, pure BiFeO<sub>3</sub> film deposited by RF sputtering on the silicon substrate crystallizes for 30 min nitrogen ambient annealing at the temperature of 500 °C. The ferroelectric properties of the BiFeO<sub>3</sub> film have been found very sensitive to the annealing temperature. The crystallized BiFeO<sub>3</sub> film in MFeS structure shows memory window



**Fig. 9** Breakdown voltage of MFe<sub>(100 nm)</sub>S and MFe<sub>(100 nm)</sub>I<sub>(10 nm)</sub>S structure annealed at 500 °C

of 2.03 V at  $\pm 10$  V sweep and remnant charge of  $2.5 \times 10^{-10}$  at 40 V pulse voltage magnitude. Improved memory window of 4.75 V and breakdown voltage of 39 V have been observed in MFeIS structure with 10-nm buffer layer. The Metal/BiFeO<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub>/Si structure shows promising PUND and endurance characteristics with the read–write cycles of 10<sup>8</sup>. The fabricated combination may serve as a promising structure for the future non-volatile ferroelectric memory applications.

**Fig. 8** a, b PUND, and c Psw–Qsw characteristics of MFeIS capacitor structure with 10-nm buffer layer



## References

1. G.G. Teather, L. Young, *Solid State Electron.* **11**, 527 (1968)
2. J.H. McCusker, S.S. Perlman, *IEEE Trans. Electron Devices* **15**, 182 (1968)
3. R. Zuleeg, H.H. Wieder, *Solid State Electron.* **9**, 657 (1966)
4. S.Y. Wu, *IEEE Trans. Electron Devices* **21**, 499 (1974)
5. K. Sugibuchi, Y. Kurogi, N. Endo, *J. Appl. Phys.* **46**, 2877 (1975)
6. O. Auciello, C.A.P. de Araujo, J. Celinska, *Emerg. Non-Volatile Memories* (Springer US, Boston, 2014), pp. 3–35
7. O. Auciello, J.F. Scott, R. Ramesh, *Phys. Today* **51**, 22 (1998)
8. H.M. Duiker, P.D. Beale, J.F. Scott, C.A. Paz de Araujo, B.M. Melnick, J.D. Cuchiaro, L.D. McMillan, *J. Appl. Phys.* **68**, 5783 (1990)
9. C.A.-P. de Araujo, J.D. Cuchiaro, L.D. McMillan, M.C. Scott, J.F. Scott, *Nature* **374**, 627 (1995)
10. R.T. Smith, G.D. Achenbach, R. Gerson, W.J. James, *J. Appl. Phys.* **39**, 70 (1968)
11. C. Michel, J.-M. Moreau, G.D. Achenbach, R. Gerson, W.J. James, *Solid State Commun.* **7**, 701 (1969)
12. J.R. Teague, R. Gerson, W.J. James, *Solid State Commun.* **8**, 1073 (1970)
13. M.M. Kumar, V.R. Palkar, K. Srinivas, S.V. Suryanarayana, *Appl. Phys. Lett.* **76**, 2764 (2000)
14. S. Zheng, J. Wang, J. Zhang, H. Ge, Z. Chen, Y. Gao, *J. Alloys Compd.* **735**, 945 (2018)
15. S.K. Singh, H. Ishiwara, *Jpn. J. Appl. Phys.* **44**, L734 (2005)
16. H. Wu, P. Xue, Y. Lu, X. Zhu, *J. Alloys Compd.* **731**, 471 (2018)
17. K. Ravaliya, A. Ravalia, D.D. Pandya, P.S. Solanki, N.A. Shah, *Thin Solid Films* **645**, 436 (2018)
18. S.M. Selbach, M.-A. Einarsrud, T. Tybell, T. Grande, *J. Am. Ceram. Soc.* **90**, 3430 (2007)
19. C.H. Yang, L.W.M.J. Seidel, S.Y. Kim, P.B. Rossen, P. Yu, M. Gajek, Y.H. Chu, R.R.M.B. Holcomb, Q. He, P. Maksymovych, N. Balke, S.V. Kalinin, A.P. Baddorf, S.R. Basu, *Nat. Mater.* **8**, 485 (2009)
20. W. Ge, A. Rahman, H. Cheng, M. Zhang, J. Liu, Z. Zhang, B. Ye, *J. Magn. Magn. Mater.* **449**, 401 (2017)
21. S. Yang, F. Zhang, X. Xie, H. Sun, L. Zhang, S. Fan, *J. Alloy. Compd.* **734**, 243 (2018)
22. P. Kharel, S. Talebi, B. Ramachandran, A. Dixit, V.M. Naik, M.B. Sahana, C. Sudakar, R. Naik, M.S.R. Rao, G. Lawes, *J. Phys. Condens. Matter* **21**, 953 (2009)
23. K.Y. Yun, D. Ricinschi, T. Kanashima, M. Noda, M. Okuyama, *Jpn. J. Appl. Physics, Part 2 Lett.* **43**, 647 (2004)
24. J. Wang, J.B. Neaton, H. Zheng, V. Nagarajan, S.B. Ogale, B. Liu, D. Viehland, V. Vaithyanathan, D.G. Schlom, U.V. Waghmare, N.A. Spaldin, K.M. Rabe, M. Wuttig, R. Ramesh, *Science (80-)* **299**, 1719 (2003)
25. D.C. Jia, J.H. Xu, H. Ke, W. Wang, Y. Zhou, *J. Eur. Ceram. Soc.* **29**, 3099 (2009)
26. R.-Z. Xiao, Z.-D. Zhang, V.O. Pelenovich, Z.-S. Wang, R. Zhang, H. Li, Y. Liu, Z.-H. Huang, D.-J. Fu, *Chin. Phys. B* **23**, 77504 (2014)
27. Z. Hu, M. Li, Y. Zhu, S. Pu, X. Liu, B. Sebo, X. Zhao, S. Dong, *Appl. Phys. Lett.* **100**, 2 (2012)
28. Y.W. Chiang, J.M. Wu, *Appl. Phys. Lett.* **91**, 2 (2007)
29. P.C. Juan, C.L. Lin, C.H. Liu, C.H. Chen, Y.K. Chang, L.Y. Yeh, *Thin Solid Films* **539**, 360 (2013)
30. P.C. Juan, C.L. Sun, C.H. Liu, C.L. Lin, F.C. Mong, J.H. Huang, H.S. Chang, *Microelectron. Eng.* **109**, 142 (2013)
31. Y. Feng, C. Wang, S. Tian, Y. Zhou, C. Ge, H. Guo, M. He, K. Jin, G. Yang, *Sci. China Phys. Mech. Astron.* **60**, 67711 (2017)
32. J. Robertson, *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.* **18**, 1785 (2000)
33. M. Voigt, M. Sokolowski, *Mater. Sci. Eng. B* **109**, 99 (2004)
34. J. Robertson, *Rep. Prog. Phys.* **69**, 327 (2006)
35. L.E. Black, K.R. McIntosh, *Appl. Phys. Lett.* **100**, 202107 (2012)
36. J. Kolodzey, E.A. Chowdhury, T.N. Adam, G. Qui, I. Rau, J.O. Olowolafe, J.S. Suehle, Y. Chen, *IEEE Trans. Electron Devices* **47**, 121 (2000)
37. X. Lu, *High-K Gate Dielectr. C. Technol* (Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany, 2012), pp. 471–499
38. G.D. Wilk, R.M. Wallace, J.M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001)
39. K.J. Hubbard, D.G. Schlom, *J. Mater. Res.* **11**, 2757 (1996)
40. K.K. Shih, D.B. Dove, *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **12**, 321 (1994)
41. M.H. Suhail, G.M. Rao, S. Mohan, *J. Appl. Phys.* **71**, 1421 (1992)