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Influences of ultrathin amorphous buffer layers on GaAs/Si grown by metal–organic chemical vapor deposition

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Abstract
In this work, a technique for the growth of GaAs epilayers on Si, combining an ultrathin amorphous Si buffer layer and a three-step growth method, has been developed to achieve high crystalline quality for monolithic integration. The influences of the combined technique for the crystalline quality of GaAs on Si are researched in this article. The crystalline quality of GaAs epilayer on Si with the combined technique is investigated by scanning electron microscopy, double crystal X-ray diffraction (DCXRD), photoluminescence, and transmission electron microscopy measurements. By means of this technique, a 1.8-μm-thick high-quality GaAs/Si epilayer was grown by metal–organic chemical vapor deposition. The full-width at half-maximum of the DCXRD rocking curve in the (400) reflection obtained from the GaAs/Si epilayers is about 163 arcsec. Compared with only using three-step growth method, the current technique reduces etch pit density from 3×10^6 cm^{-2} to 1.5×10^5 cm^{-2}. The results demonstrate that the combined technique is an effective approach for reducing dislocation density in GaAs epilayers on Si.

1 Introduction

Increased data throughput in wireless communications and smart phone markets have created huge demand for unprecedented bandwidth and low power consumption between radio frequency and logic devices. This goal could be achieved at low cost by successful monolithic integration of III–V-based optoelectronic devices onto Si-integrated circuits [1, 2]. Therefore, GaAs-on-Si wafers are supposed to have a considerable market potential for the replacement of expensive GaAs wafers in the fabrication of traditional III–V devices (microwave devices, solar cells, photodetectors, lasers, etc.) and monolithic integration of high-performance GaAs devices with high-density Si-integrated circuits. However, the growth of high-quality GaAs epilayers on Si substrates is difficult because of the large lattice and thermal mismatches, 4 and 63%, respectively. In addition, the presence of a polar/non-polar interface leads to anti-phase domain (APD) boundaries which can also make the crystalline quality of the GaAs/Si epilayers deteriorate. Accordingly, GaAs epilayers grown directly on Si substrates usually had a dislocation density of over 10^8 cm^{-2} in early days [3, 4]. The influence of dislocation density on the performance of the GaAs-on-Si devices has been theoretically analyzed, suggesting that the density of these dislocations should be reduced to below 10^5 cm^{-2} in the active region of the devices [5, 6]. Numerous approaches have been reported to reduce the dislocation density in GaAs epilayers on Si, including two-step growth method [7–9], thermal cycle annealing (TCA) [10, 11], strained-layer superlattices (SLS) [12–15], nucleation layers [16, 17], selective area or patterned growth [18–21], three-step growth method [22, 23], dislocation filter with quantum dots [24, 25], and amorphous Si buffer layer [26, 27]. Nevertheless, the SLS involves complicated processes and a relatively low growth rate. The selective area or patterned growth requires further ex situ treatments for substrates and is difficult to adopt for large-scale wafer fabrication. Meanwhile, the dislocation density of GaAs/Si epilayers with three-step growth method is not low enough. Hence, it is necessary to further search for a simpler and more effective method of obtaining high-quality GaAs epilayers on Si.

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In our previous experiments, the three-step growth method has been investigated and high-quality GaAs/Si epilayers was achieved [23]. The three-step growth method is a modified two-step growth method in which an intermediate-temperature (IT) layer is inserted between the low-temperature (LT) layer and the high-temperature (HT) layer. Using the three-step growth method, the surface morphology is greatly improved, but the dislocation density of GaAs epilayers cannot be reduced to as low as 10^5 cm^{-2}. In this article, on the basis of the three-step growth method, an amorphous Si buffer layer is introduced for obtaining higher quality GaAs/Si epilayers. By adding an amorphous Si buffer layer prior to the three-step growth method, the dislocation density in GaAs/Si epilayers can be effectively decreased [26–28]. In addition, the combined method can be applied to large-scale fabrication of wafers by metal–organic chemical vapor deposition (MOCVD).

In this work, a thin amorphous Si film is deposited on a Si substrate firstly. Then, the three-step growth method and TCA are carried out. A low etch pit density (EPD) of about 1.5×10^5 cm^{-2} is achieved in the sample using the combined technique. In addition, the influences of combining amorphous Si buffer layer and three-step growth method on lattice mismatch, thermal mismatch, and dislocation density are investigated in detail. The measurement results show an obvious effect of the proposed technique on reducing the dislocation density.

2 Materials and methods

The growth of GaAs on Si was carried out in a Thomas Swan MOCVD system. The growth experiments were conducted at a constant pressure of 13.3 kPa. The epitaxial structure and growth process of sample A with amorphous Si buffer layer and three-step growth method is shown in Fig. 1a. For comparison, the sample B was grown with only the three-step growth method, as shown in Fig. 1b. 2-inch (001)-oriented Si wafers with 4°-misorientation toward [011] direction were used as the substrates for inhibiting the formation of APD. Before being loaded into the reactor chamber, the substrates were immersed in $NH_3H_2O:H_2O_2:H_2O = 1:1:6$ solution for 12 min and in $HCl:H_2O_2:H_2O = 1:1:6$ solution for 18 min at 75–85 °C, and then dipped in dilute hydrofluoric acid (HF) solution for 10 s to obtain a stable hydrogen-passivated surface. After chemical cleaning, the Si wafers were immediately loaded into the reactor chamber of the MOCVD system, heated up to 220 °C and held for 30 min. Then, the wafers were thermally desorbed to remove native oxide on the surface at 750 °C for 15 min. For comparison, the above experimental procedure of sample A was consistent with that of sample B. After that, the growth process of sample A began. First, the temperature was reduced to 620 °C and a thin amorphous Si buffer layer was deposited using SiH_4 as source reactant. The growth rate was about 0.07 Å/s and the thickness was about 2 nm. Afterwards, the three-step growth method was conducted. For the three-step growth, a 15-nm-thick LT GaAs nucleation layer was grown on the amorphous Si buffer layer at 420 °C; then, a 300-nm-thick IT GaAs epilayer was grown at 630 °C and a 1500-nm-thick HT GaAs epilayer was grown at 685 °C. The growth rates of the LT GaAs nucleation layer, IT GaAs epilayer, and HT GaAs epilayer were 1.3, 6.0, and 6.3 Å/s, respectively. The V/III ratios for these three layers were 248, 68, and 68. To obtain higher crystalline quality of a metamorphic GaAs epilayer, two series of TCA were also inserted in the process of the three-step growth, as shown in Fig. 1a. Each TCA series contains three cycles. In each cycle of the TCA process, the GaAs/Si wafers were first heated to 750 °C. After a 5-min stabilization process, the wafers were cooled down

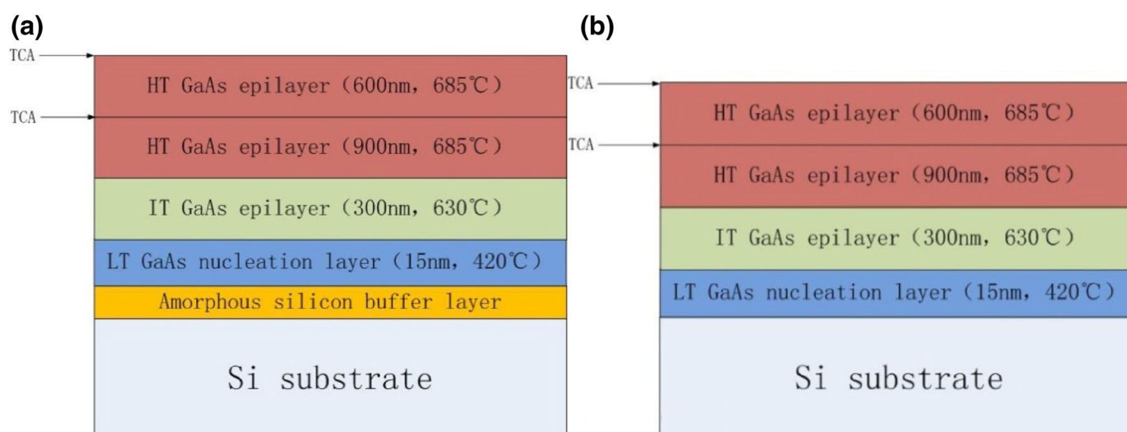

Fig. 1 Schematic of epitaxial structure, growth process, and growth conditions for **a** sample A grown with the amorphous Si buffer layer and three-step growth method and **b** sample B grown with only the three-step growth method

to 350 °C and held for 6 min. During the TCA processes, the GaAs/Si wafers were in AsH_3 and H_2 ambient. The growth process of sample B is identical with that of sample A except the amorphous Si buffer layer, as shown in Fig. 1b.

After growth, the dislocation density in GaAs epilayers was characterized by EPD. The EPD was obtained after etching the samples with molten KOH and observation using scanning electron microscopy (SEM). The crystalline quality of GaAs/si epilayers was also evaluated by double crystal X-ray diffraction (DCXRD) and photoluminescence (PL). In addition, cross-sectional images of the GaAs epilayers and the amorphous Si buffer layer were obtained by the transmission electron microscopy (TEM).

3 Results and discussion

3.1 EPD

The dislocation density of GaAs epilayers on Si was evaluated through EPD obtained using molten KOH etching. Figure 2 shows representative plan view SEM images of the two samples. The EPD was calculated as the average value from five different regions on each sample. The EPD of the sample A is about 1.5×10^5 cm^{-2} and the EPD of sample B is about 3×10^6 cm^{-2}. Compared with the sample B, the EPD of the sample A with the combined method is decreased significantly.

As a result of applying the amorphous Si buffer layer, the LT-GaAs layer can be deposited uniformly over the surface of the amorphous Si layer. The lattice mismatch between them is unnecessary to consider in this case. Hence, the island growth model in the deposition of crystalline GaAs on crystalline Si can be avoided [28, 29]. In the process of the three-step growth, the growth of the IT layer and HT layer is equivalent to providing two in-situ annealing steps to the LT GaAs layer and amorphous Si buffer layer. The LT GaAs layer and amorphous Si buffer layer are crystallized and the mismatch between GaAs and Si can be easily accommodated by the amorphous Si buffer layer [27, 28, 30]. Moreover, the annealing also can make the dislocations glide and annihilate [23]. In this way, the EPD of GaAs epilayers is sharply reduced by the combined technique.

3.2 DCXRD

Figure 3 shows the DCXRD rocking curve in the (400) reflection obtained from the GaAs/Si epilayers and the inset is the magnified view of peaks. The full-width at half-maximum (FWHM) of GaAs (004) diffraction peak is 163 arcsec for sample A, which is lower than sample B of 175 arcsec. The FWHM of GaAs peak related to the threading dislocation density (TDD) is given by [31]:

$$D = \frac{\beta^2}{4.36b^2}. \quad (1)$$

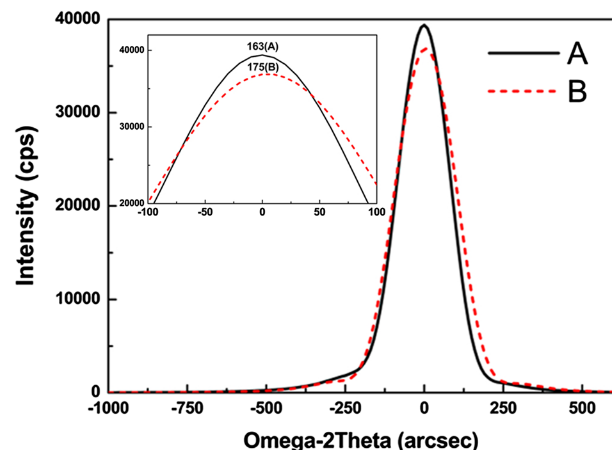

Fig. 3 GaAs (004) rocking curve measured by DCXRD of sample A and sample B, and the inset is the magnified view of peaks

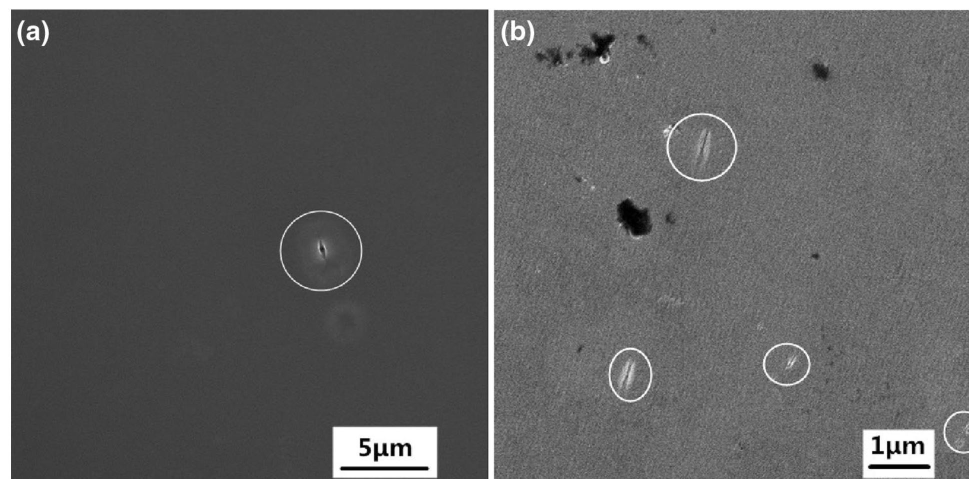

Fig. 2 SEM images of etch pits from **a** sample A and **b** sample B. All the etch pits are marked by the white circles

In Eq. (1), D represents the TDD of the GaAs/Si epilayers, β is the FWHM value of the GaAs/Si epilayers obtained by the DCXRD, and b is the length of Burgers vector. As shown in Fig. 3, the FWHM values of sample A and sample B were 163 arcsec and 175 arcsec. According to Eq. (1), the TDD of sample A decreased by 13.2% in comparison to sample B. The reduction in dislocation density shown in DCXRD results is not as obvious as that in EPD results. The reason for this situation will be explained below.

By applying the combined technique, most of dislocations were confined in the near-interface regions and eliminated from the upper GaAs epilayers. Therefore, there is a significant decrease in dislocation density for the samples with increasing distance from the GaAs/Si interface. The EPD primarily reflects the dislocations in the upper GaAs epilayers, which are mainly threading dislocations. Hence, the EPD value is reduced from 3×10^{6} cm^{-2} to 1.5×10^{5} cm^{-2}. The DCXRD characterizes the crystalline quality of the whole GaAs/Si epilayer. It is affected by dislocations throughout the GaAs epilayer, strain field around dislocations, and other defects, mainly including microtwins and stacking faults [31]. In this work, in addition to the dislocations, there are still a large number of microtwins and stacking faults in the LT GaAs and the amorphous Si buffer layer. These defects exist in a very small region near the interface and only a tiny fraction of dislocations can be seen in the upper layer as shown in the EPD results, but it can influence the DCXRD results yet [9]. In summary, the DCXRD results are affected by more factors than the EPD results. In addition, it is not absolutely consistent with the EPD measurements which show an obvious reduction of dislocation density in GaAs epilayers.

Moreover, based on the test data of DCXRD, the lattice constants of GaAs epilayers along the growth direction were calculated to be about 5.63 Å for sample A and sample B. Compared with the actual lattice constant for GaAs of 5.65 Å, at the room temperature, the lattice constant of GaAs epilayers was diminished in vertical direction of the surface. It is evident that the strain in GaAs epilayers is tensile strain resulting from the thermal mismatch between GaAs and Si.

3.3 PL

Figure 4 displays the PL spectra and the inset shows the magnified view of peaks measured at room temperature with 300-μW excitation power for the two samples. The PL measurements were carried out using a 532-nm continuous-wave diode-pumped solid-state (DPSS) laser for excitation. The excitation beam was focused onto a region of ~2 μm in diameter by a ×100 microscope objective lens on the sample placed in a cryostat. In Fig. 4, the sample A has smaller FWHM value and higher intensity of PL spectrum than that of sample B. These suggest that the uniformity and luminous efficiency of the GaAs epilayer are better in sample A.

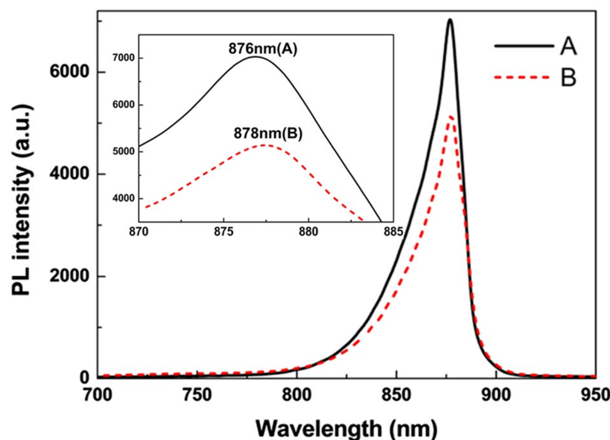

Fig. 4 PL spectra of sample A and sample B, and the inset is the magnified view of peaks

Compared to GaAs, Si has smaller thermal expansion coefficient. Hence, after the whole growth process, the strain resulting from the thermal mismatch is tensile strain which is consistent with DCXRD measurement results, and the peaks in PL spectra are identified as the transitions of electrons from the conduction band to the light-hole valence band [32, 33]. The energy difference between the conduction band and light-hole valence band ΔE_{lh} at the Γ point with respect to the strain ϵ is given as [33]

$$\Delta E_{\mathrm{lh}} = \left[-\frac{2a\left(C_{11}-C_{12}\right)}{C_{11}} + \frac{b\left(C_{11}+2C_{12}\right)}{C_{11}}\right]\varepsilon. \tag{2}$$

For GaAs, the elastic stiffness $C_{11}=11.80\times10^{11}$ dyn/cm^{2} and $C_{12}=5.36\times10^{11}$ dyn/cm^{2}, the hydrostatic deformation potential $a=-9.80$ eV, and the shear deformation potential $b=-2.00$ eV. Therefore, $\Delta E_{\mathrm{lh}}=6.88\epsilon$ (eV). Compared with the GaAs epilayers on GaAs substrates, the red shift of the peak position for sample A is less than that of sample B, as shown in Fig. 4. According to Eq. (2), ΔE_{lh} is 10 meV and $\epsilon=1.45\times10^{-3}$ for sample A, and ΔE_{lh} is 13 meV and $\epsilon=1.89\times10^{-3}$ for sample B. It is evident that the strain in sample A decreased by 23.8% compared to that in sample B. The mechanism of reducing thermal strain remains unknown. These results indicated that the crystalline quality of the GaAs epilayer was improved by the combined method.

3.4 TEM

To confirm the crystalline quality of GaAs/Si epilayers and more clearly observe the performance of the combined method for blocking dislocations, TEM observations are

conducted. The cross-sectional TEM photographs of the crystalline quality and dislocations blocking of sample A and sample B are shown in Fig. 5.

Figure 5a shows the whole growth structure of the GaAs/Si epilayers of sample A with the amorphous Si buffer layer and three-step growth method. The magnification of region I in Fig. 5a is presented in Fig. 5c. Figure 5b shows the TEM image of GaAs/Si epilayer of sample B with only three-step growth method. As it can be seen from Fig. 5a, the vast majority of dislocations are well confined in the near-interface regions, and the minority of the threading dislocations (TDs) propagates into the HT GaAs layer. Using buffer layers and TCA, the residual dislocations can either glide or form dislocation loops and then annihilate, as presented in Fig. 5c [23]. Beyond 1-μm-thick GaAs epilayer on the Si substrate, there are a few threading dislocations which propagate continuously to the upper GaAs epilayer, as shown in Fig. 5a. In Fig. 5b, there are comparatively more dislocations in the near-interface regions than that in Fig. 5a. Many dislocations propagate in the upper GaAs epilayer and deteriorate the crystalline quality.

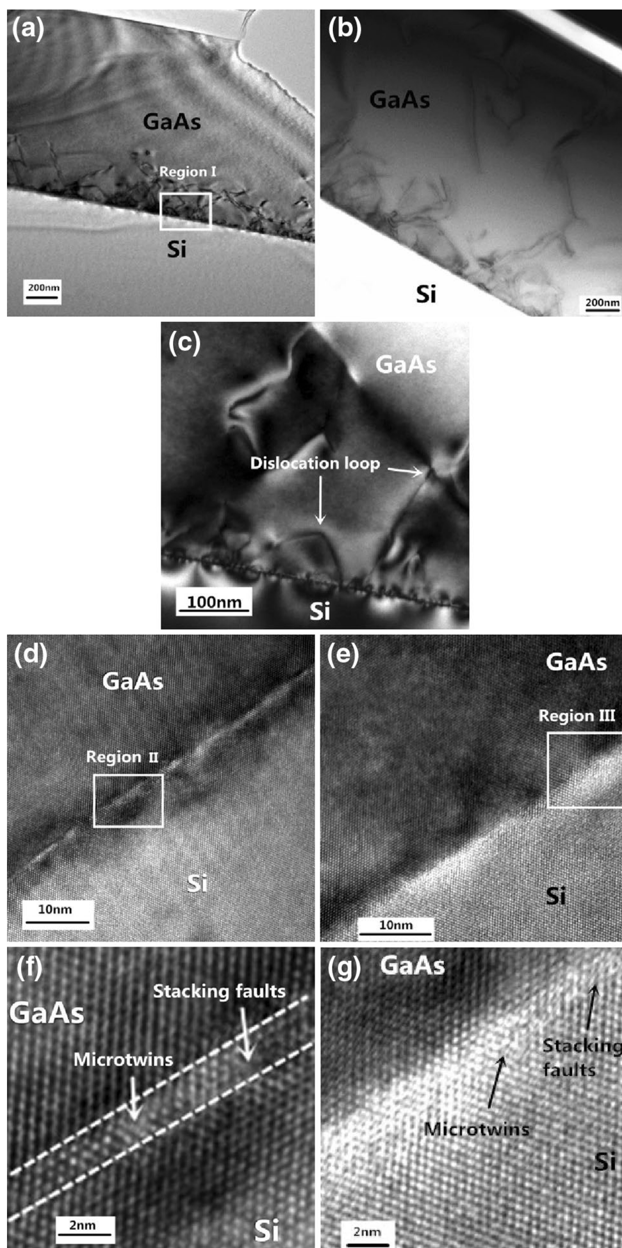

Fig. 5 TEM cross-sectional images of GaAs-on-Si: **a** whole growth structure of sample A; **b** whole growth structure of sample B; **c** magnified view of region I in **a; d** GaAs/Si interface of sample A; **e** GaAs/Si interface of sample B; **f, g** magnified views of region II in (**d**) and region III in (**e**)

Figure 5d, e shows the interface of GaAs/Si of sample A and sample B, and the magnified images of the region II and region III are shown in Fig. 5f, g. In Fig. 5f, the interfaces between GaAs/amorphous Si/Si substrate are atomically sharp. The amorphous Si buffer layer includes three-atomic layers and is about 2-nm thick, and it is indicated by the two white dotted lines. The LT GaAs layer grown on amorphous Si buffer layer has relatively higher crystalline quality, and the interface between the amorphous Si film and the LT GaAs layer is flat. In the amorphous Si buffer layer, defects such as microtwins and bundles of stacking faults are observed, while these defects are confined in the amorphous Si buffer layer and leave a high-quality upper GaAs layer. In Fig. 5e, the GaAs/LT GaAs/Si interface can be seen clearly. A highly defective GaAs region can be observed near the GaAs/Si interface, as shown in Fig. 5g. Compared with sample A, there are greater fluctuations and more defects such as microtwins and stacking faults in the interface of Si and LT GaAs layer. In addition, more dislocations propagated to the upper GaAs layer which is presented in Fig. 5b, e. The above results indicate that the combined method can effectively avoid the island growth model and decrease the dislocation density in the upper GaAs epilayer.

According to the previous experiment works and our results, the probable reason of defect reduction with the combination method is explained as follows. In the whole growth process, a thin amorphous Si film is first grown on a Si substrate at 620 °C. He et al. have proved that at the temperature range of 600–680 °C, the phase of amorphous Si layer is between amorphous and microcrystalline, and the amorphous Si layer includes a large number of microcrystalline grains attached by tissues [30, 34–38]. Then, the thin GaAs film grown at 420 °C is also amorphous [7, 9, 29, 39, 40]. In addition the LT GaAs layer on the amorphous Si layer can be approximately considered as that of an amorphous material deposited uniformly on another amorphous film, in spite of a large lattice mismatch between them [28, 29]. Therefore, the island growth model which occurs in the case of the deposition of crystalline GaAs on crystalline Si can be avoided, as shown in Fig. 5d, f. In the process of

heating to 630 °C, the number of microcrystalline grains in amorphous Si buffer layer would increase as the growth temperature increases [34–38]. Since this amorphous Si layer is very thin, most of the microcrystalline grains have the same orientation as the Si substrate [30]. In the same time, the LT GaAs layer was crystallized by the solid-phase epitaxy process before the growth of IT GaAs layer, whose crystallization can be seeded through microcrystalline grains in amorphous Si buffer layer [7, 9, 29, 30, 34–40]. The lattice mismatch between Si and GaAs can be accommodated by the tissue between microcrystalline grains in the amorphous Si film [27, 28]. Then, the transition of the ultrathin amorphous Si buffer layer to the crystalline phase occurs when the growth temperature continues to rise to more than 680 °C for the growth of HT GaAs layer [30, 34–38]. The remaining misfit between GaAs and Si could be accommodated in this Si layer and cannot affect the GaAs layer. The density of threading dislocations propagating to the upper GaAs epilayers would be reduced, as shown in Fig. 5a. After two series of TCA, the dislocation density can be further decreased [23]. Hence, the vast majority of dislocations can be well confined in the near-interface regions and cannot affect the crystalline quality of the upper GaAs epilayer, as shown in Fig. 5. In general, the combination method can effectively reduce the dislocation density and improve the crystalline quality of GaAs/Si epilayers.

4 Conclusions

We have proposed a method to improve the crystalline quality of GaAs epilayers on Si by combining an amorphous Si buffer layer and three-step growth method. A 1.8-µm-thick metamorphic GaAs/Si with low EPD of 1.5×10^5 cm^{-2} is obtained, and its FWHM of rocking curve for GaAs epilayers is only 163 arcsec. The dislocation behaviors and crystalline quality of the GaAs epilayer are also observed by TEM measurements. These measurement results show that the combined method can effectively block dislocations and improve crystalline quality of GaAs/Si epilayers. However, the surface morphology of GaAs epilayers on Si is not obviously improved. In future experiments, the amorphous Si buffer layer will be further investigated to improve the crystalline quality of III–V semiconductors on Si. We believe that our research can provide a potential way for fabricating low-cost and high-quality GaAs/Si epilayers and making monolithically integrated III–V optoelectronic devices on Si.

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References

1. R. Cipro, T. Baron, M. Martin, J. Moeyaert, S. David, V. Gorbenko, F. Bassani, Y. Bogumilowicz, J.P. Barnes, N. Rochat, V. Loup, C. Vizioz, N. Allouti, N. Chauvin, X.Y. Bao, Z. Ye, J.B. Pin, E. Sanchez, Appl. Phys. Lett. **104**, 262103 (2014)
2. M. Takahasi, Y. Nakata, H. Suzuki, K. Ikeda, M. Kozu, W. Hua, Y. Ohshita, J. Cryst. Growth **378**, 34 (2013)
3. Y.B. Bolkhovityanov, O.P. Pchelyakov, Phys. Usp. **51**, 437 (2008)
4. K.K. Linder, J. Phillips, O. Qasaimeh, X.F. Liu, S. Krishna, P. Bhattacharya, J.C. Jiang, Appl. Phys. Lett. **74**, 1355 (1999)
5. M. Yamaguchi, C. Amano, J. Appl. Phys. **58**, 3601 (1985)
6. S.F. Fang, K. Adomi, S. Iyer, H. Morkoç, H. Zabel, C. Choi, N. Otsuka, J. Appl. Phys. **68**, R31 (1990)
7. M. Akiyama, Y. Kawarada, K. Kaminishi, Jpn. J. Appl. Phys. **23**, L843 (1984)
8. M. Tachikawa, H. Mori, M. Sugo, Y. Itoh, Jpn. J. Appl. Phys. **32**, L1252 (1993)
9. M. Akiyama, Y. Kawarada, T. Ueda, S. Nishi, K. Kaminishi, J. Cryst. Growth **77**, 490 (1986)
10. J.W. Lee, H. Shichijo, H.L. Tsai, R.J. Matyi, Appl. Phys. Lett. **50**, 31 (1987)
11. M. Yamaguchi, M. Tachikawa, Y. Itoh, M. Sugo, S. Kondo, J. Appl. Phys. **68**, 4518 (1990)
12. N.A. El-Masry, J.C. Tarn, N.H. Karam, J. Appl. Phys. **64**, 3672 (1988)
13. R. Fischer, H. Morkoç, D.A. Newmann, H. Zabel, C. Choi, N. Otsuka, M. Longerbone, L.P. Erickson, J. Appl. Phys. **60**, 1640 (1986)
14. T. Soga, S. Hattori, S. Sakai, M. Umeno, J. Cryst. Growth **77**, 498 (1986)
15. T. Soga, T. Imori, M. Umeno, S. Hatori, Jpn. J. Appl. Phys. **26**, L536 (1987)
16. G. Balakrishnan, S. Huang, L.R. Dawson, Y.-C. Xin, P. Conlin, D.L. Huffaker, Appl. Phys. Lett. **86**, 034105 (2005)
17. S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S.N. Elliott, A. Sobiesierski, A.J. Seeds, I. Ross, P.M. Smowton, H. Liu, Nat. Photonics **10**, 307 (2016)
18. S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sana, K. Chocho, Appl. Phys. Lett. **72**, 211 (1998)
19. Y. He, J. Wang, H. Hu, Q. Wang, Y. Huang, X. Ren, Appl. Phys. Lett. **106**, 202105 (2015)
20. S.W. Kim, Y.D. Cho, C.S. Shin, W.K. Park, D.H. Kim, D.H. Ko, J. Cryst. Growth **401**, 319 (2014)
21. H.Y. Yu, S.I. Cheng, J.H. Park, A.K. Okyay, M.C. Onbasli, B. Ercan, Y. Nishi, K.C. Saraswat, Appl. Phys. Lett. **97**, 063503 (2010)
22. S. Nozaki, N. Noto, T. Egawa, A.T. Wu, T. Soga, T. Jimbo, M. Umeno, Jpn. J. Appl. Phys. **29**, 138 (1990)
23. Y. Wang, Q. Wang, Z. Jia, X. Li, C. Deng, Y. Yan, X. Ren, J. Vac. Sci. Technol. B **31**, 051211 (2013)
24. J. Yang, P. Bhattacharya, Z. Mi, IEEE Trans. Electron Devices **54**, 2849 (2007)
25. H. Hu, J. Wang, Y. He, K. Liu, Y. Liu, Q. Wang, X. Duan, Y. Huang, X. Ren, Appl. Phys. A **122**, 588 (2016)
26. M. Ishida, H. Ohyama, S. Sasaki, Y. Yasuda, T. Nishinaga, T. Nakamura, Jpn. J. Appl. Phys. **20**, L541 (1981)
27. W.Y. Uen, Z.Y. Li, Y.C. Huang, M.C. Chen, T.N. Yang, S.M. Lan, C.H. Wu, H.F. Hong, G.C. Chi, J. Cryst. Growth **295**, 103 (2006)

28. J. Wang, H. Hu, Y. He, C. Deng, Q. Wang, X. Duan, Y. Huang, X. Ren, Chin. Phys. Lett. **32**, 088101 (2015)
29. K. Ismail, F. Legoues, N.H. Karam, J. Carter, H.I. Smith, Appl. Phys. Lett. **59**, 2418 (1991)
30. M.S. Hao, J.W. Liang, X.J. Jin, Y.T. Wamg, L.S. Deng, Z.B. Xiao, L.X. Zheng, X.W. Hu, Chin. Phys. Lett. **13**, 42 (1996)
31. J.E. Ayers, J. Cryst. Growth **135**, 71 (1994)
32. P. Zhang, Y. Song, J. Tian, X. Zhang, Z. Zhang, J. Appl. Phys. **105**, 053103 (2009)
33. W. Stolz, F.E.G. Guimaraes, K. Ploog, J. Appl. Phys. **63**, 492 (1988)
34. Y.L. He, X.N. Liu, Acta Electron Sin **4**, 71 (1982)
35. J.A. Reimer, R.W. Vaughan, J.C. Knights, Solid State Commun. **37**, 161 (1981)
36. M. Conradi, R. Norberg, Phys. Rev. B **24**, 2285 (1981)
37. D.E. Polk, J. Non-Cryst. Solids **5**, 365 (1971)
38. Z. Iqbal, S. Veprek, A.P. Webb, P. Capezzuto, Solid State Commun. **37**, 993 (1981)
39. J. Soutadé, C. Fontaine, A. Muñoz-Yagüe, Appl. Phys. Lett. **59**, 1764 (1991)
40. S. Nishi, H. Inomata, M. Akiyama, K. Kaminishi, Jpn. J. Appl. Phys. **24**, L391 (1985)