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Simultaneous ultra-long data retention and low power based on $Ge_{10}Sb_{90}/SiO_2$ multilayer thin films

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Abstract
In this article, $Ge_{10}Sb_{90}/SiO_2$ multilayer thin films were prepared to improve thermal stability and data retention for phase change memory. Compared with $Ge_{10}Sb_{90}$ monolayer thin film, $Ge_{10}Sb_{90}$ (1 nm)/SiO_2 (9 nm) multilayer thin film had higher crystallization temperature and resistance contrast between amorphous and crystalline states. Annealed $Ge_{10}Sb_{90}$ (1 nm)/SiO_2 (9 nm) had uniform grain with the size of 15.71 nm. After annealing, the root-mean-square surface roughness for $Ge_{10}Sb_{90}$ (1 nm)/SiO_2 (9 nm) thin film increased slightly from 0.45 to 0.53 nm. The amorphization time for $Ge_{10}Sb_{90}$ (1 nm)/SiO_2 (9 nm) thin film (2.29 ns) is shorter than $Ge_2Sb_2Te_5$ (3.56 ns). The threshold voltage of a cell based on $Ge_{10}Sb_{90}$ (1 nm)/SiO_2 (9 nm) (3.57 V) was smaller than GST (4.18 V). The results indicated that $Ge_{10}Sb_{90}/SiO_2$ was a promising phase change thin film with high thermal ability and low power consumption for phase change memory application.

1 Introduction

It is well known that phase change memory (PCM) is deemed as one of most promising candidates for next-generation non-volatile memory because of its high scalability, ultra-fast speed, and good compatibility with complementary metal-oxide semiconductor (CMOS) technology [1, 2]. $Ge_2Sb_2Te_5$ (GST) is the most widely investigated phase change thin film for PCM applications due to its excellent comprehensive performance. However, GST still has some shortcomings, including the poor data retention (85 °C for 10 years) and long crystallization time (~ 100 ns in SET process) [3–5]. Recently, Sb-rich GeSb (GS) thin film was found to display superior characteristics for PCM application [6]. For instance, GS thin film has high phase change speed due to its specific crystallization mechanism. Meanwhile, GS thin film contains no volatile Te element which will not pollute the product line. Our former studies show that PCM devices based on the multilayer thin films such as SbSe/GaSb [7], SnSb/GaSb [8], GST/Sb [9], can dramatically improve thermal stability as well as power consumption [10].

In order to further optimize the phase change characteristic of GS thin film, the SiO_2 was selected to composite with GS by the multilayer method in this work. The investigations of resistance versus temperature (*R*–*T*), X-ray diffraction (XRD) and surface topography measurements were carried out. The effect of the adding of SiO_2 layers on the thermal stability, crystallization characteristics, and optical transition of GS/SO phase-change thin film was analyzed in detail.

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2 Experimental methods

GS/SO multilayer thin films with different periods and thickness rations were deposited on 0.5 mm thick oxidized Si (100) wafers using a radio-frequency (RF) magnetron sputtering system at room temperature. Before the growth of GS/SO multilayer thin films, the deposition rates of GeSb and SiO_2 were determined and the thickness of each individual layer was designed by controlling the sputtering time. For comparing, monolayer GS and GST thin films were also prepared. The total thickness of monolayer GS and multilayer

GS/SO thin films was set to 50 nm and the periodicity was 5. The purity of GeSb and SiO_2 targets was 99.999%. The power density was 1.48 W/cm^2 on the sputtering targets. Magnetron sputtering apparatus needed to be vacuum and the pressure of magnetron sputtering apparatus was 4×10^{-4} Pa before sputtering. Subsequently, the deposition process was carried out in an Ar atmosphere at a pressure of 0.4 Pa with gas flow of 30 sccm (sccm denotes standard cubic centimeter per minute at STP) and radio frequency power of 30 W. An automatic rotation of 20 rpm for the substrate was used for well-proportioned deposition.

The resistance as a function of temperature (*R*–*T*) was measured using the *in situ* measurement with a heating rate of 30 °C/min. The sample temperature was measured by a Pt-100 thermocouple located at a heating stage controlled by a TP 94 temperature controller (Linkam Scientific Instruments Ltd, Surrey, UK). The optical band gap was measured by NIR spectrophotometer. The phase structures of the films annealed at various temperatures were investigated by XRD analysis using Cu Ka radiation in the 2θ range from 20° to 60°, with a scanning step of 0.01°. Roughness on the surface of the films was examined by atomic force microscopy (AFM, FM-Nanoview 1000). A picosecond laser pump–probe system was used for real-time reflectivity measurement. The light source used for irradiating the samples was a frequency-doubled model-locked neodymium yttrium aluminum garnet laser operating at 532 nm wave-length with a pulse duration of 30 ps. Samples with a thickness of 50 nm were prepared for X-ray reflectometry (XRR) measurement to estimate the film density change during crystallization. The device properties of PCM cell were measured using a Tektronix AWG5012B arbitrary waveform generator and a Keithley 2602 A parameter analyzer.

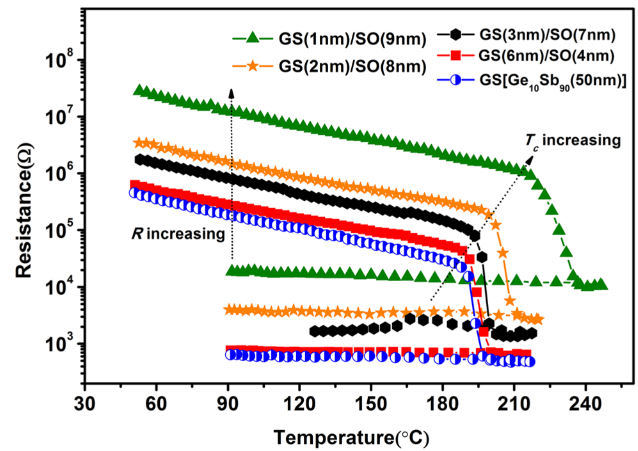

Fig. 1 The resistance as functions of temperature of GS monolayer thin film and GS/SO composite multilayer thin films with a heating rate of 30 °C/min

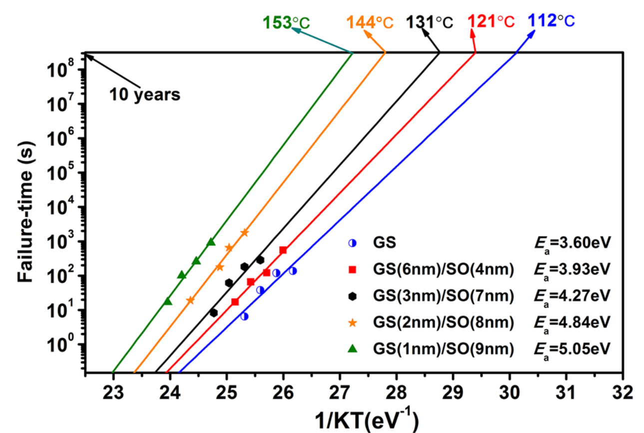

Fig. 2 Plots of failure times as a function of reciprocal temperature of GS monolayer thin film and GS/SO multilayer thin films

3 Results and discussion

Figure 1 shows that the variation in the resistance is a function of the heating temperature for monolayer GS and multilayer GS/SO thin films. Initially, all thin films display high resistance values, which can be attributed to semiconductor behavior. Then, the resistance decreases sharply when the temperature reaches a certain value which is regarded as the crystallization temperature T_c. With increase of the thickness of SiO_2, the T_c of GS/SO thin films become higher than GS. Subsequently, as we can see in Fig. 1, the T_c for GS, GS (6 nm)/SO (4 nm), GS (3 nm)/SO (7 nm), GS (2 nm)/SO (8 nm), and GS (1 nm)/SO (9 nm) thin films are 187, 190, 194, 199, and 218 °C, respectively. Generally, the thermal stability can be evaluated by the crystallization temperature roughly. Thus, GS/SO multilayer thin films have better thermal stability than GS. Furthermore, the crystalline resistances of GS/SO thin films increase with the thickness of SiO_2 layer. According to the joule heat $Q = I^2 \times R \times t$ [11], a higher crystallization resistance can improve the heating efficiency and decrease the power consumption in RESET operation process. Besides, the resistance difference for GS/SO thin films between amorphous and crystalline state is more than three orders of magnitude, which is enough for PCM application.

The plot of logarithm failure time versus $1/k_bT$, exhibited in Fig. 2, fits a linear Arrhenius relationship because of its thermal activation nature. The linear relationship is described as follows:

$$t = \tau_0 \exp\left(E_a / k_b T\right), \tag{1}$$

where t, τ_0, k_b, and T are failure time, a pre-exponential factor depending on the thin film's properties, Boltzmann constant and absolute temperature, respectively [12]. Accordingly,

the extrapolated temperatures of 10-year retention lifetime for above phase-change thin films can be achieved as 112, 121, 131, 144, and 153 °C. That is, the adding of SiO_2 layers thickness enhances the amorphous thermal stability of GS thin films. Generally, the activation energy for crystallization E_a is a significant index, which can evaluate the difficulty for the crystallization. The E_a of GS, GS (6 nm)/SO (4 nm), GS (3 nm)/SO (7 nm), GS (2 nm)/SO (8 nm), and GS (1 nm)/SO (9 nm) thin film, obtained from the slope of Fig. 2, was3.60 ~ 5.05 eV. From this perspective, GS/SO multilayer thin films possess a more reliable resistance state to meet the application of data storage at elevated temperature.

The diffuse reflectivity spectra of amorphous monolayer GS and GS/SO multilayer thin films were shown in Fig. 3 measured at room temperature by NIR UV-visible-NIR spectrophotometry in the wavelength range from 400 to 2500 nm [13]. The optical band gap (E_g) is determined by extrapolating the absorption edge onto the energy axis [14], wherein the conversion of the reflectivity to absorbance data is obtained by the Kubelka–Munk function (K–M) [15]:

$$K/S = (1 - R)^2 / (2R), \quad (2)$$

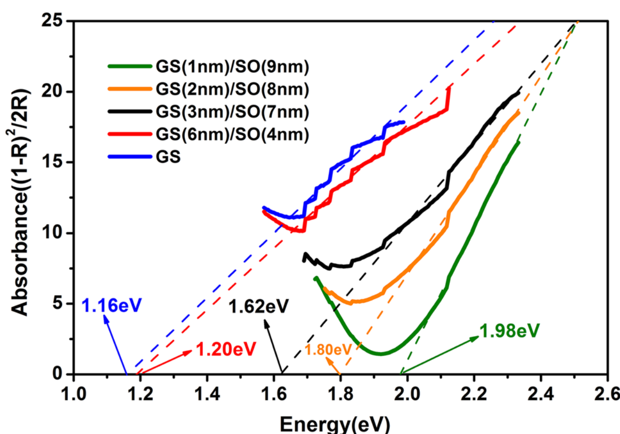

Fig. 3 The Kubelka–Munk function of amorphous GS monolayer thin film and GS/SO multilayer thin films

where R, K, and S are the reflectivity, absorption coefficient and scattering coefficient, respectively. As shown in Fig. 3, the band gap energy for GS (4 nm)/SO (6 nm), GS (3 nm)/SO (7 nm), GS (2 nm)/SO (8 nm) and GS (1 nm)/SO (9 nm) thin films are 1.20, 1.62, 1.80 and 1.98 eV, respectively, which are all larger than that of GS (1.16 eV). The dependent temperature for the conductivity in a semiconductor can be explained according to $\rho = \rho_0 \exp(-E_\sigma/kT)$, where ρ is conductivity, ρ_0 is a pre-exponential factor and E_σ is the activation energy for electrical conduction [16]. The activation energy of electrical transport is simply measured by half of the band gap $E_\sigma = E_g/2 + \Delta E$, where $E_g/2$ is the distance from the Fermi level to the conduction band and ΔE is depth of the trap states [17]. An increase in the band gap will lead to the decrease of carriers, which make a major contribution to the increase of film resistivity. Therefore, this finding is in conformity with the trends of resistance curves for GS and GS/SO thin films.

Figure 4a, b display the XRD patterns of GS and GS (1 nm)/SO (9 nm) thin films, respectively. At first, no clear diffraction peaks were observed for both GS and GS (1 nm)/SO (9 nm) thin films below the temperature 160 °C. It hints that the deposited GS and GS (1 nm)/SO (9 nm) thin films are in amorphous structure. The diffraction peaks (012) and (110) of Sb phase in GS thin film become sharp and intense with the increasing of annealing temperature, representing its enhanced crystalline nature. Nevertheless, being different from GS, only a fuzzy diffraction peak (110) of Sb phase is identifiable in GS (1 nm)/SO (9 nm) at 187 °C. Two weak peaks of (012) and (110) exist at 196 and 270 °C annealed GS (1 nm)/SO (9 nm) in Fig. 4b. These results illustrate that a large amount of Sb phase exist in GS thin films which is conducive to improve the crystallization rate by using the growth-dominated crystallization mechanism of Sb. Besides, no diffraction peaks belonging to SiO_2 are observed in Fig. 4b, indicating the existence of SiO_2 in amorphous state. The crystallization of GS (1 nm)/SO (9 nm) multilayer thin film is obviously inhibited by SiO_2 layers, resulting in its better amorphous thermal stability. From the main peak at around 28.6°, the average grain size of annealed GS (1 nm)/

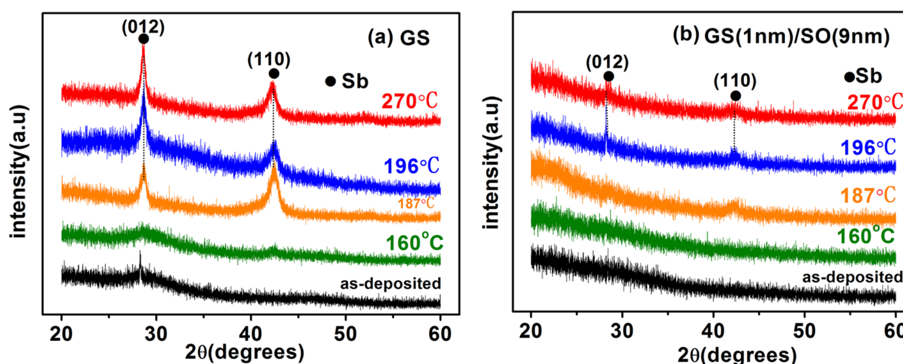

Fig. 4 XRD patterns of **a** GS, **b** GS (1 nm)/SO (9 nm) thin films annealed at different temperature for 10 min in Ar atmosphere

SO (9 nm) thin film is approximately 15.71 nm calculated utilizing the Scherrer equation, assuming no stress effect:

$$D_{hkt} = 0.943\lambda/(\beta \cos\theta), \quad (3)$$

where λ is wavelength of the X-ray, β is the full-width-at-half-maximum (FWHM), and θ is the diffraction angle [18]. It reveals that the grain size of GS (1 nm)/SO (9 nm) increases along with the annealing temperature but not so distinctly as the GS. It is known that the smaller grain produces more grain boundaries, which brings enhancing electron scattering, thus leading to a higher resistance. This result is in concert with Fig. 1.

It is the surface roughness of phase change film that is very significant for device performance by influencing the quality of the electrode-film interface. The phase change of GS and GS (1 nm)/SO (9 nm) thin films is accompanied by an induced internal stress. Figure 5a–d exhibit the AFM images of as-deposited and annealed GS and GS (1 nm)/SO (9 nm) thin films. The surface of amorphous GS and GS (1 nm)/SO (9 nm) thin films are smooth relatively, with the root-mean-square (RMS) surface roughness 0.51 and 0.45 nm, respectively. After crystallization, the RMS of GS increases to 1.02 nm. By contrast, the annealed GS (1 nm)/SO (9 nm) has a smaller RMS (0.53 nm). From above points, it implies that the internal stress change of GS (1 nm)/SO (9 nm) thin film is much smaller, which is beneficial for the fatigue performance of phase change memory.

The dramatic resistivity change is accompanied by the optical reflectivity in the reverse transformation. The evolution of reflectivity from crystalline to amorphous state is measured by the picosecond pulse intended to study the reverse transformation power consumption. In a nutshell, the operation speed and the power of PCM are bound up with the SET speed and the RESET power because the SET operation needs lower power but much longer time compared with the RESET one. Figure 6a, b shows that the reflectivity of GS (1 nm)/SO (9 nm) and GST thin films maintains a high value until a sudden drop, corresponding to the crystalline-to-amorphous state transition. The time of amorphization process for GS (1 nm)/SO (9 nm) and GST thin films is 2.29 and 3.56 ns with the same irradiation fluence of 9.7 mJ/cm^2.

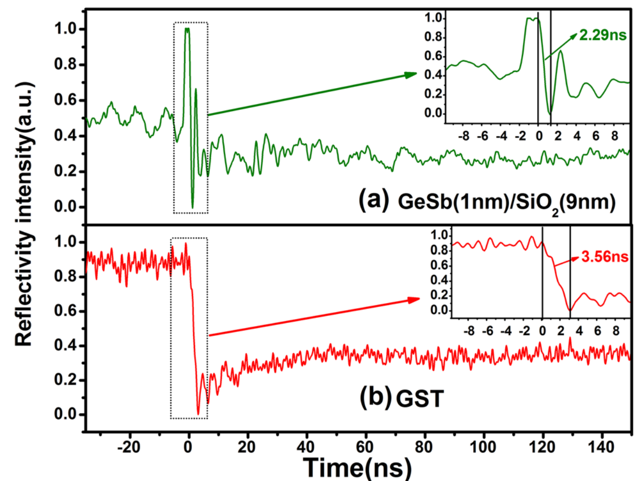

Fig. 6 **a, b** Reflectivity evolutions in the amorphization process for GS (1 nm)/SO (9 nm) and GST thin films

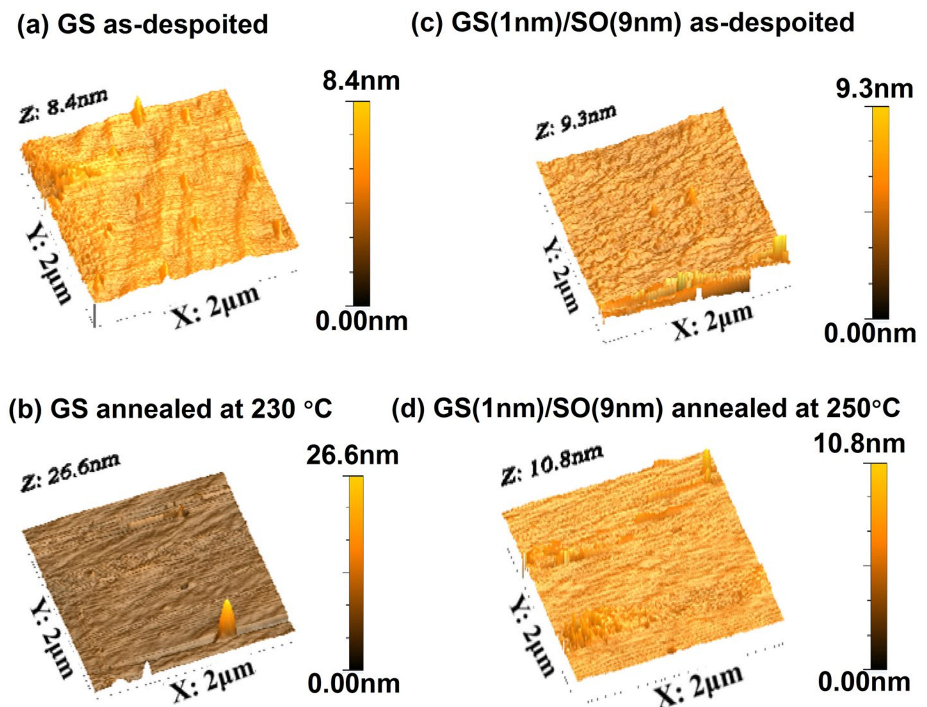

Fig. 5 AFM topographic images of **a** as-deposited GS, **b** annealed GS at 230 °C, **c** as-deposited GS (1 nm)/SO (9 nm), **d** annealed GS (1 nm)/SO (9 nm) at 250 °C

It demonstrates that GS (1 nm)/SO (9 nm) thin film has a lower power consumption than GST. This can owe to the lower thermal conductivity, higher resistivity and smaller grain size of multilayer thin films.

XRR patterns of the amorphous and crystalline GS (1 nm)/SO (9 nm) thin films are shown in Fig. 7a. It is well known that the density change upon amorphous-to-crystalline phase transition will affect the interfacial stress and reliability of contact between the phase-change layer (PLC) and electrode. The reflection peak of GS (1 nm)/SO (9 nm) thin film moves toward a higher angle after the phase transformation from amorphous-to-crystalline phase. It implies that crystalline GS (1 nm)/SO (9 nm) thin film has a higher density than the amorphous one. The modified Bragg's equation is written as [19]:

$$\sin^2\theta_m = 2\delta + (m + \Delta m)^2(\lambda/2t)^2, \quad (4)$$

where δ, m ($m = 1, 2, 3...$), λ, t, and m are a constant, reflection series, wavelength of Cu-Kα radiation (0.154 nm), thin film thickness, and correction factor, respectively. The value of Δm is 0.5, which corresponds to the smallest or largest intensity of XRR pattern for every reflection series. Figure 6b exhibits plot of f $\sin^2\theta_m$ versus $(m + \Delta m)^2$ for thin film thickness change. The connection between t and slop of fitted line (k) is gained by

$$t = \lambda/2\sqrt{k}. \quad (5)$$

The thin film thickness reduction under crystallization is calculated to be 5.4%, which is smaller than that of GST (6.5%) [20]. If no element is lost through evaporation, the thickness reduction compares well with the density change. It illustrates that GS (1 nm)/SO (9 nm) thin film has a smaller density change than GST, which is adaptive for the reliability of interface between PCL and electrode for PCM.

The scanning electron microscope of PCM device cells is shown in Fig. 8a. The current–voltage (I–V) curves of the PCM cells for GS (1 nm)/SO (9 nm) and GST thin films are measured. An obvious threshold switching from a high resistivity state to a low resistivity state can be seen beyond

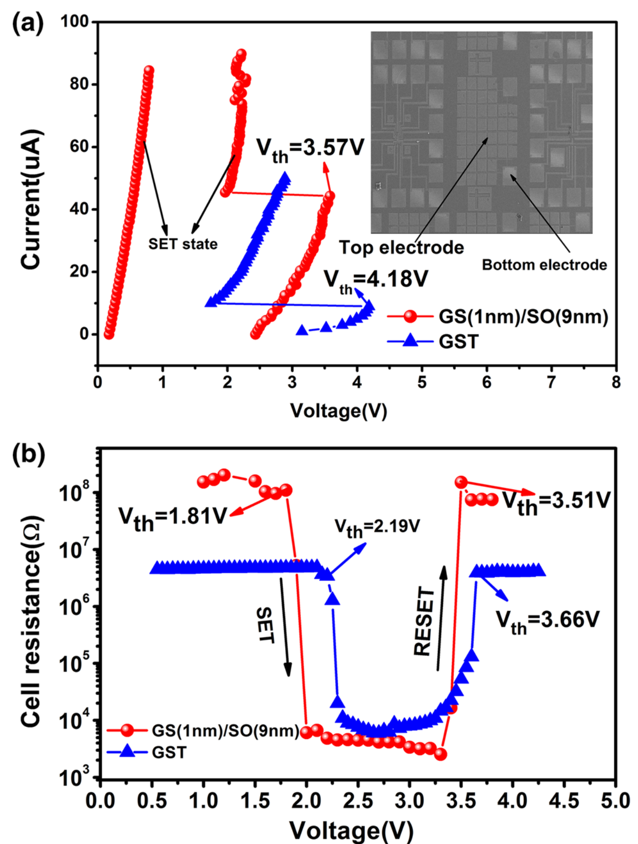

Fig. 8 **a** I–V curves of the PCM cells based on the GS (1 nm)/SO (9 nm) and GST thin films. The inset shows the scanning electron microscope of PCM device cells. **b** R–V curves of the PCM cells based on the GS (1 nm)/SO (9 nm) and GST thin films

the threshold voltage (V_{th}). The V_{th} of GS (1 nm)/SO (9 nm) and GST thin films is 3.57 and 4.18 V, respectively. The SET and RESET operations can be implemented by the electrical pulse, shown in Fig. 8b. The resistance ratio of RESET to SET state for GS (1 nm)/SO (9 nm) multilayer thin film reaches four orders of magnitude. At the application of 100 ns electric pulse, the switching voltages of SET and RESET operations for GS (1 nm)/SO (9 nm) multilayer thin film are 1.81 and 3.51 V, respectively, which are smaller

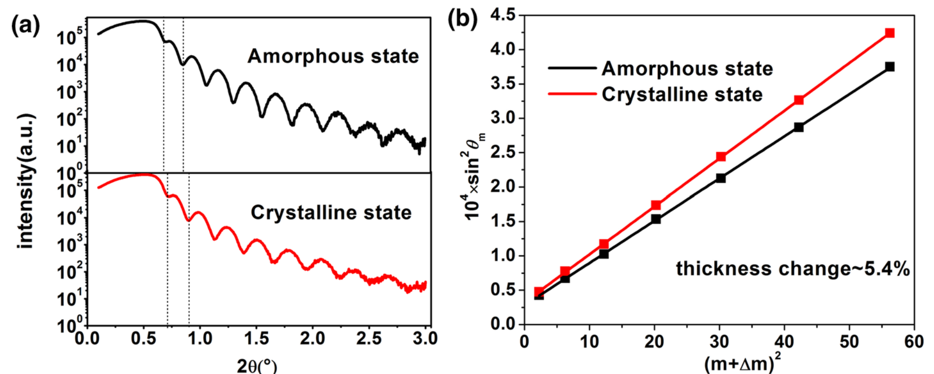

Fig. 7 **a** XRR patterns of the amorphous and crystalline GS (1 nm)/SO (9 nm) thin films; **b** plot of $\sin^2\theta_m$ versus $(m + \Delta m)^2$ for film thickness change

than those of GST (2.19 and 3.66 V). The switching energy for RESET operation E_{reset} is a vey important index, which can be estimated by [21]:

$$E_{RESET} = U^2{}_{RESET} \times t/R_{SET}, \tag{6}$$

where R_{SET} is the SET resistance, t is the pulse width, and U_{RESET} is the RESET voltage. The energy of the RESET operation for GS (1 nm)/SO (9 nm)-based device is calculated to be around 3.51×10^{-10} J, which is lower than that of GST cell (9.7×10^{-9} J). GS (1 nm)/SO (9 nm) multilayer thin films with lower power consumption can be acquired from above points.

4 Conclusions

Compared with GS monolayer thin film, GS/SO multilayer thin film has higher crystallization temperature (190 ~ 218 °C) and larger crystalline state resistance, which means a better thermal stability. The RMS surface roughness for crystalline GS (1 nm)/SO (9 nm) thin film (0.5369 nm) is smaller than GS (1.02 nm). The picosecond pulse laser measurement shows that the GS (1 nm)/SO (9 nm) multilayer thin film has a shorter amorphization time (2.29 ns) than GST (3.56 ns). Its density change upon amorphous-to-crystalline transition is about 5.4%. The energy for the RESET operation of GS (1 nm)/SO (9 nm) cell is 3.51×10^{-10} J. It implies that GS/SO multilayer thin film is a promising candidate for PCM application on account of its long data retention and low power consumption.

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