Appl. Phys. A (2017) 123:356
DOI 10.1007/s00339-017-0973-7

Applied Physics A
Materials Science & Processing

Impact of threshold voltage variation on 1S1R crossbar array with threshold switching selectors

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Received: 11 January 2017 / Accepted: 11 April 2017 / Published online: 18 April 2017

Abstract It is important that selector achieves voltage compatibility with paired resistive random access memory element. Nevertheless, unsatisfactory uniformity existing in practical selector devices will lead to serious problems during operation. This paper investigates the potential impact of threshold voltage variation on crossbar array with one-selector one-resistor cell. We prove that large variation of threshold voltage may lead to unintentional writing during read process. Therefore, we propose a method to determine selectors' threshold voltage range within 1/2 or 1/3 bias scheme. Results indicate tolerable threshold voltage range basically expands with the increasing OFF-resistance or decreasing ON-resistance of selectors. The proposed method gives a guideline for choosing and fabricating appropriate selectors for RRAM elements with specific parameters.

1 Introduction

Sneak current issue of crossbar RRAM array is one of the main obstacles for the high-density memory application. It can be effectively tackled by the addition of necessary non-linearity to the RRAM by integrating a highly non-linear and bidirectional selector device. This topology is known as the 1S1R architecture [1–3].

Among selectors based on various mechanisms, threshold switching selectors are widely concerned because of large non-linearity and large drive current in the ON-state, including ovonic threshold switch (OTS) [4–12], metal–insulator transition switch (MIT) [13–16], field-assisted super-linear threshold switch (FAST) [17, 18], programmable metallization switch [19–25] and threshold vacuum switch (TVS) [26]. As Fig. 1, during forward voltage sweeps, it maintains high-resistive state (OFF-state) before threshold voltage (V_{th}) is achieved. When applied voltage surpasses threshold voltage, an abrupt and reversible transition occurs to conductive state (ON-state). During reverse sweeps, it transits to OFF-state after applied voltage is less than hold voltage (V_{hold}).

To investigate the impact of selector characteristics on the 1S1R crossbar array performance, IMEC compare various selectors and demonstrate that threshold voltage and ON-state resistance (R_{s_on}) are crucial parameters [26]. Nonetheless, the research is based on ideal circumstance, which did not take devices variation into consideration. Although it has not been emphasized, variation of threshold voltage is a common phenomenon in established literature [5, 6, 26, 26]. Unsatisfactory variation of reported selectors will lead to serious problems during operation. Consequently, novel operation scheme enabling easy integration of selector and memory is proposed by He et al. to remove the rigid voltage-matching requirements [26]. Nonetheless, it needs two adjoined pulses to implement operation and neglect the variation of devices, as well. In this work, we discuss the impact of threshold voltage variation on array performance. Meanwhile, a method is proposed to determine appropriate threshold voltage range within 1/2 and 1/3 bias scheme. The simulation is implemented by utilizing matrix algebra with MATLAB [26].

This paper is organized as follows. The simulation settings are presented in Sect. 2. The impact of threshold voltage variation on array performance is analyzed in

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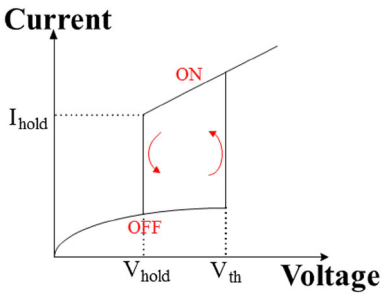

Fig. 1 Schematic behavior of threshold switching selectors in voltage sweeps

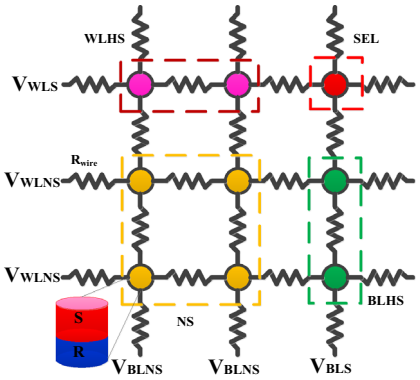

Fig. 2 Schematic of 2-D cross-point array. *SEL* selected cell, *WLHS* WL half-selected cell, *BLHS* BL half-selected cell, *NS* non-selected cell, *WLS* selected WL, *BLS* selected BL, *WLNS* WL unselected, *BLNS* BL unselected, R_{wire} 5 Ω/cell [26]

Sect. 3. In Sect. 4, appropriate threshold voltage range is determined. The conclusion is given in Sect. 5.

2 Simulation setup

2.1 Array configuration

As in Fig. 2, wordlines (WL) perpendicularly intersect with bitlines (BL) in a crossbar array with 1S1R cells built at the junctions. All RRAM elements are identical, while threshold voltage of selectors is variable. Simulation is implemented using the worst case scenario for different read and write operation modes (Table 1). The selected cell is located at the farthest distance from voltage source and ground. 1/2 and 1/3 bias schemes are adopted for single-bit read and write operation. Default line resistance is fixed at 5 Ω/cell.

Array performance for read or write operation can be evaluated by read margin (RM), write margin (WM), read power (Pr) and write power (Pw). Read margin is defined as the ratio of readout disparity between HRS and LRS states over readout of LRS state. Write margin is defined as the ratio of voltage drop on selected RRAM over applied voltage. Read power and write power is the total power consumption of array in read and write process, respectively.

2.2 RRAM model

The RRAM device structure is usually a resistive switching layer sandwiched between two electrodes. As shown in Fig. 3a, RRAM device can switch between a high-resistance (HRS) and a low-resistance state (LRS) by applying opposite voltage. In our mathematic model, LRS/HRS are assumed being linear, where R_{HRS} and R_{LRS} are fixed at 500 and 50 kΩ, respectively. It leads HRS/LRS resistance ratio equals to 10, which represents a typical resistance ratio for HfOx-based RRAM device [26]. The parameterized RRAM has symmetrical set and reset voltages of ±1.5 V. Nonetheless, unintentional switching of practical devices occurs occasionally when applied voltage is less than write voltage. Disturb voltage is defined to determine the maximum voltage drop on the RRAM element, beyond which the element state may change unintentionally. At this stage, default disturb voltage value is set to 1.0 V.

2.3 Selector model

Three parameters are employed to describe the threshold switching selectors, namely threshold voltage (V_{th}), OFF-resistance (R_{s_off}) and ON-resistance (R_{s_on}). Like RRAM element, there are two distinct states existing in threshold switching selectors, namely OFF-state and ON-state. Take ovonic threshold switch for example, the Poole–Frenkel (P–F) conduction mechanism accurately accounts for the I–

Table 1 Worst case data pattern

	Set	Reset	Read '0'	Read '1'
RRAM	SEL: HRS	ALL LRS	SEL: HRS	SEL: HRS
	WLHS: LRS		WLHS: LRS	WLHS: LRS
	BLHS: LRS		BLHS: LRS	BLHS: HRS
	NS: LRS		NS: LRS	NS: LRS
Threshold switching selector	SEL: maximum threshold voltage (V_{th_max})			
	Others: minimum threshold voltage (V_{th_min})			

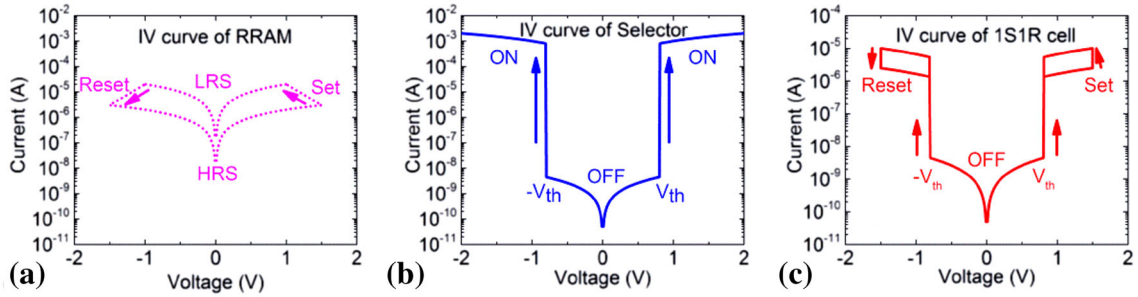

Fig. 3 Schematic IV curve of **a** RRAM element, **b** threshold switching selector, **c** 1S1R memory cell. The sneak path current is largely suppressed by the selector

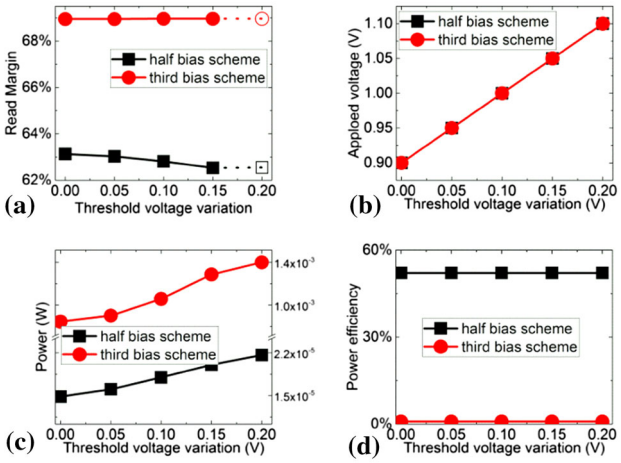

Fig. 4 Relationship between read performance with threshold voltage variation in 1/2 or 1/3 bias scheme

V characteristics in the OFF-state regime [6]. While in the ON-state regime, it is widely thought as ohmic because of linear I–V behavior (Fig. 3b). The current of OFF-state is usually millesimal or even smaller of the ON-state current. For simplicity, in our model, OFF-state is also regarded as linear. The non-linearity (NL) of selectors is defined as OFF-/ON-resistance ratio ranging from 1e3 to 1e5. Previous studies alleged that non-linearity can even attain 1e7 [4, 5], which is promising for high-density array applications. In this case, once the selector is turned to ON-state, it will keep this state till the applied voltage is removed.

3 Analysis of impact of threshold voltage variation on array performance

3.1 Possible adverse outcomes

As in Table 1, variability of threshold voltage is expressed by the worst case scenario. In the array, selected selector possesses maximum threshold voltage (V_{th_max}) while others possess minimum threshold voltage (V_{th_min}). This will lead to serious problem during operation.

During set/reset operations, large applied voltage is required to switch selected RRAM element. Thus, partial bias voltage drop on unselected selector is likely to be larger than V_{th_min}. This may lead to unselected selectors turn on. On one hand, ON-state selectors are not able to limit the current of the unselected elements. Leakage current results in the reduction of voltage in selected wordline. Consequently, it reduces voltage drop on selected cell and fail the operation. On the other hand, unintentional ON-state selector may result in wrongly writing of unselected RRAM element because most of the voltage drops over the RRAM.

During read operation, larger applied voltage for selected cell is demanded for larger V_{th_max}. It may lead to unintentional writing of selected RRAM element because most of the voltage will drop on RRAM after selector turns on. In addition, non-selected selectors with V_{th_min} may wrongly turn on and increase the readout current. This will make read margin less sharp and even induce wrong read results mixing HRS with LRS. In other cases, HRS is attained if applied voltage is not enough to turn on the selected selector regardless of the real state.

3.2 Simulation verification

Compared to set/reset operation, impact of V_{th} variation on read operation is more severe. Worst outcomes in set/reset operation may occur in read operation as well. Thus, this subsection aims at providing the evidence that V_{th} variation may induce wrong results by simulating read operation.

A threshold switching selector is designed with threshold voltage of 0.8 V. OFF-resistance and ON-resistance are set to 1e8 and 1e4 Ω, respectively. The non-linearity is 10^4 enough for the 1 Mb array if no variation of threshold voltage is taken into account [26]. In fact, variation apparently occurs among devices. Thus, it is necessary to study the relationship between read performance and threshold voltage variation within different bias schemes (

Fig. 4). In Fig. 4a, read margin barely changes with the increase of threshold voltage variation. In the meantime, applied voltage, needed to turn on the selector, increases with the rising variation in Fig. 4b. However, there is a problem when the variation increases to 0.2 V. According to aforementioned definition, variation of 0.2 V means minimum and maximum threshold voltage is 0.6 and 1.0 V, respectively. Thus, applied voltage of 1.1 V is utilized to turn on the selected selector. Under such circumstance, read HRS state of RRAM fails because it changes to LRS state unintentionally after selector turns on, which is not tolerable during read process. Owing to large HRS resistance of RRAM relative to ON-resistance of selector, most of the applied voltage will be dropped on RRAM element after selector turns on. In addition, even if the variation is appropriate such as less than 0.2 V, larger power consumption accompanies the increasing applied voltage with similar power efficiency in Fig. 4c, d.

Through the simulation results of above read process, it testifies that variation of threshold voltage of selector may lead to mistakenly writing or larger power consumption under the same circumstance. So it is essential to assure the threshold voltage is in appropriate range to match the requirements of RRAM element.

4 Appropriate threshold voltage range

4.1 Minimum threshold voltage determination

To explore appropriate minimum threshold voltage of selectors, simulation of reset process is implemented. Applied voltage and power consumption are chosen as evaluation indices. First of all, applied voltage must be adequate to turn on the selected selector. Then, applied voltage must guarantee that voltage drop on RRAM satisfies the requirement for reset. Nevertheless, unselected selector may be wrongly turned on under worst scenario if V_{th_min} is too low. At last, the critical one with minimum applied voltage is defined as the minimum threshold voltage.

The simulation involves two parts: First of all, it is necessary to determine the minimum applied voltage to complete operation. Then, according to determined applied voltage, V_{th_min} is determined by seeking the minimum tolerable V_{th_min}. Concrete calculation is as following steps: (1) calculating the voltage distribution with all selectors under OFF-state to check if selected cell can be turned on; (2) calculating the voltage distribution to check if selected RRAM can be reset. If so, calculating the write margin and power consumption (considering the fact that changing state of RRAM takes time); (3) checking the validity of results according to Kirchhoff's current law, Ohm's law and current continuity; (4) repeating above calculation after altering the V_{th_min}. Relationship between minimum threshold voltage and varying OFF-/ON-resistance of selectors is analyzed within 1/2 and 1/3 bias scheme.

The simulation results are illustrated in Figs. 5 and 6. Figure 5 shows reset requirements as function of OFF-/ON-resistance of selectors under 1/2 bias scheme. Applied voltage positively correlates to ON-resistance while negatively correlates to OFF-resistance (Fig. 5a). Larger ON-resistance of selector leads to less voltage drop on RRAM element. Thus, larger voltage has to be applied to satisfy reset requirement. In the meantime, all selectors are in OFF-state on initial stage. Larger OFF-resistance suppresses leakage current more efficiently. In this way, voltage decaying in selected wordline will be less drastic. So more voltage will drop on selected cell and finish reset operation. That means larger OFF-resistance is better. However, curves of OFF-resistance with 5e7, 1e8 and 1e9 Ω take on similar trend and value as indicated in Fig. 5a. It demonstrates that OFF-resistance of 5e7 Ω is adequate to suppress leakage current with certain array size (1 Mb). Further increasing OFF-resistance will not promote the reset performance. Figure 5b shows the tendency of minimum threshold voltage. As mentioned above, limitation on minimum threshold voltage is to prevent unselected selector from switching unintentionally. Therefore, it is closely connected to applied voltage and presents similar tendency as applied voltage. To be specific, minimum threshold voltage increases with increasing ON-resistance and decreasing OFF-resistance of selectors.

Power consumption and write margin are the other two criterions for reset performance. As illustrated in Fig. 5c,

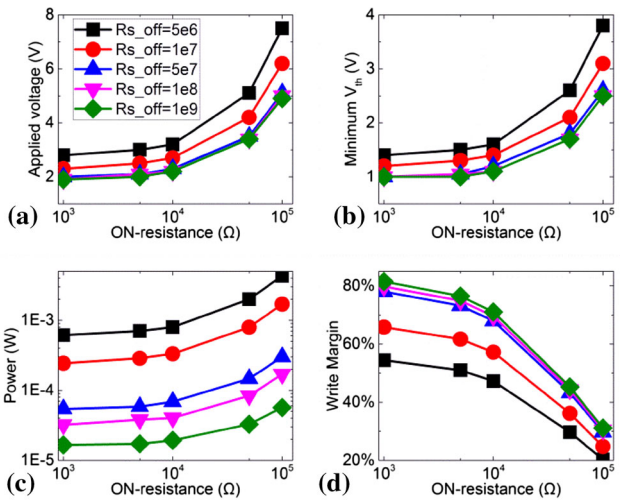

Fig. 5 Relationship between reset performance and OFF-/ON-resistance of selectors, including: **a** applied voltage, **b** minimum threshold voltage, **c** power consumption, and **d** write margin

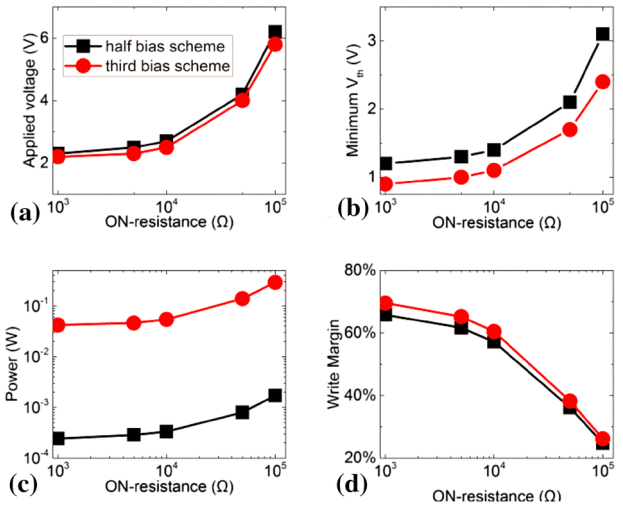

Fig. 6 Relationship between reset performance and OFF-state resistance of selectors, including: **a** applied voltage, **b** minimum threshold voltage, **c** power consumption, and **d** write margin

power greatly increases with ON-resistance increasing. Larger applied voltage inevitably consumes more power. Power decreases with increasing OFF-resistance all the while. The power is known to be driven by OFF-current of unselected cells rather than ON current of the selected one. Under ideal conditions, unselected selectors are all in OFF-state, so larger OFF-resistance will consumes less power. Relationship between write margin and resistance is reverse to the one between applied and resistance (Fig. 5d).

Figure 6 depicts the impact of bias scheme on reset requirements and performance. As an important circuit parameter, array bias scheme strongly affects the operation performance. Voltage on selected wordline and bitline is applied voltage and 0, respectively, under any bias schemes. The difference between these schemes is the voltage on unselected wordline and bitline. Under 1/2 bias scheme, voltage on unselected wordline and bitline is half applied voltage. Under 1/3 bias voltage, voltage on unselected wordline is one-third of applied voltage and voltage on unselected bitline is two-thirds of applied voltage.

OFF-resistance is set to 1e7 Ω. In Fig. 6a, applied voltage of 1/2 bias scheme is slightly larger than 1/3 bias scheme. The phenomenon/reason can be explained as follows. Maximum voltage on unselected cell along selected wordline and bitline is half applied voltage under 1/2 bias scheme. However, it is one-third applied voltage under 1/3 bias scheme. Thus, with same applied voltage, leakage current along selected wordline and bitline is larger under 1/2 bias scheme. Larger applied voltage is needed to compensate required voltage for switching RRAM. In a similar way, minimum threshold voltage under 1/2 bias scheme is larger than 1/3 bias scheme (Fig. 6b). As well-known, 1/3 bias scheme consumes much more power than 1/2 bias scheme under same conditions (Fig. 6c). Because voltage drops on all cells are 1/3 applied voltage under 1/3 bias scheme. This leads to larger leakage current than 1/2 bias scheme.

In summary, minimum threshold voltage increases with rising of ON-resistance and decreasing OFF-resistance. It causes the increasing of applied voltage, consumes more power and lowers write margin. So it is desirable to design threshold switching selectors with lower ON-resistance and higher OFF-resistance. In the meantime, minimum threshold voltage of 1/3 bias scheme is lower while consumes more power than 1/2 bias scheme.

4.2 Maximum threshold voltage determination

Simulation of read process can be utilized to evaluate the maximum threshold voltage. If threshold voltage of selected cell is too high, larger applied voltage is required. Thus, most voltage drops on RRAM after the selector turns on, which may lead to wrong writing. Simulation is divided to four parts: (1) calculating the voltage distribution with all selectors under OFF-state resistance to check if selected cell can be turned on. If selected selector is turned on, drop voltage on RRAM element is calculated immediately to check if it may induce wrong writing; (2) calculating the voltage distribution to define readout voltage and power consumption; (3) checking the results according to Kirchhoff's current law, Ohm's law and current continuity; (4) calculating read margin after simulating high-resistance and low-resistance state of RRAM.

Results are analyzed through two aspects. Firstly, maximum threshold voltage is ascertained by calculating the voltage allocation between selector and RRAM. Selector switches to ON-state after voltage drop on selector surpass the threshold voltage. At this moment, voltage drop on RRAM element is approximately $R_{HRS}/(R_{HRS} + R_{s\_on}) \times V_{th}$. It must be less than V_{dis} to avoid wrong writing. Thus the threshold voltage should be less than $(R_{HRS} + R_{s\_on})/R_{HRS} \times V_{dis}$, namely

$$V_{th\_max} < (R_{HRS} + R_{s\_on})/R_{HRS} \times V_{dis} \quad (1)$$

It indicates maximum threshold voltage is positively correlated to disturb voltage of RRAM element and ON-resistance of selector (Fig. 7). Larger disturb voltage means tolerable voltage drops on RRAM is higher. Meanwhile, larger ON-resistance means less voltage will drop on RRAM after selector turns on. Thus, larger voltage can be applied to turn on selector with higher threshold voltage.

The second one is discussing relationship between read performance and ON-resistance of selector as shown in Fig. 8. Disturb voltage of RRAM and OFF-resistance of selector is set to 1.0 V and 1e8 Ω, respectively. In Fig. 8a,

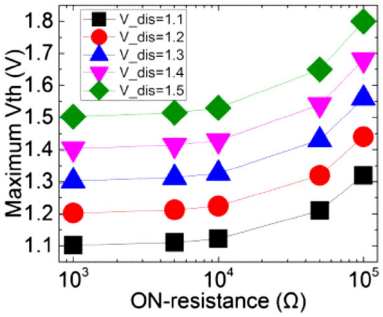

Fig. 7 Relationship between maximum threshold voltage and ON-resistance of selector and disturb voltage of RRAM

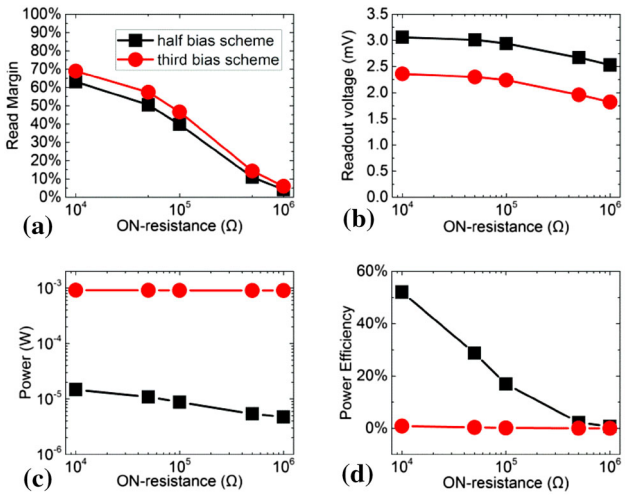

Fig. 8 Performance comparison between different bias scheme with variation-free scenario, including: **a** read margin, **b** readout HRS voltage, **c** power consumption, **d** power efficiency

read margin decreases with increasing ON-resistance of selectors within both bias schemes. It is reasonable because larger ON-resistance decreases disparity between high-resistance state and low-resistance state of RRAM. As a result, read margin is lowered. Figure 8b reflects that readout voltage of reading HRS decreases with increasing ON-resistance of selectors. Increasing ON-resistance leads to lower readout current corresponding to lower readout voltage. In addition, readout voltage of 1/2 bias scheme is a bit higher than that of 1/3 bias scheme and easier for accurately test. However, power consumption of 1/3 bias scheme is much higher than 1/2 bias scheme (Fig. 8c). Within both schemes, power consumption is unrelated to ON-resistance under 1/3 bias scheme and decreases with increasing ON-resistance under 1/2 bias scheme. Under 1/3 bias scheme, all selectors but selected one are in OFF-state and consume power. While under 1/2 bias scheme, only selectors along selected wordline or bitline consume power. Thus, ON-resistance of selected selector will induce more obvious effects. Moreover, power efficiency of 1/3 bias scheme is also unrelated to ON-resistance while it sharply decreases with increasing ON-resistance under 1/2 bias scheme (Fig. 8d).

In summary, larger ON-resistance of selectors permits higher maximum threshold voltage. But read margin and readout voltage will decrease with increasing ON-resistance.

5 Conclusion

Threshold voltage variation of threshold switching selectors severely affects array operation and performance. Controlling impacts in the appropriate range is proved to be essential before integrating selector and RRAM element. In this work, we analyze the possible impact of variation in threshold voltage of selectors. Meanwhile, we propose a method to determine minimum and maximum threshold voltage in crossbar array according to array performance of write and read operation. We have demonstrated that minimum threshold voltage is closely related to OFF- and ON-resistance of selectors while maximum threshold voltage is related to ON-resistance of selectors. Higher OFF-resistance and lower ON-resistance will assure that array can stand larger variation of threshold voltage without increasing the complexity and power of the operation. This method to attain the threshold voltage range can be used to assure the voltage compatibility between selector and RRAM.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant No. 61471377 and 61604177) and NUDT Science Support Program (No. JC-15-04-02).

References

1. G.W. Burr, R.S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, H. Hwang, Access devices for 3D crosspoint memory. J. Vac. Sci. Technol. B. **32**, 4 (2014)
2. B. Govoreanu, L. Zhang, M. Jurczak, Selectors for high density crosspoint memory arrays: design considerations, device implementations and some challenges ahead. International Conference on IC Design & Technology (ICICDT), IEEE (2015)
3. A. Chen, Nonlinearity and asymmetry for device selection in cross-bar memory arrays. IEEE. Trans. Electron. Dev. **62**, 9 (2015)
4. Y. Koo, K. Baek, H. Hwang, Te-based amorphous binary OTS device with excellent selector characteristics for x-point memory applications. IEEE Symposium on VLSI Technology, IEEE (2016)
5. H. Yang, M. Li, W. He, Y. Jiang, K. G. Lim, W. Song, Novel selector for high density non-volatile memory with ultra-low holding voltage and 10^7 on/off ratio. IEEE Symposium on VLSI Technology, IEEE (2015)
6. M. Lee, D. Lee, S. Cho, J. Hur, S. Lee, D.H. Seo, D. Kim, A plasma-treated chalcogenide switch device for stackable scalable 3D nanoscale memory. Nat. comm. **4**, 2629 (2013)

7. S. Kim, Y.-B. Kim, K.M. Kim, S.-J. Kim, S.R. Lee, M. Chang, Performance of threshold switching in chalcogenide glass for 3D stackable selector. IEEE Symposium on VLSI Technology, IEEE (2013)
8. M.-J. Lee, D. Lee, H. Kim, H.-S. Choi, J.-B. Park, H.G. Kim, Highly-scalable threshold switching select device based on chalcogenide glasses for 3D nanoscaled memory arrays. International Electron Devices Meeting (IEDM), IEEE (2012)
9. D. Kau, S. Tang, I.V. Karpov, R. Dodge, B. Klehn, J.A. Kalb, A stackable cross point Phase Change Memory. IEEE International Electron Devices Meeting (IEDM), IEEE (2009)
10. M. Anbarasu, M. Wimmer, G. Bruns, M. Salinga, M. Wuttig, Nanosecond threshold switching of $GeTe_6$ cells and their potential as selector devices. Appl. Phys. Lett. **100**, 143505 (2012)
11. W. Czubatyj, S.J. Hudgens, Invited paper: Thin-film Ovonic threshold switch: Its operation and application in modern integrated circuits. Electron. Mater. Lett. **8**, 2 (2012)
12. H. Yang, C.C. Tan, W. He, M. Li, Y. Jiang, Y. Yang, (Invited) Novel Selector and 3D RRAM Development for High Density Non-Volatile Memory. ECS. Trans. **69**, 5 (2015)
13. K. Zhang, B. Wang, F. Wang, Y. Han, X. Jian, H. Zhang, H.S.P. Wong, VO_2-Based Selection Device for Passive Resistive Random Access Memory Application. IEEE. Electron. Device. Lett. **37**, 8 (2016)
14. E. Cha, J. Woo, D. Lee, S. Lee, J. Song, Nanoscale ($\sim$10nm) 3D vertical ReRAM and NbO_2 threshold selector with TiN electrode. IEEE International Electron Devices Meet (IEDM), IEEE (2013)
15. J.A.J. Rupp, R. Waser, D.J. Wouters, Threshold Switching in Amorphous Cr-Doped Vanadium Oxide for New Crossbar Selector, IEEE 8th International Memory Workshop (IMW), IEEE (2016)
16. J. Park, E. Cha, I. Karpov, H. Hwang, Dynamics of electroforming and electrically driven insulator-metal transition in NbOx selector. Appl. Phys. Lett. **108**, 23 (2016)
17. S.H. Jo, T. Kumar, S. Narayanan, W.D. Lu, H. Nazarian, 3D-stackable Crossbar Resistive Memory based on Field Assisted Superlinear Threshold (FAST) Selector. IEEE International Electron Devices Meet (IEDM), IEEE (2014)
18. S.H. Jo, T. Kumar, S. Narayanan, H. Nazarian, Cross-Point Resistive RAM Based on Field-Assisted Superlinear Threshold Selector. IEEE. Trans. Electron. Devices. **62**, 11 (2015)
19. U.-B. Han, D. Lee, J.-S. Lee, Reliable current changes with selectivity ratio above 10^9 observed in lightly doped zinc oxide films. NPG. Asia. Mater. **9**, 2 (2017)
20. S. Cortese, M. Trapatseli, A. Khiat, T. Prodromakis, A TiO2-based volatile threshold switching selector device with 10^7 non linearity and sub 100 pA Off current. International IEEE Symposium on VLSI Technology, IEEE(2016)
21. J. Woo, D. Lee, E. Cha, S. Lee, S. Park, H. Hwang, Control of Cu Conductive Filament in Complementary Atom Switch for Cross-Point Selector Device Application. IEEE. Electron. Device. Lett. **35**, 60 (2014)
22. J. Song, A. Prakash, D. Lee, J. Woo, E. Cha, S. Lee, H. Hwang, Bidirectional threshold switching in engineered multilayer (Cu_2O/Ag:Cu_2O/Cu_2O) stack for cross-point selector application. Appl. Phys. Lett. **107**, 113504 (2015)
23. G. Du, C. Wang, H. Li, Q. Mao, Z. Ji, Bidirectional threshold switching characteristics in Ag/ZrO_2/Pt electrochemical metallization cells. AIP. Adv. **6**, 085316 (2016)
24. R. Midya, Z. Wang, J. Zhang, S.E. Savelev, C. Li, M. Rao et al., Anatomy of Ag/Hafnia-Based Selectors with 1010 Nonlinearity. Adv. Mater (2017). doi:10.1002/adma.201604457
25. C.H. Ho, H. Huang, M. Lee, C. Hsu, T. Lai, W. Chiu, M. Lee, T. Chou, I. Yang, M. Chen, C. Wu, K. Chiang, Y. Yao, C. Hu, F. Yang, Threshold Vacuum Switch (TVS) on 3D-stackable and $4F^2$ cross-point bipolar and unipolar resistive random access memory, IEEE International Electron Devices Meet (IEDM), IEEE (2012)
26. L. Zhang, S. Cosemans, D.J. Wouters, G. Groeseneken, M. Jurczak, B. Govoreanu, One-Selector One-Resistor Cross-Point Array With Threshold Switching Selector. IEEE. Trans. Electron. Devices. **62**, 10 (2015)
27. Q. Luo, X. Xu, H. Lv, T. Gong, S. Long, Q. Liu, Fully BEOL compatible TaOx-based selector with high uniformity and robust performance. IEEE International Electron Devices Meet (IEDM), IEEE (2016)
28. W. He, H. Yang, L. Song, K. Huang, R. Zhao, A Novel Operation Scheme Enabling Easy Integration of Selector and Memory. IEEE. Electron. Device. Lett. **38**, 2 (2016)
29. A. Chen, A Comprehensive Crossbar Array Model With Solutions for Line Resistance and Nonlinear Device Characteristics. IEEE. Trans. Electron. Devices. **60**, 4 (2013)
30. L. Zhang, S. Cosemans, D.J. Wouters, G. Groeseneken, Selector Design Considerations and Requirements for 1S1R RRAM Crossbar Array. IEEE International Memory Workshop (IMW), IEEE (2014)