Appl. Phys. A (2016) 122:988
DOI 10.1007/s00339-016-0530-9

Applied Physics A
Materials Science & Processing

Improved performance of nanoscale junctionless tunnel field-effect transistor based on gate engineering approach

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Received: 17 August 2016 / Accepted: 26 October 2016 / Published online: 2 November 2016

Abstract In this paper, a first qualitative study on the performance characteristics of dual-work function gate junctionless TFET (DWG-JLTFET) on the basis of energy band profile modulation is investigated. A dual-work function gate technique is used in a JLTFET in order to create a downward band bending on the source side similar to PNPN structure. Compared with the single-work function gate junctionless TFET (SWG-JLTFET), the numerical simulation results demonstrated that the DWG-JLTFET simultaneously optimizes the ON-state current, the OFF-state leakage current, and the threshold voltage and also improves average subthreshold slope. It is illustrated that if appropriate work functions are selected for the gate materials on the source side and the drain side, the JLTFET exhibits a considerably improved performance. Furthermore, the optimization design of the tunnel gate length (L_{Tun}) for the proposed DWG-JLTFET is studied. All the simulations are done in Silvaco TCAD for a channel length of 20 nm using the nonlocal band-to-band tunneling (BTBT) model.

1 Introduction

Over the past several decades, CMOS technology has been scaled down tremendously in order to increase integration density, operation speed, and energy proficiency. As we scale down the conventional metal–oxide–semiconductor FET (MOSFET) to sub-20 nm regimes, it encounters critical challenges and major obstacles in the fabrication of ultra-sharp doping gradient at the source and drain junction [1, 2]. Due to these fabrication difficulties, the performance characteristics of MOS devices have deteriorated by various short-channel effect (SCE), such as surface scattering, drain-induced barrier lowering (DIBL) and so on [3, 4]. The carrier injection in the source–channel junction of the MOSFET is dominated by thermionic emission mechanism over the potential barrier that is also increased because of this antagonistic scaling, and hence, the inverse subthreshold swing is limited to 60 mV/decade at room temperature [5]. Therefore, tunnel FET (TFET) is one of the alternative candidates to substitute CMOS technology which is most suitable for low-power applications [6–8]. Unlike MOSFET, TFET is not restricted by the thermionic emission constraint since the carrier injection mechanism from source to channel in the TFET is by band-to-band tunneling (BTBT) which could enable SS lower than kT/q limits of conventional MOSFETs [9–12]. Due to the channel, current is controlled by the quantum tunneling mechanism on the source side; TFETs are less prone to short-channel effects (such as V_T roll-off) unlike the conventional MOSFETs [13–15]. However, TFETs suffer from several drawbacks such as ambipolarity, low ON-state current (I_{ON}) as reported in the literature [16–18]. Besides, it is problematic that the SS values of experimentally proved silicon TFET are higher than expected values. In order to overcome these problems, different techniques such as low band gap materials, high-k gate insulators, strained silicon and dual-work function gate concept have been used [19–22]. Moreover, the current saturation mechanism in the output characteristics in a TFET is completely different from a conventional

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MOSFET [23]. As a result, TFETs often represent delayed saturation in the output characteristics. In addition, the dependence of the drain current on the drain voltage in a TFET is quite dissimilar from a conventional MOSFET [23]. Significant drain-induced barrier lowering (DIBL) effects are sometimes unveiled in a TFET, and this limitation can drastically reduce the efficiency of the device. Therefore, to treat TFETs for low-power CMOS applications, it is favorable that the overall performance characteristics of the TFET must be improved. Recently, junctionless tunnel FET (JLTFET) has represented tremendous potential as it blends advantages of JLTFET, which has high ON-current and TFET, which has low subthreshold slope [24–27]. A JLTFET is basically a uniformly doped junctionless transistor, which utilizes the work function engineering concept to behave analogously to any metallurgical junction. Due to the presence of uniform doping concentration, it has better scalability and low short-channel effects (SCEs). The JLTFET has been proposed as a solution for the various problems encountered in conventional CMOS technology such as scalability, low SS, and ON/OFF current ratio. JLTFETs also make a feature of high speed because of relatively large drive current and at the same time highly suppressed leakage current [28, 29]. Although the subthreshold slope of JLTFET is less than 60 mV/decade at room temperature, ON-state current is still inadequate to use in the present CMOS technology. In this paper, we present the application of dual-work function gate (DWG) in a double-gate junctionless TFET (JLTFET) by means of work function engineering concept. Using calibrated 2D numerical simulations, we prove that by engineering the work functions of the dual gates, it is possible to improve the ON-state current I_{ON}, the OFF-state current I_{OFF}, and the threshold voltage V_T and also optimize the subthreshold slope SS_{avg}. The dual-work function gate has been studied considerably and has been treated in not only ultra-scale MOSFETs [30–32], but also in power MOSFETs [33, 34]. However, the calibration of dual-work function gate concept in a JLTFET to enhance its ON-current and the subthreshold slope has not been reported.

The rest of this paper is organized as follows: Sect. 2 elaborates the physical structure of DWG-JLTFET and the simulation model used in this study. Section 3 represents simulation results for a DWG-JLTFET and demonstrates the privilege of using a DWG. In this section, the proposed dual-work function gate JLTFET (DWG-JLTFET) is compared with single-work function gate JLTFET (SWG-JLTFET) which taking scandium (Sc) with the work function of 4.0 eV and tungsten (W) with the work function of 4.4 eV as the gate material with a gate length of 20 nm. Also, in the proposed structure a local conduction band minima, E_c due to the low work function of the tunnel gate near the source end are observed, whose effect will be investigated in this section. The analysis of the DWG-JLTFET has been accomplished for $V_{DD} = 1.0$ V. Finally, Sect. 4 draws important conclusions out of this study.

2 Device structure and simulation

The sketch of the proposed dual-work function double-gate junctionless tunnel FET (DWG-JLTFET) and its cross section along the channel are shown in Fig. 1. The parameters for the DWG-JLTFET used in our simulation are [24]: source/drain/channel doping $= 1 \times 10^{19}/\text{cm}^3$, silicon film thickness (t_{Si}) = 5 nm, gate oxide thickness (t_{ox}) = 2 nm, and isolation layer between SG and TG (L_{sp}) = 5 nm, source/drain extension length ($L_{S/D}$) = 20 nm, channel length (L_G) = 20 nm, tunnel gate length (L_{Tun}) = 6 nm, and auxiliary gate length (L_{Aux}) = 14 nm. The double-gate technology is utilized to provide better electrostatic controllability of gate over the channel. In this feature, both top and bottom gated in the channel region are comprised of materials with two different work functions. We refer to the gate closer to the

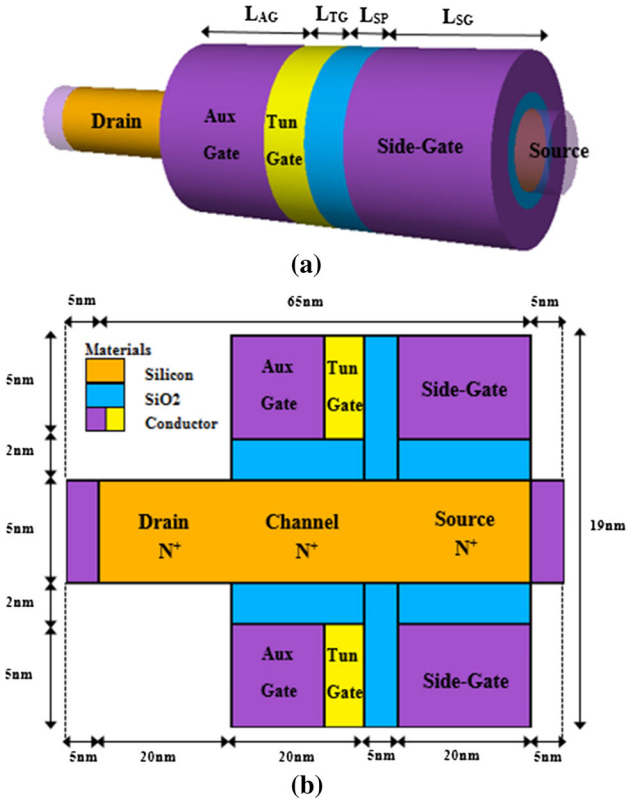


Fig. 1 **a** 3D schematic view and **b** cross-sectional view of the JLTFET with a dual-work function gate (L_{Tun}, L_{Aux}). Silicon film thickness $t_{si} = 5$ nm, gate dielectric thickness $t_{ox} = 2$ nm, gate length (L_G) = 20 nm, tunnel gate length (L_{Tun}) = 6 nm, and auxiliary gate length (L_{Aux}) = 14 nm

source region as the tunnel gate (TG) which controls the tunneling generation rate at the source–channel junction. The one closer to the drain as the auxiliary gate (AG) and its work function variation mainly controls the OFF-current. For the proposed device characterization, we have taken the tunnel gate and auxiliary gate metals with the work function of 4.0 and 4.4 eV, respectively. The length of the tunnel gate is $L_{Tun} = 6$ nm and that of the auxiliary gate is $L_{Aux} = 14$ nm. Moreover, we have used a source metal electrode platinum (Pt) with a work function of 5.93 eV to make the layer beneath side gate (SG) p + source region. This is while the (TG + AG) in the channel region is used to modulate the effective tunneling barrier on the source and drain side. The integration of SG above the source region and (TG + AG) above the channel region together in the fabrication process, whose work functions are different, could be done by using the techniques as reported in Refs. [35–37]. The formation of the isolation layer with thickness of 5 nm of SiO_2 between SG and TG could be done either by using a sputtering process or other modern gate dielectric fabrication process such as atomic layer deposition (ALD) after formation of the field oxide by wet oxidation.

The technology computer aided design (TCAD) simulation has been evaluated by using 2D-ATLAS device simulator [35]. We use nonlocal band-to-band tunneling (BTBT) model [36] to account for the spatial profile of the energy bands and also to account for the spatial separation of electrons generated in the conduction band from the holes generated in the valence band. We comprise the effect of Fermi–Dirac statistics in the calculation of the intrinsic carrier concentration required in the expressions for Shockley–Read–Hall (SRH) recombination. To capture the effect of temperature-dependent mobility, a concentration-dependent mobility (CONMOB) model and parallel and perpendicular electric field-dependent mobility (FLDMOB) model are used. Due to the presence of high doping concentrations, band gap narrowing (BGN) and auger recombination (AUGER) models are included in the simulations. Moreover, to assume high impurity atom in the channel and also to taking into account an interface trap (or defect), the Shockley–Read–Hall (SRH) recombination mode is enabled [37]. To include quantum confinement effects at the Si/SiO_2 interface due to heavy doping concentration and thin oxide thickness, Quantum Confinement (HANSCHQM) model given by Hansch [38] is considered. Trap-assisted tunneling (SCHENK.TUNN) model given by Schenk [39] to account for interface trap effect on electron band-to-band tunneling in TFETs is enabled. The simulation model used in this paper, including tunneling model, has also been used in our previous works [26, 27]. Moreover, for validation of the device, conventional JLTFET reported by Ghosh and Akram [24] has been implemented and simulated. The simulated I_D–V_{GS} characteristics of this implemented device are calibrated with reported results as shown in Fig. 2. Then, the calibrated conventional JLTFET is scaled to work function and gate-to-source voltage values that are considered in this work.

3 Results and discussion

At first, the impact of the work function of the auxiliary gate (Φ_{Aux}) on the OFF-state leakage current, I_{OFF} in a DWG-JLTFET is analyzed. The analysis is accomplished in the same way as it is done in DWG-DGTFET [22]. Figure 3a, b illustrates the variation in the energy band diagram profile of the device as Φ_{Aux} is increased while keeping Φ_{Tun} fixed at 4.0 eV. In the OFF-state (Fig. 3a), as Φ_{Aux} is increased, the tunneling barrier width on the source side increases which results in a significant suppression of the tunneling probability of electrons in the OFF-state. This behavior originates from the smaller band overlap on the source side of the proposed device. The OFF-state current is comprised of BTBT current plus reverse leakage current, as Φ_{Aux} increases up to 4.4 eV; the current flow will be governed by reverse leakage current phenomena since there is no tunneling path. However, with further increase in Φ_{Aux} (>4.4 eV), band overlap starts to appear on the drain side, and if the tunneling barrier width on the drain side becomes narrow enough (as in the case of $\Phi_{Aux} = 4.8$ eV), tunneling can happen in the OFF-state. In the ON-state (Fig. 3b), an increase in Φ_{Aux} does not bring any considerable change in the energy band diagram profile. In this case, the tunnel barrier width modulation between source and channel is negligible and as a result, the electrons tunneling probability is not significantly

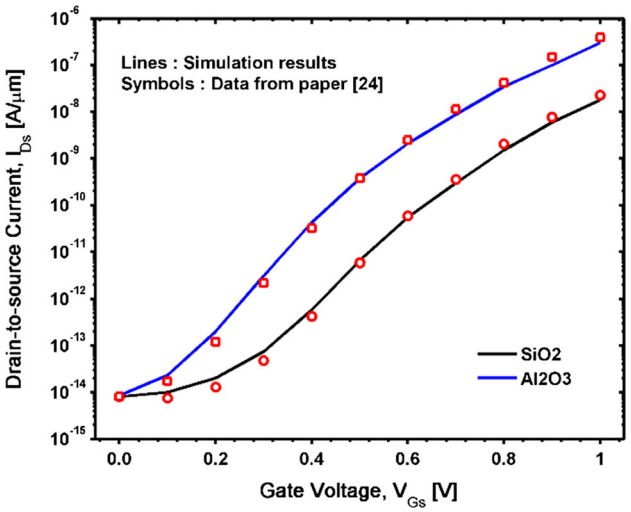


Fig. 2 Calibration for simulation results with the data extracted from [24] under the same conditions

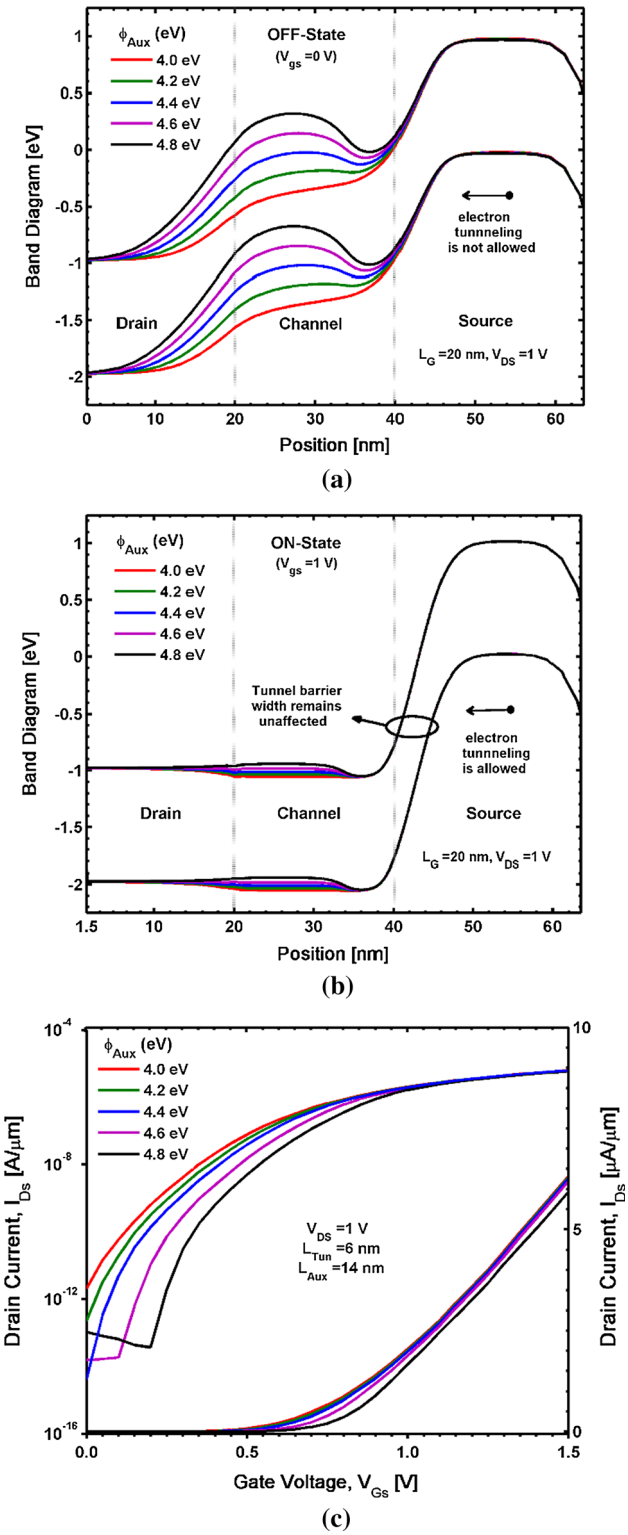


Fig. 3 For DWG-JLTFET with $\Phi_{Tun} = 4.0$ eV, $L_{Tun} = 6$ nm and $L_{Aux} = 14$ nm **a** OFF-state band diagram profile along *x*-direction ($V_{GS} = 0$ V, $V_{DS} = 1$ V). **b** ON-state band diagram profile along *x*-direction ($V_{GS} = 1.5$ V, $V_{DS} = 1$ V). **c** Transfer characteristics of DWG-JLTFET with variation of auxiliary gate work function at $V_{DS} = 1$ V

affected. The transfer characteristics of the DWG-JLTFET while Φ_{Aux} is increased from 4.0 to 4.8 eV, are shown in Fig. 3c. The OFF-state current of the proposed structure, which is defined as the drain-to-source current I_{DS} at $V_{GS} = 0$ V and $V_{DS} = 1$ V is considerably affected and exhibits more than two orders of magnitude improvement when $\Phi_{Aux} \geq 4.4$ eV. However, the ambipolar current which is the tunneling of holes from conduction band of drain-to-valence band of channel begins to flow due to the decrement in tunneling width at the drain–channel interface and further band overlap on the drain side when $\Phi_{Aux} \geq 4.8$ eV; hence, the drain current starts increasing by the tunneling of holes rather than tunneling of electrons at the opposite end (source–channel interface) in the negative gate voltages. The ON-state current of DWG-JLTFET which is defined as the drain-to-source current I_{DS} at $V_{GS} = 1$ V and $V_{DS} = 1$ V, is not diminished seriously. In other words, the flow of minority charge carriers from valence band of source region to the conduction band of channel region does not change considerably.

Afterward, the impact of the tunnel gate work function (Φ_{Tun}) on the characteristics (I_{ON}) of a DWG-JLTFET is examined. Figure 4a, b illustrates the variation in the energy band diagram profile of the device as Φ_{Tun} is decreased while keeping Φ_{Aux} fixed at 4.4 eV. In the OFF-state (Fig. 4a), a local conduction band minima, E_c is observed in the energy band diagram profile on the source side when Φ_{Tun} is reduced to 4.0 eV. However, there is no significant band overlap on the source side occurs because of conduction band minima (E_c). Hence, in the OFF-state, we obtained a quite low BTBT rate which gives as expected low I_{OFF}. But, in the ON-state (Fig. 4b), due to this energy band diagram modulation caused by the reduction in Φ_{Tun}, the tunneling barrier width of the DWG-JLTFET considerably becomes small. So, there is a high probability of tunneling of electrons from the occupied states of the valence band of the source side into the unoccupied states of the conduction band of the channel. Consequently, it will result in an improved ON-current of the proposed structure. The electrical characteristics of the DWG-JLTFET are studied with the reduction of Φ_{Tun} from 4.8 to 4.0 eV keeping Φ_{Aux} fixed at 4.4 eV as shown in Fig. 4c. As predicted, the I_{ON} enhances by about one order of magnitude. The I_{OFF} is relatively at the same value for all the work function values of Φ_{Tun}. The threshold (V_T) of the DWG-JLTFET which is defined as the gate-to-source voltage V_{GS} where the drain current is 10^{-7} A/μm [39], is appropriately improved and reduced to 0.48 V at $\Phi_{Tun} = 4.0$ V.

The abovementioned analysis demonstrates using a dual-work function gate concept (TG, AG) in the DWG-JLTFET provides additional capability to control different section of the transfer characteristics results in improving

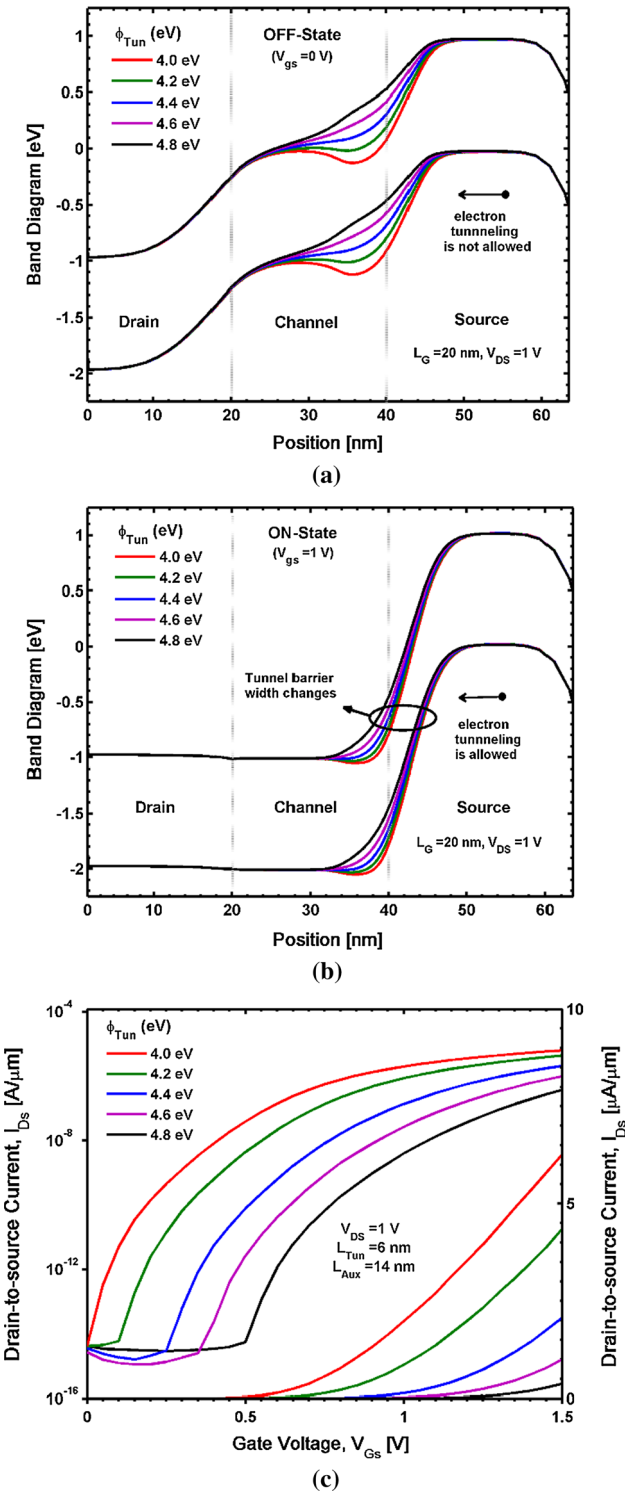


Fig. 4 For DWG-JLTFET with $\Phi_{Aux} = 4.4$ eV, $L_{Tun} = 6$ nm, and $L_{Aux} = 14$ nm **a** OFF-state band diagram profile along *x*-direction ($V_{GS} = 0$ V, $V_{DS} = 1$ V). **b** ON-state band diagram profile along *x*-direction ($V_{GS} = 1.5$ V, $V_{DS} = 1$ V). **c** Transfer characteristics of DWG-JLTFET with variation of tunnel gate work function at $V_{DS} = 1$ V

TFET performance operation. It can be seen from Fig. 4c, when we decrease Φ_{Tun} to 4.0 eV, the I_{ON} increases, and V_T decreases. Since the conventional SWG-JLTFET suffers from a relatively low I_{ON} and high V_T, it is favorable to determine the device parameter to obtain a maximum value of I_{ON} and a minimum value of V_T. Also, from the Fig. 3c it is observed that when we increase Φ_{Aux}, the I_{OFF} decreases, but with further increase $\Phi_{Aux} > 4.4$ eV the ambipolar conduction significantly increases leading to lower I_{ON}/I_{OFF}. Therefore, the best possible values for both the tunnel and auxiliary gate are 4.0 and 4.4 eV, respectively. There are several metals nominates that can be engineered to obtain the desirable Φ_{Tun} (4.0 eV) (e.g., Mo, Ni–Ti, and Sc) and Φ_{Aux} (4.4 eV) (e.g., W, Ta, and Mo) [40–45].

The I_D–V_{GS} curve of DWG-JLTFET and comparable SWG-JLTFET with different work functions at the drain-to-source voltage $V_{DS} = 1$ V are shown in Fig. 5. This implicates the good electrostatic integrity of DWG-JLTFET over SWG-JLTFET. It is clear that using dual-work function over SWG-JLTFET. It is clear that using dual-work function gate (DWG) technique, we can provide an enhanced ON-state current as well as improved I_{OFF}, which cannot be achieved by using SWG-JLTFET. Therefore, the I_{ON}/I_{OFF} ratio increases to 1.52×10^9 from 0.58×10^8, which is the best possible value of the SWG-JLTFET by adjusting the gate work function at $\Phi = 4.4$ eV in the simulation. It is observed that at low gate voltage, the OFF-state current of DWG-JLTFET is followed by auxiliary gate ($\Phi_{Aux} = 4.4$ eV) where a low I_{OFF} is achieved and the ON-state current of DWG structure is followed by tunnel gate ($\Phi_{Tun} = 4.0$ eV) at high gate voltage, which gives rise to high value of I_{ON}. Indeed,

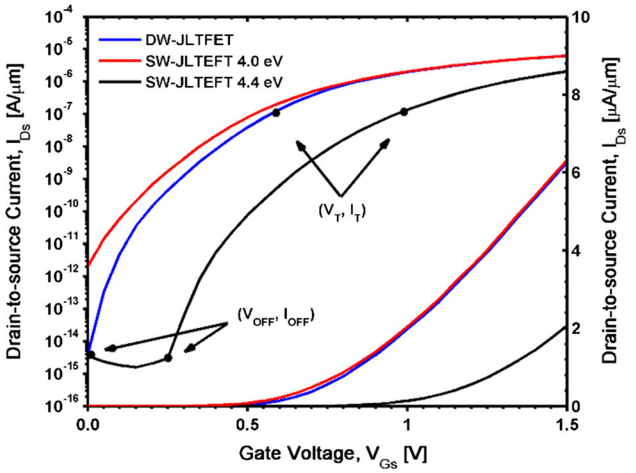


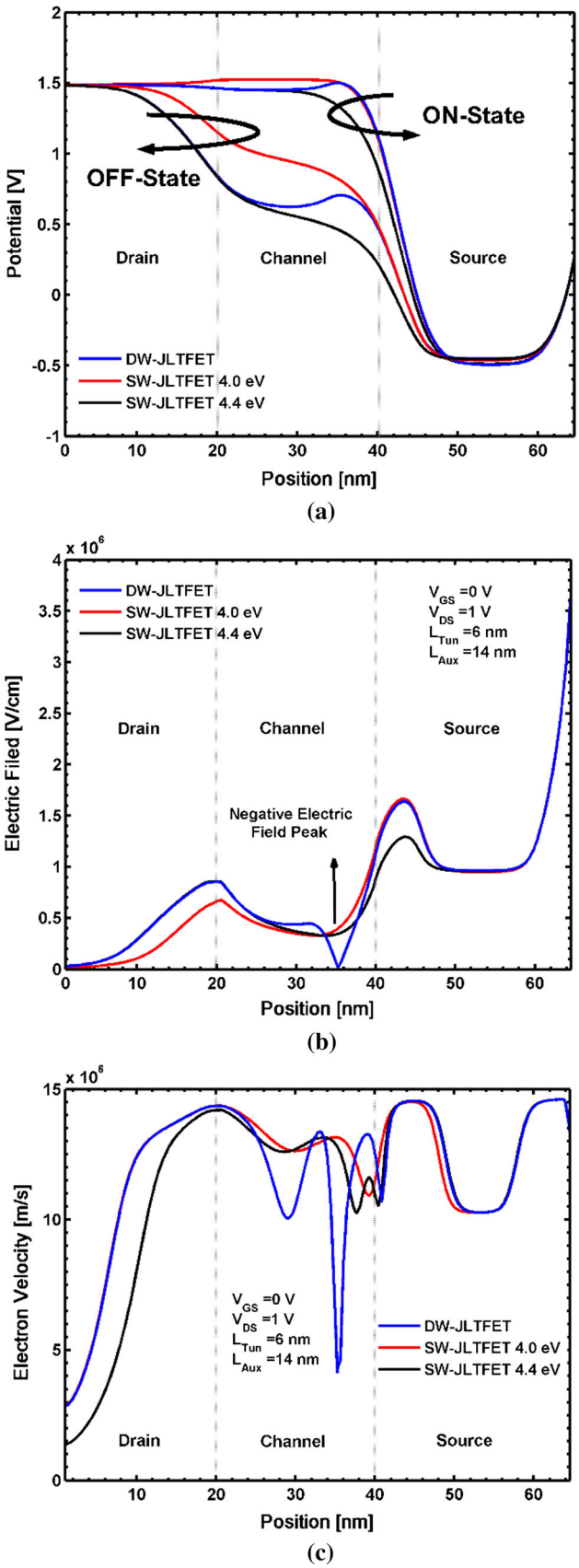
Fig. 5 Transfer characteristics of DWG-JLTFET and corresponding SWG-JLTFET with different work functions

this treatment implicates that the OFF-state current of the DWG-JLTFET is controlled by the auxiliary gate at low V_{GS} and the ON-state current is controlled by tunnel gate at high gate voltage. As a result, the DWG-JLTFET has simultaneously high I_{ON} and low I_{OFF} which is not achievable by use of an SWG-JLTFET. Furthermore, the subthreshold slope SS is lower than that of the SWG-JLTFET, not only for the point SS_p extracted from taking off point (V_{OFF}, I_{OFF}) shown in Fig. 5, but also for the average SS_{avg} which is defined as:

$$SS_{avg} = \frac{V_T - V_{OFF}}{\log(I_T) - \log(I_{OFF})}$$

where V_T is the threshold voltage extracted at the drain-to-source current $I_{DS} = 10^{-7}$ A/μm [39]. The SS_p significantly improves from 37.62 mV/dec in the SWG-JLTFET to 24.21 mV/dec in the DWG-JLTFET and for the SS_{svg} from 64.8 to 52.12 mV/dec at given $V_{DS} = 1$ V. It is noteworthy that the manipulation of gate work function in the conventional SWG-JLTFET only shifts the transfer characteristics parallel to the x-axis which does not affect the SS.

The surface potential, lateral electric field, and electron velocity distribution along the channel in the DWG-JLTFET and the corresponding SWG-JLTFET are further investigated in Fig. 6. Contradictory to conventional MOSFET which has a steep potential rising and an electric field peak in the drain side [35, 36], the TFET keeps them on the source side where the quantum band-to-band tunneling (BTBT) occurs. As shown in Fig. 6a, an opposite potential trend emerges at the interface of the two gates of the proposed DWG-JLTFET. This phenomenon originates from a higher work function is used for the auxiliary gate ($\Phi_{Aux} = 4.4$ eV) (Fig. 7). Due to the aforementioned potential step, a negative electric field appears at the transition of two gates as shown in Fig. 6b. This part of electric field decreases the average velocity of electrons which establish in the channel region by means of indirect BTBT in the OFF-state (Fig. 6c). As a consequence, reasonable work function leads to next, we analyze the impact of tunnel gate length (L_{Tun}) to reduce the opportunity of OFF-state tunneling on the drain side, and consequently, the setting helps to suppress the OFF-state leakage current I_{OFF} variation on the electrical characteristic of the proposed DWG-JLTFET and we also find an optimum value of the of tunnel gate length (L_{Tun}) for the given $V_{DS} = 1$ V. Figure 7 illustrates the change in the transfer characteristics curve of the proposed device as L_{Tun} is increased. The tunnel gate length is varied from 4 to 14 nm, while keeping the total gate length $L_G = L_{Tun} + L_{Aux}$ unchanged. It can be concluded from the figure, as the length of the L_{Tun} increases, the local E_c minima on the source side become wider which makes the electrons to tunnels from the source to the channel without the applied gate bias. Thus, the



◀**Fig. 6** Distribution of **a** channel surface potential, **b** channel lateral electric field, and **c** channel average electron velocity. The proposed DWG-JLTFET lengths are $L_{Tun} = 6$ nm and $L_{Aux} = 14$ nm

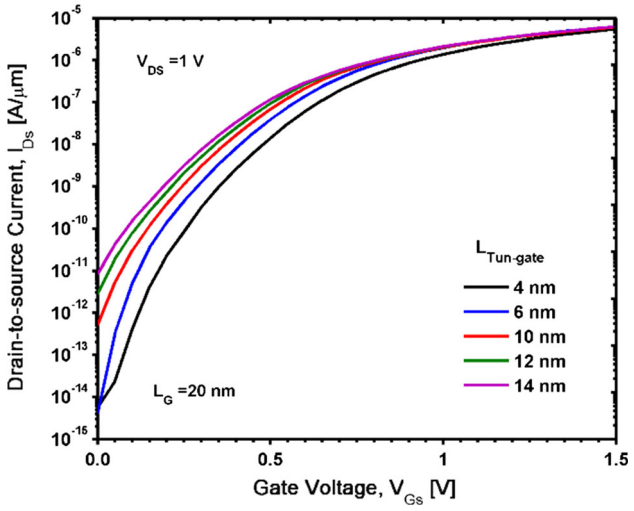


Fig. 7 Transfer characteristics of the DWG-JLTFET for different values of L_{Tun}

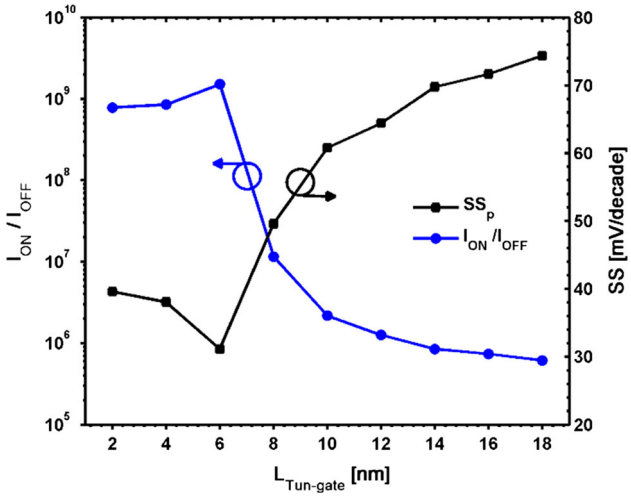


Fig. 8 ON/OFF current ratio and point subthreshold slope (SS_p) as a function of the tunnel gate length (L_{Tun}) for the DWG-JLTFET

region of the channel beneath the L_{Tun} operates as a virtual source of electrons. So, this region under the L_{Tun} creates a downward band bending similar to the PNPN structure [46, 47], which increases the electric field at the tunnel junction and reduces the source to channel tunnel path. As a result, the L_{Tun} gate loses it controllability over the tunneling barrier width at low gate voltage, and for such a PNPN-like structure, the source–channel tunneling junction is not gate-controlled. In this situ, the L_{Aux} takes control responsibility of transistor operation. Therefore, the tunneling barrier width modulation has saturated, and the transistor actually operates by means of lowering the barrier beneath the L_{Aux} gate which is now analogous to MOSFET operation. As a result, this leads to a degradation of the subthreshold slope SS and an enhancement in leakage OFF-current I_{OFF} in the device as L_{Tun} length increases.

Figure 8 shows the dependence of the ON/OFF current ratio (I_{ON}/I_{OFF}) and the point subthreshold slope (SS_p) of the proposed DWG-JLTFET with a variation of tunnel gate length (L_{Tun}). When the L_{Tun} starts to increase, as we explained in the previous section, the values of I_{ON}/I_{OFF} and SS_p are degraded at room temperature of 300 K. However, for a range of L_{Tun} values (2–6 nm), the DWG-JLTFET represents both a high ON/OFF current ratio and a low SS_p exhibiting that the process-induced variations in L_{Tun} will not affect its performance. The aforementioned analysis shows that the length of the tunnel gate can be adjusted for better I_{ON}/I_{OFF} and SS_p. Since there is a low I_{ON}/I_{OFF} ratio when L_{Tun} higher than 6 nm, we have chosen $L_{Tun} \leq 6$ nm. Finally, we have taken a tunnel gate length of 6 nm for our device simulation, which gives the optimized value of I_{ON}/I_{OFF} ratio and SS_p. These simulation results reveal the fact that the utilization of a dual-work function gate to form the PNPN-like structure makes the DWG-JLTFET more attractive candidate compared to an SWG-JLTFET.

4 Conclusion

A comparative study of device physics of the DWG-JLTFET over the conventional SWG-JLTFET is explored through extensive 2D numerical simulations. These results demonstrate that the technique of using DWG can be applied to obtain superior characteristics, e.g., I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio improvement and suppression of subthreshold slope SS, compared to the corresponding single-work function JLTFET (SWG-JLTFET). Thus, DWG-JLTFET has potential advantages in the low operation power (LOP) application. Moreover, it is observed that the length of tunnel gate considerably affects the device characteristics by changing channel controllability, as well as affect the tunneling probability. As a general guideline, $L_{Tun} = 6$ nm and $L_{Aux} = 14$ nm at $L_G = 20$ nm and the corresponding work function values, $\Phi_{Tun} = 4.0$ eV and $\Phi_{Tun} = 4.4$ eV are proposed for the DWG-JLTFET performance optimization.

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