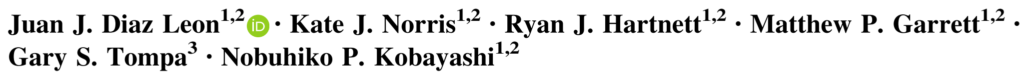
Appl. Phys. A (2016) 122:741
DOI 10.1007/s00339-016-0260-z

Applied Physics A
Materials Science & Processing

CrossMark

Nonlinear current–voltage characteristics based on semiconductor nanowire networks enable a new concept in thermoelectric device optimization



Juan J. Diaz Leon[1,2] · Kate J. Norris[1,2] · Ryan J. Hartnett[1,2] · Matthew P. Garrett[1,2] · Gary S. Tompa[3] · Nobuhiko P. Kobayashi[1,2]

Received: 9 May 2016 / Accepted: 5 July 2016 / Published online: 16 July 2016
© Springer-Verlag Berlin Heidelberg 2016

Abstract Thermoelectric (TE) devices that produce electric power from heat are driven by a temperature gradient ($\Delta T = T_{hot} - T_{cold}$, T_{hot}: hot side temperature, T_{cold}: cold side temperature) with respect to the average temperature (T). While the resistance of TE devices changes as ΔT and/or T change, the current–voltage (*I*–*V*) characteristics have consistently been shown to remain linear, which clips generated electric power (P_{gen}) within the given open-circuit voltage (V_{OC}) and short-circuit current (I_{SC}). This P_{gen} clipping is altered when an appropriate nonlinearity is introduced to the *I*–*V* characteristics—increasing P_{gen}. By analogy, photovoltaic cells with a large fill factor exhibit nonlinear *I*–*V* characteristics. In this paper, the concept of a unique TE device with nonlinear *I*–*V* characteristics is proposed and experimentally demonstrated. A single TE device with nonlinear *I*–*V* characteristics is fabricated by combining indium phosphide (InP) and silicon (Si) semiconductor nanowire networks. These TE devices show P_{gen} that is more than 25 times larger than those of comparable devices with linear *I*–*V* characteristics. The plausible causes of the nonlinear *I*–*V* characteristics are discussed. The demonstrated concept suggests that there exists a new pathway to increase P_{gen} of TE devices made of semiconductors.

Juan J. Diaz Leon and Kate J. Norris have contributed equally to this work.

✉ Juan J. Diaz Leon
jdiazleo@ucsc.edu

[1] Baskin School of Engineering, University of California Santa Cruz, Santa Cruz, CA 95064, USA

[2] Nanostructured Energy Conversion Technology and Research (NECTAR), Advanced Studies Laboratories, University of California Santa Cruz – NASA Ames Research Center, Moffett Field, CA 94035, USA

[3] Structured Materials Industries, Inc., Piscataway, NJ, USA

1 Introduction

Thermoelectric (TE) power generation is an attractive method for generating electrical power from various heat sources [1–3]. In the past, progress in this field has resulted from focusing on TE materials engineering aspects, rather than TE device designs [4–6]. Various TE materials are routinely evaluated by the dimensionless figure of merit ($ZT = S^2\sigma T/\kappa$), where T is an operating average temperature, S is the Seebeck coefficient ($S = -\Delta V/\Delta T$, with ΔV and ΔT being the total voltage and temperature differences, respectively, across the gradient axis), σ is the electrical conductivity, and κ is the thermal conductivity of the material under study. For instance, a range of emerging nanomaterials expected to increase ZT by increasing S and decreasing κ have propelled the development of exotic TE materials controlled at the nanometer scale [7, 8]. Advances have been made with superlattices [9–11], thin films [12–15], organic semiconductors [16, 17], densely packed nanopowders [18], and nanowires [19–22]. Nanowires (NWs) have stood out as an especially desirable option due to their reduced thermal conductivity while maintaining electrical conductivity and the Seebeck coefficient [23–26]. The thermal conductivity—and hence ZT—of a single nanowire is heavily dependent on its physical dimensions [26]. The collective properties of NWs forming a network, rather than myriad discrete NWs, are further beneficial in TE applications, as heat must travel over a much longer distance in a nanowire network than in a single nanowire [27]. Doping at an appropriate level is key to semiconductor thermoelectrics,

as it allows σ to be enhanced in the extrinsic region, yet going "deep" into the valence band (for p doping) decreases S [28, 29]. ZT is often used to scale the Carnot efficiency in obtaining power conversion efficiency. However, such ZT-deduced power conversion efficiency does not always provide a practical way of optimizing device power performance. In lies the direction of the current work how to supplement ZT in addressing power generation from TE devices.

In this paper, we present a new concept: nonlinearity. We suggest that rather than relying on performance improvements, electrical power generated from TE devices at various temperatures can benefit from the concept of nonlinear current–voltage characteristics. Traditionally, TE materials are appropriately doped to ensure highly efficient ohmic contacts in a TE device [30]. As a result, given a conventional TE device architecture, the current–voltage characteristic is linear. In contrast, the device presented in this paper takes advantage of nonlinearity explicitly introduced in current–voltage characteristics to increase electrical power generation. It is conceivable that this new concept in TE, if designed and implemented properly, adds another parameter to utilize in optimizing TE devices—in the same way that nonlinear current–voltage characteristics have been known to be one of the key performance parameters in photovoltaics [31, 32]. Nonlinearity in current–voltage characteristics of TE devices can be established, for instance, through the introduction of a rectifying layer, interface, or inducing space-charge region without substantially destructing overall charge transport [33, 34]. The new device architecture presented herein is made possible by our unique processes of growing single-crystal semiconductor NW networks on non-single-crystal copper substrates [35]. The metal/semiconductor nanowire/metal building blocks (i.e., TE cells, which are devoid of a thick semiconductor substrate) can be successively stacked to fabricate multistage TE devices, which can be physically much thicker than single-stage TE devices [21]. In this demonstration, Si and InP, two representative materials available in our laboratory, were chosen for the NW materials. Silicon (Si) NWs have been thoroughly produced and studied for TE [20, 21, 36]. Indium phosphide (InP) NWs have been the object of study for optical and TE applications in our laboratory [37, 38]. The current work shows how Si and InP can be combined to achieve nonlinearity and increase overall TE efficiency.

2 Experimental

First, small (2 cm^2 in area) coupons were cut from a sheet of flexible copper (Cu) foil that was $\sim$50 μm thick. The Cu coupons were further prepared with acetic acid, rinsed with DI water, and air dried. In complete TE devices, the Cu coupon served as a substrate as well as a bottom electrode. InP and Si NW networks were grown on the prepared Cu coupons in two different deposition systems. As a pre-growth preparation step on the prepared Cu coupons, two distinctive processes were developed for InP and Si NW growth as follows. For the growth of InP NWs, electron beam evaporation was used to deposit a 30 nm Si layer directly on the prepared Cu coupons. Subsequently, the Cu coupons were coated with colloidal gold particles with diameters approximately 10–50 nm and allowed to dry in air. A two-step metal organic chemical vapor deposition (MOCVD) growth process, specifically developed for the prepared Cu coupons, was used to grow the InP NW network [35, 39]. The two-step MOCVD growth, consisting of a NW growth mode (step 1) followed by a film growth mode (step 2), formed a continuous layer on the tips of the NWs. This ensured that a good ohmic contact (i.e., a top electrode) was formed on the NWs without electrically shorting the top electrode and the Cu coupon (i.e., the bottom electrode). In the two-step MOCVD growth for InP NW networks, growth conditions were as follows: in step 1, growth pressure: 150 Torr, molar V/III ratio: 3.8, growth time: 45 min, and growth temperature: 560 °C, and in step 2, growth pressure: 150 Torr, molar V/III ratio: 1.5, growth time: 55 min, and growth temperature: 500 °C. The precursors for the two-step MOCVD growth of InP NW network were ditertiary butylphosphine (DTBP) and trimethylindium (TMIn). In the MOCVD growth, the InP NW network was exposed solely to indium during the final step of the growth to increase the surface area on which the PECVD Si top layer was deposited. Following the InP NW network growth, an n-type (Sb-doped) Si layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the nearly continuous surface made of InP NWs that resulted from the two-step MOCVD growth. The Sb-doped Si PECVD layer deposition was conducted at 500 °C, 0.5 Torr for 15 min with 180–250 kHz plasma generated by a 12.6 kW power source. Precursors/standard cubic centimeters per minute (sccm) flow for the Sb-doped Si layer were disilane/10 sccm and triethylantimony/0.148 sccm (introduced as an n-type dopant) in a hydrogen/344 sccm carrier gas environment. This Si layer, referred to as "PECVD Si" provided a doped semiconductor surface for a top electrode and prevented shorting when a top electrode was formed. The fabricated TE device, referred to as "InP TE device," made of Cu bottom electrode/evaporated Si/InP NW network/PECVD Si/Cu top electrode, is schematically shown in Fig. 1a.

For the Si NW network growth, carbon deposition was performed on the prepared Cu coupon. The process of depositing a carbon layer on Cu foils and the role graphene plays within the context of growing Si nanowires have

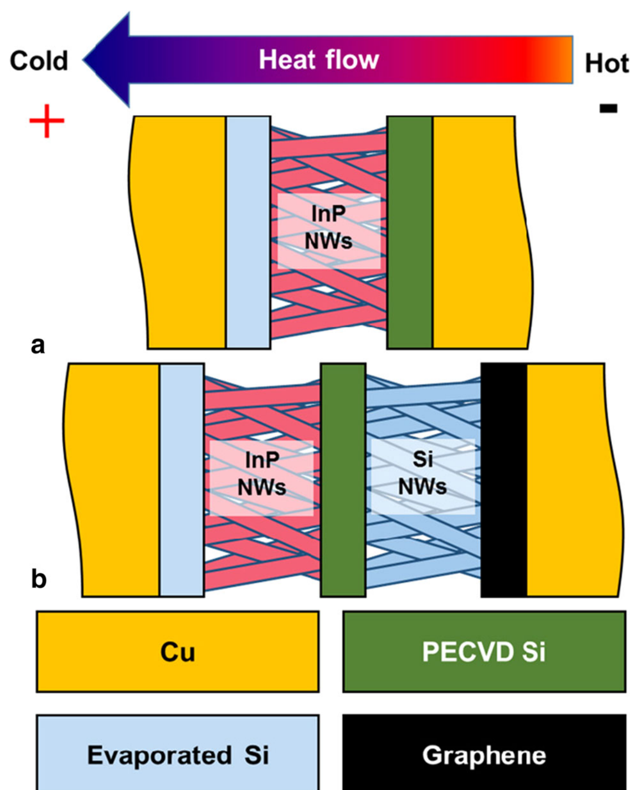


Fig. 1 Schematic of two TE devices: **a** an InP TE device composed of an InP NW network and a PECVD Si layer, and **b** an InP/Si TE device composed of InP and Si NW networks and a PECVD Si layer

been described and studied using Raman spectroscopy [35]. The study showed that growing Si on Cu without a graphene layer results in a polycrystalline Si layer rather than NWs. After the graphene deposition, the Cu foils were further coated with colloidal gold prepared from a 1 mM hydrogen tetrachloroaurate and 1 % trisodium citrate solution. Plasma-enhanced chemical vapor deposition (PECVD) was utilized to grow silicon NW networks at a growth temperature of 500 °C. The disilane flow rate was 10 sccm with a reactor pressure of 0.3 Torr and a growth time of 15 min, resulting in unintentionally doped (UID) Si NWs forming a 3D network. After the growth of Si NW network, the reaction chamber was evacuated and the sample was cooled to 50 °C in argon. The resulted TE device based on Si NW networks is referred to as "Si TE device". The fabricated InP and Si TE devices were integrated in a single structure by applying pressure between the "InP TE device" and the "Si TE device," forming the "InP/Si TE device," schematically as shown in Fig. 1b.

TE measurements of the InP TE device and InP/Si TE device were taken at average temperatures ranging between 300 and 350 K. (these devices are schematically shown in Fig. 1 and described above). Heat was supplied by a Joule heater to the top electrode of the device, while a heat sink removed heat from the bottom electrode, maintaining a constant temperature gradient. Current–voltage measurements were taken in the same direction of heat flow. Current–voltage measurements were taken at different temperature gradients by applying electrical voltage to the top electrode while the bottom electrode was grounded.

3 Results and discussion

Scanning electron microscopy (SEM) was used to investigate the InP NW growths on Cu coated with an evaporated Si layer before and after a PECVD Si layer was deposited. Figure 2a illustrates as-grown InP NWs from the two-step MOCVD growth described above. The two-step MOCVD growth promoted the formation of large, up to ~ 1 μm in diameter, spherical tips from 50 nm colloidal Au and ~ 250 nm caps stemming from 10 nm colloidal Au. These features provided an effective large surface area for the formation of a top electrode. As shown in Fig. 2b, the InP NW network and spherical tips grew up to 10 μm long. The InP NWs grew uniformly across the area of 2 cm × 2 cm with total length/area ratio in the range of 10–50 μm^{-1}. The InP NWs are oriented along the directions normal to the surface planes of non-single-crystalline evaporated Si domains. Therefore, the InP NWs grew in random directions. The evaporated Si layer served as a nucleation layer that promoted the formation of InP NWs on a Cu substrate, validated by the fact that InP grew as a polycrystalline film when deposited directly on a Cu substrate [35]. In Fig. 2c, d, SEM was further used to characterize morphology of the InP NWs after having been covered with a PECVD Si layer. This layer prevents electrical shorting upon the application of a top electrode. It is possible that in some areas where nanowire coverage was particularly lower than the average, a blanket Si layer was directly formed on the substrate and may dominate the electrical and thermal transport properties, which would have forced a portion of the electrical and thermal carriers to propagate through a PECVD Si layer not associated with the InP nanowires. However, based on SEM observation, the InP NWs cover >95 % of the substrate surface; thus, the contribution from the PECVD Si layer can be neglected for the purposes of this study.

Structural information of NWs is also vital for TE designs; therefore, transmission electron microscopy (TEM) was performed on the InP NW network covered with the PECVD Si layer in the single-stage InP TE device (i.e., Fig. 1a) and is shown in Fig. 2e. Shown in Fig. 2f is a selected area diffraction (SAD) pattern collected with a diffraction aperture that covered a large number of InP NWs. Based on unique features, fringe spacing, and pattern symmetry of multiple diffraction spots present in Fig. 2e, it

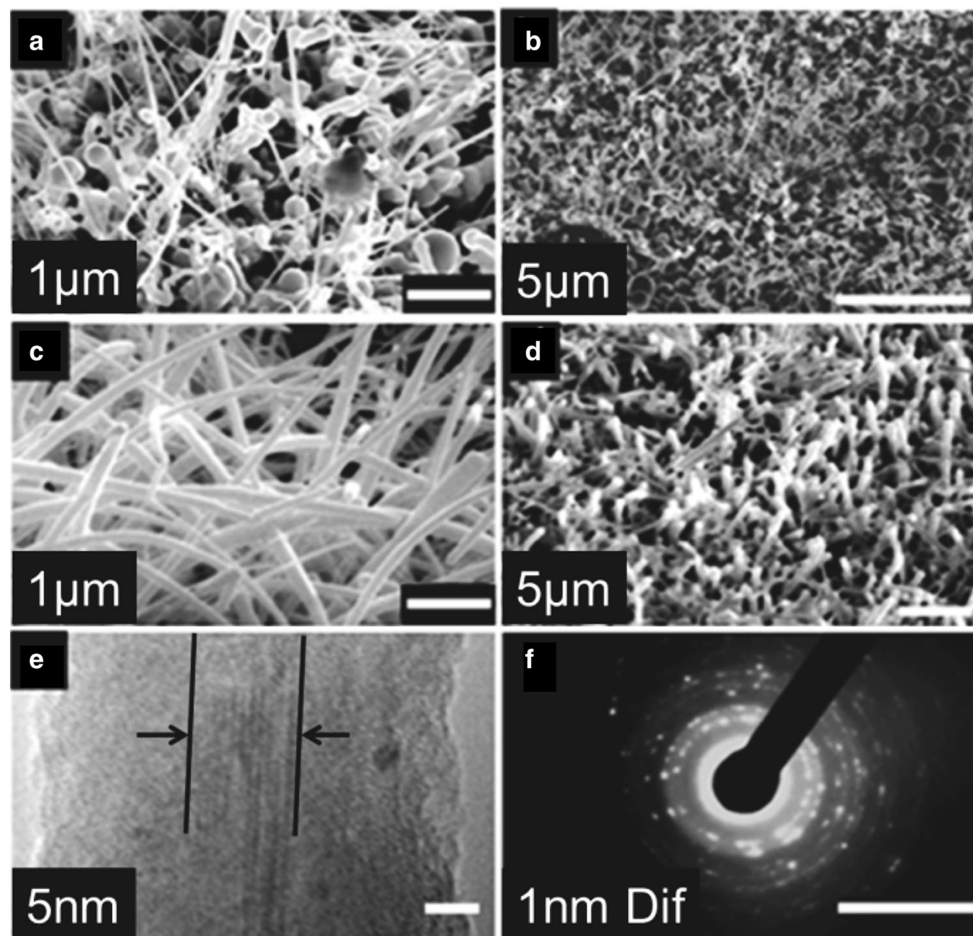


Fig. 2 Scanning electron microscope (SEM) images of InP grown by the two-step MOCVD growth prior to the PECVD Si layer deposition **a** at high magnification and **b** at low magnification. SEM images of the same sample after PECVD Si layer was deposited **c** at high magnification and **d** low magnification. **e** TEM imaging of the sample imaged in **c**–**d**. There appears to be an InP crystalline core with a Si shell. The InP core was delineated in the figure—the section indicated between *arrows*. **f** The diffraction pattern of the NW, indicating the presence of single-crystalline InP and polycrystalline Si

appears that the core of each NW is composed of single-crystalline InP oriented along their respective <111> directions. The PECVD Si layer formed a rough Si shell around the InP NW. The core–shell structure is theoretically expected to be beneficial in simultaneously providing a transport path for charged carriers and a scattering mechanism for phonons [40, 41]. Additionally, rough surface morphology has been shown to benefit TE properties of NWs [25, 42]. Diffraction rings slightly offset from each other were found to be associated with polycrystallinity of the Si shell. Therefore, the NW network used in the single-stage InP TE device is made of a large number of single-crystalline InP NW cores, each surrounded by a polycrystalline Si shell.

Figure 3 offers various images of Si NWs used in the single-stage Si TE device. Figure 3a shows a high magnification SEM image, revealing a 3D network of interconnections formed by fusing of neighboring NWs during growth. Previously, it was found that NW networks allow for electrical charge transport across farther trajectories than the length of the individual NWs [27]. With many conduction paths, electrical current will be able to flow readily through the network, whereas the interconnections may limit the propagation of phonons through the network, reducing thermal conductivity [43]. In Fig. 3b, it is shown that the average length of the NWs exceeds 15 μm. The Si NWs grew uniformly across the area of 2 cm × 2 cm with total length/area ratio in the range 20–100 μm^{-1}. A bright field TEM image of a representative NW is shown in Fig. 3c. The NWs exhibited a core–shell structure with the core being single-crystalline silicon and the shell being polycrystalline silicon. The Si crystalline cores ranged from 10 to 20 nm in diameter. NWs with crystalline cores and polycrystalline shells may potentially reduce thermal conductivity by scattering phonons in the polycrystalline shell, while the single-crystalline core provides a conduction path for electrical charges. The SAD pattern in Fig. 3d indicates that there are both single- and polycrystalline

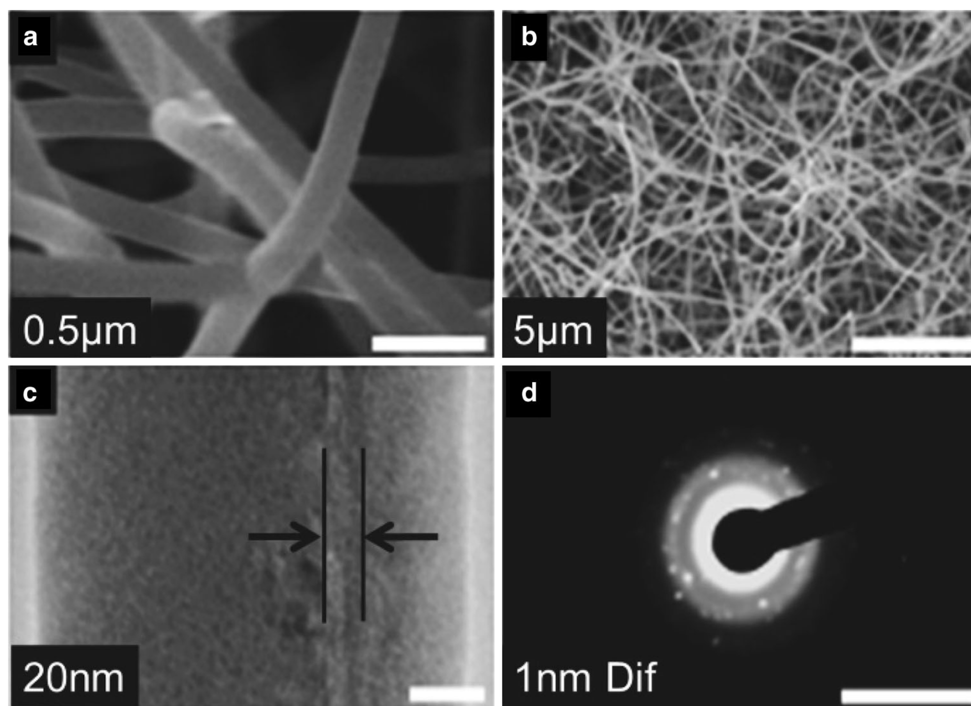


Fig. 3 SEM image of an unintentionally doped silicon NW network **a** at high magnification and **b** at low magnification. **c** TEM image of the same growth, showing delineation of a single-crystalline core in the NW. **d** The diffraction pattern of the Si NW indicates the presence of both single-crystalline and polycrystalline regions

phases. It appears that the zone is [110] with bright (111) spots of single-crystalline Si, with a slight rotation due to off tilt, and the surrounding shell is polycrystalline.

Current–voltage (*I*–*V*) measurements on the InP and InP/Si TE devices taken at various temperatures are shown in Fig. 4. Curves 4(a–d), representing the InP TE device, reveal n-type conduction characteristics with the *I*–*V* curves shifted into the second quadrant. Curves 4(e–g), representing the InP/Si TE device, reveal p-type conduction characteristics with the *I*–*V* curves shifted into the fourth quadrant. [Note: n-type and p-type bulk Si reference samples were used to calibrate the measurement setup and to confirm that n-type and p-type semiconductors show P_{gen} in the second and fourth quadrants, respectively]. Power produced by the InP TE device in the second quadrant suggests that the n-type PECVD Si top layer dominates the power production when combined with an unintentionally doped (UID) InP NW network. More specifically, electrons in the n-type PECVD Si top layer will easily dominate transport properties of the entire device, regardless of the presence of the unintentional doping of the InP NW network. Therefore, it is unsurprising that the overall device characteristics are more closely aligned with that of the sole doped layer (i.e., n-type PECVD Si layer). The fact that the InP/Si TE device produces power in the fourth quadrant (i.e., it behaves as a p-type material) and that the InP TE device produces power in the second quadrant (i.e., it behaves as an n-type material) suggests that the InP/Si TE device behaves as a p-type material overall, following the p-type conduction characteristics of the Si TE device.

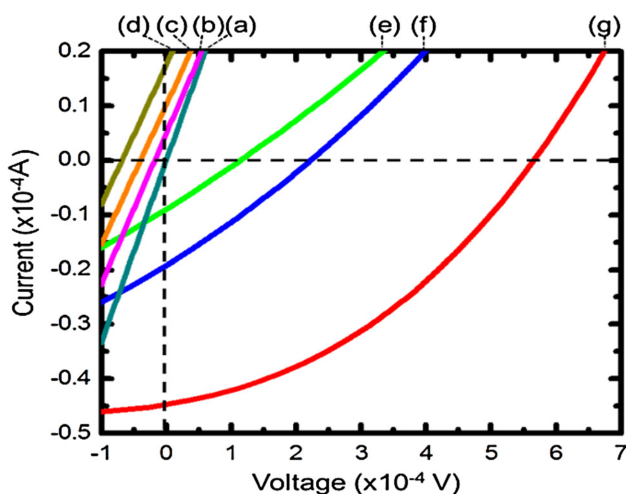


Fig. 4 Current versus voltage curves for the (**a**–**d**) InP TE device, and (**e**–**g**) InP/Si TE device. Temperature gradients were varied at **a** $\Delta T = 0$ °C, **b** $\Delta T = 30$ °C, **c** $\Delta T = 41$ °C, **d** $\Delta T = 50$ °C and **e** $\Delta T = 5$ °C, **f** $\Delta T = 20$ °C, and **g** $\Delta T = 51$ °C

Curves (a–d) in Fig. 4 representing the InP TE device show that as ΔT increases, so does V_{OC} and I_{SC}, along with

the area under the curve. This indicates that the maximum P_{gen} associated with each *I*–*V* curve increases as ΔT increases. Unlike semiconductor solar cells, the absence of a PN junction with a fixed doping on both sides enables the open-circuit voltage V_{OC} to increase when the temperature difference increases and is not limited by a fixed, built-in depletion region. Curves 4(e–g) of the InP/Si TE device also indicate that as the temperature difference increases, so does the maximum output power found on each *I*–*V* curve. The InP/Si TE device demonstrates a significant increase in power production when compared to the InP TE device at ΔT = 50 °C [i.e., curve 4(d)]. In contrast to the linear *I*–*V* curves 4(a–d), the *I*–*V* curves of the InP/Si TE device present nonlinear characteristics, which resemble *I*–*V* characteristics of photovoltaic (PV) cells at different illumination levels, obviating the dependence between V_{OC} and temperature for the reasons stated above. Such nonlinear *I*–*V* curves at various temperatures, based on its analogy to power production in PV cells, can be viewed as a means of increasing overall electrical power production for a given energy conversion efficiency in TE devices, when compared to traditional TE devices with linear *I*–*V* characteristics.

The nonlinear characteristics seen in InP/Si TE device pose an interesting concept that could be applied to the parameterization and optimization of semiconductor TE devices. The phenomenon of nonlinearity may arise from (1) one or more of the interfaces present in this device (in the form of a rectifying layer) as either a Schottky barrier or a PN junction, or (2) at the undoped NWs operating in the space-charge-limited (SCL) transport regime:

1. As nonlinearity is not exhibited by the InP TE device (see Fig. 1a), it is unlikely that a rectifying junction (e.g., PN junction) is present at the interface between the PECVD Si layer (n-type) and the p-type InP NWs. Additionally, the nonlinearity must not have been caused by the undoped 30 nm Si evaporated directly on Cu, considering the identical interfaces are also present in the single-stage InP TE device which does not exhibit nonlinearity. Moreover, we have previously tested Si NWs with different template layers and different doping layers (including UID) and found no trends of nonlinearity either [20, 21]. This barrier could therefore have been created by forming a PN junction when the n-type PECVD Si layer formed a contact with the UID, slightly p-type Si NW network. The nonlinear *I*–*V* curves (i.e., rectifying *I*–*V* curves) could indicate the presence of a Schottky barrier in the InP/Si TE device as shown in Fig. 1b. It has been previously reported that a Si/graphene interface creates a Schottky barrier with rectifying behavior [44–46], and a Schottky barrier could have formed along with the formation of graphene on the copper foil.
2. It has been reported that undoped semiconductor NWs experience space-charge-limited (SCL) transport with characteristic nonlinear IV curves. SCL dominates over small Schottky barriers at large enough voltages—a region where TE may be more efficient [33]. It is plausible that the Si NWs employed their higher Seebeck coefficient to induce a larger voltage difference in the device, augmenting the nonlinearity of InP NWs operating in the SCL region. Additionally, SCL transport theory indicates that efficiencies will scale proportionally with temperature, with the square of conductivity, and with the cube of the Seebeck coefficient, having the ability to exceed 10 % when NW diameters are reduced to 20 nm [33]. Thus, our results present a possible path to optimize electrical power generation from TE devices, by optimizing the curvature of nonlinear current–voltage characteristics. As nonlinearity—or the fill factor often used for PV—increases, so does efficiency. Therefore, it would be desirable to have a dopant concentration high enough to achieve low resistance contacts, yet low enough that the NW networks still operate in the SCL transport regime.

Figure 5a shows that the maximum power output of the InP TE device at $\Delta T = 50$ °C is $\sim$0.4 nW, a normalized power of 8×10^{-12} W/°C. The small power output is

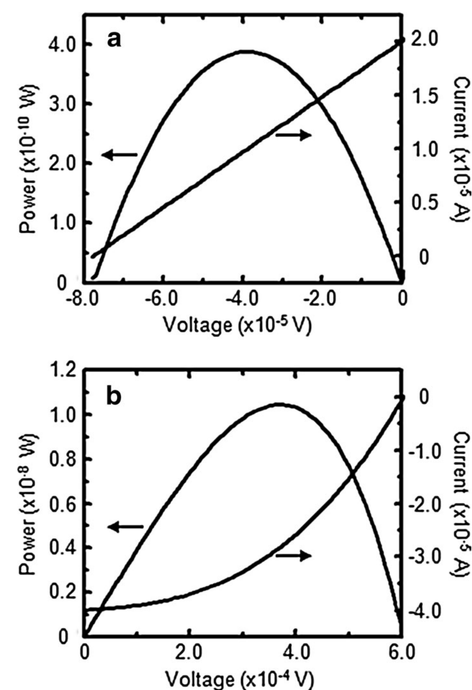


Fig. 5 Power and current versus voltage curves at $\sim$50 °C temperature differences are shown **a** for the InP TE device and **b** for the InP/Si TE device

Table 1 P_{max}, I_{SC}, and V_{OC} values for each TE device at $\sim\Delta T = 50$ °C

	I_{SC} (μA)	V_{OC} (mV)	P_{max} (nW)	Normalized power (nW/°C)	FF (fill factor)
InP	20	−0.08	0.4	0.008	0.25
InP/Si	−40	0.6	10.4	0.2	0.433

attributed to the InP NWs; the contact resistance between the UID NWs and the metallic interfaces reduced the overall conduction of the device. Moreover, the low doping of the InP NWs limits the conductivity of the device. A compromise between device conductivity and InP NW nonlinearity must be found and can be controlled by the doping level [30, 33]. When this UID InP NW layer is covered with the intentionally doped n-type PECVD Si layer, the overall electrical conduction results in n-type behavior as shown in the *I–V* curves(a–d) in Fig. 4.

Figure 5b reveals that the InP/Si TE device produced a maximum power of ~10.4 nW at $\Delta T = 51$ °C (i.e., normalized power $\sim 2 \times 10^{-10}$ W/°C). The normalized power increased approximately 25 times compared to that of Fig. 5a with the addition of the Si NW network layer. V_{OC}, I_{SC}, and other TE characteristics for the two devices are summarized in Table 1, showing that the addition of the Si NW network increases V_{OC} by a factor of 7.5, and the magnitude of I_{SC} by a factor of two. It appears that Si NWs enabled higher generated power by providing a better Seebeck effect, while the InP NWs offer nonlinearity to the device, increasing the power factor for a given I_{SC} and V_{OC}. The fill factor increased from 0.25 in the InP TE device (typical for a linear device) to 0.433 because of the nonlinearity effects present in the InP/Si TE device. The maximum current–voltage point (maximum power in Fig. 5b) could be optimized by changing the device nonlinear characteristics, and thus optimized for a given load. While the InP NWs may or may not increase, or even limit, the open-circuit voltage, they introduce a nonlinear current–voltage characteristic that can be used as another tuning knob to optimize a TE device.

The concept of TE devices with nonlinear current–voltage characteristics presented herein has a clear potential in increasing electrical power output. The fill factor of the nonlinear device (FF = 0.433) is larger than that obtained for a linear current–voltage curve found in conventional TE devices (FF = 0.25). Power output of these samples is low, due to significant performance limitations. However, the major cause is identified and can be alleviated by, for instance, properly doping NWs and semiconductor layers (e.g., PECVD Si and evaporated Si in Fig. 1a, b) present in a TE device. Given the additional attributes of mechanical flexibility and scalability, these TE devices present a viable option for befitting application to heat sources with large surface areas and/or odd shapes. Also, by constructing a device composed of concatenated cells of varyingly doped materials, a TE device can be optimized for a large temperature gradient, employing a series of materials with bandgaps appropriate for performance within different temperature ranges [47]. Furthermore, our device architecture allows to build a TE device that has a thickness much larger than that obtainable by conventional thin film deposition technologies or bulk semiconductor technologies, offering a new means to deal with large temperature gradients.

4 Summary and conclusions

We presented a new concept that can be applied to parameterize and optimize TE devices for electrical power generation: nonlinearity. The concept is built upon TE cells that are made of different semiconductor nanowire networks and that exhibit nonlinear current–voltage characteristics when concatenated. The origin of this nonlinearity phenomenon has not been conclusively identified in the current study and is the focus of continuing work. However, several potential origins were considered, including the presence of a Schottky barrier and the space-charge-limited transport regime in the nanowire layer; either (or both) of which may be inherent to the InP/Si TE devices presented in this work.

Acknowledgments This work was supported by NASA SBIR NNX11CE14P. The authors are grateful to HP laboratories and the MACS facility (Moffett Field, California) at Advanced Studies Laboratories, University of California Santa Cruz, and NASA Ames Research Center for continuous support on analytical equipment. This material is based on work supported by the National Science Foundation Graduate Research Fellowship under Grant No. DGE-0809125. Support by Semiconductor Research Corporation CSR fund (Dr. Victor Zhirnov) is also highly appreciated.

References

1. S.P. Beeby, T. O'Donnell, in *Electromagnetic Energy Harvesting*. Energy Harvesting Technologies (Springer, US, 2009), pp. 129–161
2. P. Shashank, D.J. Inman (eds.), *Energy Harvesting Technologies*, vol. 21 (Springer, New York, 2009)
3. G.J. Snyder, Small thermoelectric generators. Interface, vol. Fall, no. 2, 54–56 (2008)
4. A. Bulusu, D.G. Walker, Review of electronic transport models for thermoelectric materials. Superlattices Microstruct. **44**(1), 1–36 (2008)

5. J.R. Sootsman, D.Y. Chung, M.G. Kanatzidis, New and old concepts in thermoelectric materials. Angew. Chem. Int. Ed. **48**(46), 8616–8639 (2009)
6. T.M. Tritt, M.A. Subramanian, Thermoelectric materials, phenomena, and applications: a bird's eye view. MRS Bull. **31**(3), 188 (2011)
7. D.M. Rowe, *Thermoelectrics Handbook: Macto to Nano* (CRC Press, Boca Raton, 2006)
8. A.J. Minnich, M.S. Dresselhaus, Z.F. Ren, G. Chen, Bulk nanostructured thermoelectric materials: current research and future prospects. Energy Environ. Sci **2**(5), 466–479 (2009)
9. J.M.O. Zide, H. Lu, T. Onishi, J.L. Schroeder, J.E. Bowers, N.P. Kobayashi, T.D. Sands, A.C. Gossard, A. Shakouri, Novel metal/semiconductor nanocomposite and superlattice materials and devices for thermoelectrics, in *in proceedings - spie the international society for optical engineering*, vol 7683, pp. 76830V, Energy harvesting and storage: materials, devices, and applications. Orlando, Florida, United States von SPIE, Bellingham, Wash.5–6 April 2010
10. T.C. Harman, P.J. Taylor, M.P. Walsh, B.E. LaForge, Quantum dot superlattice thermoelectric materials and devices. Science **297**(5590), 2229–2232 (2002)
11. S.S. Stein, G. Savelli, P. Faucherand, L. Montes, Growth and characterization of QDSL (Quantum Dots Superlattices) of metal silicides in an n-doped SiGe matrix for thermoelectric applications, in *14th International Conference on Nanotechnology (IEEE-NANO)*. IEEE, 2014, pp. 64–69
12. P. Fan, Z. Zheng, Y. Li, Q. Lin, J. Luo, G. Liang, X. Cai, D. Zhang, F. Ye, Low-cost flexible thin film thermoelectric generator on zinc based thermoelectric materials. Appl. Phys. Lett. **106**, 073901 (2015)
13. R. Venkatasubramanian, E. Siivola, T. Colpitts, B. O'Quinn, Thin-film thermoelectric devices with high room-temperature figures of merit. Nature **413**(6856), 597–602 (2001)
14. H. Tsai, Effect of substrate type and thickness on power output of silicon nanowire thermoelectric device, in *2013 International Symposium on Next-Generation Electronics*, 2013, pp. 126–129
15. D. Dragoman, M. Dragoman, Giant thermoelectric effect in graphene. Appl. Phys. Lett. **91**(20), 10–13 (2007)
16. G.-H. Kim, L. Shao, K. Zhang, K.P. Pipe, Engineered doping of organic semiconductors for enhanced thermoelectric efficiency. Nat. Mater. **12**(8), 719–723 (2013)
17. O. Bubnova, X. Crispin, Towards polymer-based organic thermoelectric generators. Energy Environ. Sci. **5**(11), 9345 (2012)
18. F. Song, L. Wu, S. Liang, Giant Seebeck coefficient thermoelectric device of MnO_2 powder. Nanotechnology **23**(8), 085401 (2012)
19. W. Wang, F. Jia, Q. Huang, J. Zhang, A new type of low power thermoelectric micro-generator fabricated by nanowire array thermoelectric material. Microelectron. Eng. **77**(3–4), 223–229 (2005)
20. A.J. Lohn, E. Coleman, G.S. Tompa, N.P. Kobayashi, Assessment on thermoelectric power factor in silicon nanowire networks. Phys. Status Solidi **209**(1), 171–175 (2012)
21. K.J. Norris, M.P. Garrett, J. Zhang, E. Coleman, G.S. Tompa, N.P. Kobayashi, Silicon nanowire networks for multi-stage thermoelectric modules. Energy Convers. Manag. **96**, 100–104 (2015)
22. H. Yang, J.-H. Bahk, T. Day, A.M.S. Mohammed, G.J. Snyder, A. Shakouri, Y. Wu, Enhanced thermoelectric properties in bulk nanowire heterostructure-based nanocomposites through minority carrier blocking. Nano Lett. **15**, 1349–1355 (2015)
23. D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, A. Majumdar, Thermal conductivity of individual silicon nanowires. Appl. Phys. Lett. **83**(14), 2934–2936 (2003)
24. K.J. Norris, J. Zhang, D.M. Fryauf, E. Coleman, G.S. Tompa, N.P. Kobayashi, Single-polycrystalline core–shell silicon nanowires grown on copper, in *Proceedings of the SPIE*, vol. 8820, pp. 882013–882017 (2013)
25. A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najarian, A. Majumdar, P. Yang, Enhanced thermoelectric performance of rough silicon nanowires. Nature **451**(7175), 163–167 (2008)
26. A.I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W.A. Goddard, J.R. Heath, Silicon nanowires as efficient thermoelectric materials. Nature **451**(7175), 168–171 (2008)
27. A.J. Lohn, N.P. Kobayashi, AC surface photovoltage of indium phosphide nanowire networks. Appl. Phys. A **107**(3), 647–651 (2012)
28. G. Mahan, B. Sales, J. Sharp, Thermoelectric materials: new approaches to an old problem. Phys. Today **50**(3), 42 (1997)
29. L. Zhao, G. Tan, S. Hao, J. He, Y. Pei, H. Chi, S. Gong, H. Xu, V.P. Dravid, C. Uher, G.J. Snyder, C. Wolverton, M.G. Kanatzidis, Ultrahigh power factor and thermoelectric performance in hole-doped single-crystal SnSe. Science **2**, 1–7 (2015)
30. B.L. Sharma, *Metal-Semiconductor Schottky Barrier Junctions And Their Applications* (Springer, Berlin, 2013)
31. R.O. Loutfy, J.H. Sharp, Photovoltaic properties of metal-free phthalocyanines. I. Al/H2Pc Schottky barrier solar cells. J. Chem. Phys. **71**(1979), 1211 (1979)
32. R. Chenni, M. Makhlouf, T. Kerbache, A. Bouzid, A detailed modeling method for photovoltaic cells. Energy **32**, 1724–1730 (2007)
33. F. Léonard, Thermoelectric efficiency in the space-charge-limited transport regime in semiconductors. Phys. Rev. B Condens. Matter Mater. Phys. **86**, 1–5 (2012)
34. A.C. Gossard, W. Brown, C.L. Allyn, W. Wiegmann, Molecular beam epitaxial growth and electrical transport of graded barriers for nonlinear current conduction. J. Vac. Sci. Technol. **20**(1982), 694 (1982)
35. K.J. Norris, M. Garrett, E. Coleman, G.S. Tompa, J. Zhang, N.P. Kobayashi, Graphene mediated growth of polycrystalline indium phosphide nanowires and monocrystalline-core, polycrystalline-shell silicon nanowires on copper. J. Cryst. Growth **406**, 41–47 (2014)
36. A. Stranz, A. Waag, E. Peiner, High-temperature performance of stacked silicon nanowires for thermoelectric power generation. J. Electron. Mater. **42**(7), 2233–2238 (2013)
37. J. Zhang, D.M. Fryauf, K.J. Norris, M. Wei, J.J. Diaz Leon, N.P. Kobayashi, Raman spectroscopy of indium phosphide nanowire networks coated with gold clusters. J. Mater. Sci.: Mater. Electron. **25**(11), 4867–4871 (2014)
38. M. Wei, J. Zhang, D.M. Fryauf, J.J. Diaz Leon, K.J. Norris, H. Deng, G. Wen, S.-Y. Wang, N.P. Kobayashi, Growth and characterization of indium phosphide nanowires on transparent conductive ZnO:Al films. J. Mater. Sci. Mater. Electron. **25**(10), 4444–4449 (2014)
39. K.J. Norris, J. Zhang, D.M. Fryauf, N.P. Kobayashi, Two-step growth and fabrication of thermoelectric devices employing indium phosphide nanowire networks, in *Proceedings of SPIE - The International Society for Optical Engineering, SPIE NanoScience + Engineering*, vol. 8820, p. 88200Q (2013)
40. R. Yang, R. Yang, G. Chen, G. Chen, M.S. Dresselhaus, M.S. Dresselhaus, Thermal conductivity modeling of core–shell and tubular nanowires. Nano Lett. **5**, 1111–1115 (2005)
41. M. Hu, K.P. Giapis, J.V. Goicochea, X. Zhang, D. Poulikakos, Significant reduction of thermal conductivity in Si/Ge core–shell nanowires. Nano Lett. **11**, 618–623 (2011)
42. L. Liu, X. Chen, Effect of surface roughness on thermal conductivity of silicon nanowires. J. Appl. Phys. **107**(3), 033501 (2010)

43. K. J. Norris, J. Zhang, D. M. Fryauf, A. Rugar, A. Flores, T. J. Longson, A. J. Lohn, and N. P. Kobayashi, "Indium phosphide nanowire network: growth and characterization for thermoelectric conversion," *Proc. SPIE 8467, Nanoepitaxy Mater. Devices IV*, vol. 8467, p. 84670E–84670E–8, 2012
44. T. Feng, D. Xie, Y. Lin, H. Zhao, Y. Chen, H. Tian, T. Ren, X. Li, Z. Li, K. Wang, D. Wu, H. Zhu, Efficiency enhancement of graphene/silicon-pillar-array solar cells by HNO_3 and PEDOT-PSS. Nanoscale **4**, 2130 (2012)
45. Y. An, A. Behnam, E. Pop, A. Ural, Metal-semiconductor-metal photodetectors based on graphene/p-type silicon Schottky junctions. Appl. Phys. Lett. **102**, 1–5 (2013)
46. S. Tongay, M. Lemaitre, X. Miao, B. Gila, B.R. Appleton, A.F. Hebard, Rectification at graphene–semiconductor interfaces: zero-gap semiconductor-based diodes. Phys. Rev. X **2**, 1–10 (2012)
47. J.O. Sofo, G.D. Mahan, Optimum band gap of a thermoelectric material. Phys. Rev. B **49**(7), 4565 (1994)