

Representation of type I heterostructure junctionless tunnel field effect transistor for high-performance logic application

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Abstract In this paper, a gate-all-around junctionless tunnel field effect transistor (JLTFET) based on heterostructure of compound and group III–V semiconductors is introduced and simulated. In order to blend the high tunneling efficiency of narrow band gap material JLTFETs and the high electron mobility of III–V JLTFETs, a type I heterostructure junctionless TFET adopting Ge–Al_xGa_{1–x}As–Ge system has been optimized by numerical simulation in terms of aluminum (Al) composition. To improve device performance, we considered a nanowire structure, and it was illustrated that high-performance logic technology can be achieved by the proposed device. The optimal Al composition founded to be around 20 % ($x = 0.2$). The numerical simulation results demonstrate that the proposed device has low leakage current I_{OFF} of $\sim 1.9 \times 10^{-17}$, I_{ON} of 4 $\mu\text{A}/\mu\text{m}$, $I_{\text{ON}}/I_{\text{OFF}}$ current ratio of 1.7×10^{11} and subthreshold swing SS of 12.6 mV/decade at the 40 nm gate length and temperature of 300 K.

1 Introduction

Over the past several decades, the continuous scaling of metal oxide semiconductor field effect transistors (MOSFETs) beyond constraints of planar structure requires multigate devices like FinFETs [1], omega-gate FETs [2] and gate-all-around FETs [3]. However, these structures are also subjected to various physical limits such as short-channel effects (SCEs) and high standby power dissipation.

In order to dominate these stringent demands, newly junctionless field effect transistor (JLFET) has been proposed and fabricated which does not require PN junctions and ultra-shallow concentration gradient at lateral junctions [4, 5]. However, it has significant leakage OFF-state current due to its bulk conduction which leads to high values of power consumption. Lately, tunneling filed effect transistors (TFETs) based on band-to-band tunneling (BTBT) mechanism are achieving popularity as one of the most promising devices for ultra-scaled MOSFETs, due to their low-OFF-state current (I_{OFF}) and steep subthreshold swing (SS) below the thermionic limit of 60 mV/decade [6–9]. Results that stem from atomistic modeling have shown that TFETs potentially can perform superior than conventional FETs at low supply voltages [10, 11]. On the other hand, it has been pointed out that silicon-based TFETs have rather low ON-state current (I_{ON}), which makes it inappropriate in high-performance (HP) applications [12, 13]. In order to achieve high tunneling current (I_{ON}), various kinds of compound semiconductors like III–V material [14] with small effective mass and narrow staggered energy band are required [15]. Recently, a new structure named junctionless tunnel field effect transistor (JLTFET) has been proposed which is tunnel FET without any abrupt doping profile [16–19]. It has presented good ON-state current and low subthreshold swing as blends advantages of JLFETs and TFETs. JLTFET also features lower subthreshold slope than conventional MOSFET and JLFET at the room temperature opens new future for low-power application devices [16]. In this paper, we have performed a comparative study on type I heterostructure junctionless TFET (IH-JLTFET) with homojunction JLTFETs based on various materials. Also, we have achieved an optimum design for an IH-JLTFET of Ge–Al_xGa_{1–x}As–Ge system by 2D device simulation to meet HP requirements. It is proved

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that the aluminum (Al) composition (x) in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ channel affects the total current, whereas it was simulated for 0 (GaAs) to 0.4 Al mole fraction with 0.05 step. It is shown that higher mole fraction x of aluminum leads to further degradation of ON-state current (I_{ON}), defect formation at the channel interface and high values of threshold voltage (V_{th}) for HP logic technology. Moreover, we have investigated the energy band diagram profile in the ON state and OFF states for a Ge– $\text{Al}_x\text{Ga}_{1-x}\text{As}$ –Ge H-JLTFET. The lateral electric field and potential pattern of the device are examined in both the states. Further, transfer characteristics of the proposed structure compared with prior homo- and heterostructure JLTFETs are simulated for constant drain voltage $V_{\text{DS}} = 1$ V. Finally, the overall optimization of the device structures such as I_{ON} , I_{OFF} , ON/OFF current ratio, subthreshold swing (SS) is analyzed by adjusting the different mole fraction of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ configurations.

2 Device structure and simulation

2.1 Device structure

The 3D schematic view and cross section along the channel of the IH-JLTFET are shown in Fig. 1. The type I heterostructure junctionless tunnel field effect transistor (IH-JLTFET) does not contain any doping junctions as the channel is uniformly n-type doped. Therefore, it is potential solution to the problem of random dopant fluctuations. It is fundamentally a hetero-channel heavily n-type-doped ($1 \times 10^{19} \text{ cm}^{-3}$) JLTFET by the concept of band-to-band tunneling. The device is the junctionless-based TFET with a channel length of 40 nm, source/drain extension length of 30 nm and nanowire film thickness of 10 nm. The gate oxide thickness is 2 nm and isolation layer in between middle gate (MG) and side gate (SG) is 2 nm, which works as a spacer. In

Table 1 Simulated device parameters of IH-JLTFET

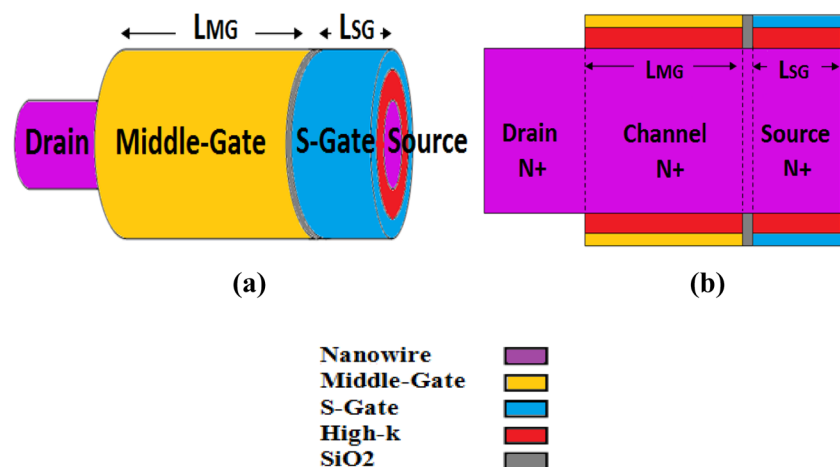
Parameter	Value
Source/drain/channel doping (N_{D})	$1 \times 10^{19} \text{ cm}^{-3}$
Effective oxide thickness (T_{OX})	2 nm
Middle-gate workfunction (Φ_{MG})	4.45 eV
Side-gate workfunction (Φ_{SG})	5.6 eV
Gate length (L_{g})	40 nm
Source/drain length ($L_{\text{s,d}}$)	30 nm
Channel thickness (T_{ch})	10 nm
Supply voltage (V_{DD})	1 V
Permittivity of gate dielectric material (ϵ_{d})	25

order to provide better electrostatic controllability of gate over channel region, gate-all-around technology is used. Also, HfO_2 as gate dielectric is included. It could be implemented utilizing atomic layer deposition (ALD) and this technique resulted in lower surface oxide defects. Preset parameters used for device simulation of IH-JLTFET as shown in Fig. 1 are tabulated in Table 1.

Typically, the IH-JLTFET is a lateral n-type JLTFET, which uses two isolated gates (MG and SG) of two different metal workfunctions, to make the layer beneath the gates intrinsic and p-type, respectively [17, 18]. The proposed device is a quantum mechanical device (QMD), and tunneling of electrons depends on the barrier width between the energy band of source–channel and drain–channel. Hence, in order to implement higher I_{ON} and $I_{\text{ON}}/I_{\text{OFF}}$ device with lower subthreshold swing, steeper energy bands have to be created with propinquity of bands in tunneling region with higher band overlap [20, 21]. Use of heterojunction of Ge at source and $\text{Al}_x\text{Ga}_{1-x}\text{As}$ at channel side satisfies above condition.

In order to make the layers beneath MG and SG intrinsic and p-type, respectively, we have deliberately varied the metal workfunction from 4.2 to 4.6 and 5.1 to 5.7 eV,

Fig. 1 a Sketch of the gate-all-around IH-JLTFET, b its cross section along z -axis. For the device, the gate near the tunneling region is named as middle gate (MG), and the other is denoted as side gate (SG)



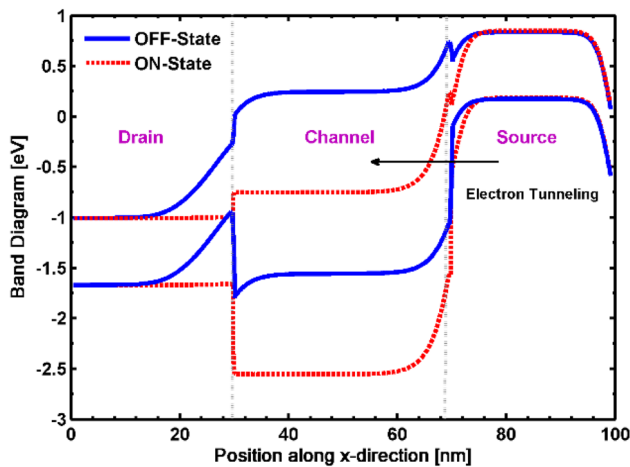


Fig. 2 OFF-state ($V_{DS} = 1$ V, $V_{MGS} = 0$ V) and ON-state ($V_{DS} = 1$ V, $V_{MGS} = 1$ V) energy band diagrams of 100-nm Ge- $\text{Al}_x\text{Ga}_{1-x}\text{As-Ge}$ H-JLTFET

respectively. For all the devices in this study, the workfunction of 4.45 and 5.6 eV for MG and SG has chosen which give the superior result in terms of SS and ON-/OFF-state current values. The integration of MG and SG together in the fabrication process, whose workfunctions are different, could be done by using the techniques as reported in Refs. [22–24]. The formation of the isolation layer with thickness of 2 nm of SiO_2 could be done either by using a sputtering process or by a modern photolithography process (such as electron beam lithography, X-ray lithography, extreme ultraviolet lithography and ion projection lithography) after formation of the field oxide by wet oxidation.

The simulated energy band diagrams of the proposed Ge- $\text{Al}_x\text{Ga}_{1-x}\text{As-Ge}$ H-JLTFET with the position at the channel and gate dielectric interface for operating mode ($V_{MGS} = V_{DS} = 1$ V) and standby mode ($V_{MGS}, V_{DS} = (0, 1$ V) are shown in Fig. 2. In the absence of gate voltage, there is no overlap between the occupied band of the source and the unoccupied band of the channel. In this case, the probability of tunneling of electrons is negligible, so the OFF-state current flows only because of an $\text{N}^+ \text{-I-P}^+$ diode leakage and consequently gives extremely small current (I_{OFF}). Contrarily, as the gate voltage becomes increasingly positive from the OFF state, band edges at the source end will bend more, making the tunneling barrier increasingly thinner. Hence, there is a high possibility of tunneling of electrons from a valence band of the source to the conduction band of the channel which result in a significant amount of current flows due to the quantum tunneling mechanism. Like in a TFET, we apply gate voltage only on the MG (the gate above the intrinsic region of the device) to turn the device on. The voltage of MG is varied from 0 to 1 V for turning the device on.

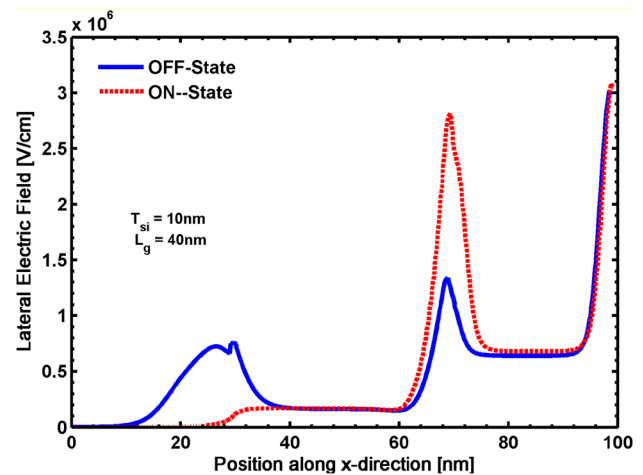


Fig. 3 OFF-state ($V_{DS} = 1$ V, $V_{MGS} = 0$ V) and ON-state ($V_{DS} = 1$ V, $V_{MGS} = 1$ V) lateral electric field profile of 100-nm Ge- $\text{Al}_x\text{Ga}_{1-x}\text{As-Ge}$ H-JLTFET

The lateral electric field profile of the suggested device as a function of position along x -direction for ON state and OFF state is illustrated in Fig. 3. In the OFF state, because the formation of band diagram profile looks like $\text{N}^+ \text{-I-P}^+$ -doped device structure, it has been created two electric field peaks at the source-channel and drain-channel interface. However, In the ON state, because of the application of gate-to-source voltage, the band diagram profile behaves similar to $\text{N}^+ \text{-N-P}^+$ -doped device structure, so it has been created one strong electric field peak at the source-channel interface. The strong electric field peak in between the source and channel regions implicates that tunneling is taking place in that region due to the quantum tunneling phenomenon. It is also seen that this high electric field peak is observed at the source contact side in both states. This peak is because of reversed biased P-N junction formation near the interface of the source region, since near the interface of the source region electrons do not get completely depleted. Because of this the interface near the source region is still an n-type region. The surface potential distributions along the channel for both the ON state and OFF state are further investigated in Fig. 4. From the figure, it is explicit that the voltage is gradually varying from the drain toward the source side with the flat region. This trend indicates the region below the gate electrode where no doping junctions are present, and the electric field is almost zero, as shown in Fig. 3. In the ON state as the gate-to-source voltage increases, the electron concentration of the device layer below the drain and channel regions increases and becomes almost an n-type region. This results in narrowing of the barrier between the source and channel of the device, and consequently, the potential increases.

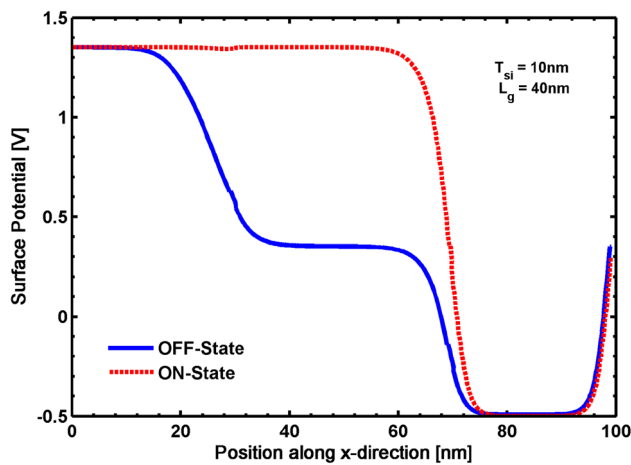


Fig. 4 OFF-state ($V_{DS} = 1$ V, $V_{MGS} = 0$ V) and ON-state ($V_{DS} = 1$ V, $V_{MGS} = 1$ V) surface potential profile of 100-nm Ge- $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -Ge H-JLTFET

The remarkable numerical simulation work has been reported on type I heterostructure TFET [25, 26]. In fabrication, $\text{Al}_x\text{Ga}_{1-x}\text{As}$ can be epitaxially grown on Ge substrate by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) to make up the Ge- $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -Ge heterostructure. In a similar fashion, Ge:AlGaAs H-JLTFET could be fabricated through epitaxial growth process. $\text{Al}_x\text{Ga}_{1-x}\text{As}$ can be grown directly on Ge since their lattice constants are very similar at room temperature, $5.6533 + 0.0078x$ and 5.658 Å, respectively. It is noteworthy that in analyzing the simulation results, the average subthreshold swing (SS_{AVG}) was defined as the average slope between the onset point of drain to source where current crosses $I_{DS} = 1 \times 10^{-7}$ A/ μm current (I_{DS}) and the reference point at $I_{DS} = 1 \times 10^{-15}$ A/ μm on the I_D - V_{GS} transfer curve [27]. The I_{ON} and I_{OFF} were calculated by supply voltages of ($V_{DS} = 1$ V, $V_{MGS} = 1$ V) and ($V_{DS} = 1$ V, $V_{MGS} = 0$ V), respectively.

2.2 Simulation configuration

All simulations evaluated using 2D TCAD simulator Silvaco AtlasTM version 5.16.2.R [28]. We use nonlocal band-to-band tunneling (BTBT) model [29] to account for the amount of current accumulated due to tunneling of electron from source to channel side of the regime. We comprise the effect of Fermi-Dirac statistics in the calculation of the intrinsic carrier concentration required in the expressions for Shockley-Read-Hall (SRH) recombination. To capture the effect of temperature-dependent mobility, a concentration-dependent mobility (CONMOB) model and parallel and perpendicular electric field-dependent mobility (FLDMOB) model are used. Due to the presence of high doping concentrations, band gap narrowing (BGN) and

auger recombination (AUGER) models are included in the simulations. Moreover, in order to assume high impurity atom in the channel and also to take into account an interface trap (or defect), the SRH recombination mode is enabled [30]. To include quantum confinement effects at the Si/SiO₂ interface due to heavy doping concentration and thin oxide thickness, quantum confinement (HANSCHQM) model given by Hansch [31] is considered. Trap-assisted tunneling (SCHENK.TUNN) model given by schenk [32] to account for interface trap effect on electron band-to-band tunneling in TFETs is enabled.

3 Results and discussion

3.1 Advantages over prior homo- and heterostructure JLTFETs

Figure 5 compares the simulated I_D - V_{GS} characteristics from homostructure JLTFETs of which materials are Si, Ge [16]. Also, a simulated transfer curves from InAs-GaSb and SiGe-Si-Si heterostructure JLTFETs in the previous researches have been brought to make further comparison with the proposed device [17, 18]. The doping concentrations of all the JLTFETs are 1×10^{19} cm⁻³ within the source, drain and channel region. For the high doping concentration, the ON/OFF current ratio is high due to enhancing the energy band overlap between the source and channel at ON-state. From Fig. 5, it is explicit that Ge homostructure JLTFET encompasses higher I_{ON} tunneling current compared with silicon one. The E_G 's of Ge and Si are 0.66 and 1.12 eV, respectively. In sequence, since a

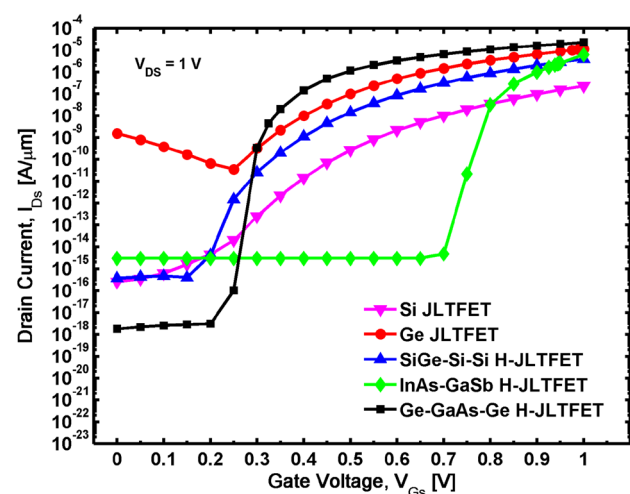


Fig. 5 Comparison among I_D - V_{GS} curves from Si, Ge, homostructure junctionless TFETs with SiGe-Si-Si, InAs-GaSb and Ge-GaAs-Ge heterostructure junctionless TFETs

smaller E_G intensifies the BTBT proficiency and the electron mobilities of Ge and Si are $3900 \text{ cm}^2/\text{V s}$ and $1400 \text{ cm}^2/\text{V s}$, respectively, I_{ON} of a Ge JLTFT is much higher than that of a Si device. SiGe source for higher tunneling proficiency and Si drain for reducing I_{OFF} more effectively can be adjoined to improve the device performances. Process attempts on Si:Si $_{1-x}$ Ge $_x$ interface resulted significant progress and indicated it as most suited candidate in heterostructure TFETs [33, 34]. In that case, values of I_{ON}/I_{OFF} and subthreshold swing are finer with the presence of SiGe at source side while they drop drastically in the presence of larger band gap silicon material at source side. In the InAs–GaSb H-JLTFT, GaSb with a band gap of 0.726 eV in the drain side and InAs with a band gap of 0.354 eV in the source side enhances BTBT current between the source and the channel. As indicated in the Figure, relatively small leakage I_{OFF} current flows due to the large barrier width for tunneling in the drain and channel interface. Finally, the proposed device with Ge–AlGaAs–Ge heterojunction shows superior transfer characteristics comparable to other homo- and heterostructure JLTFTs. For a good comparison, no Al composition was introduced to match gate-to-source voltage where the minimum I_{OFF} 's appear. The suggested device presents higher tunneling barrier width modulation at higher gate voltage which reasons higher I_{ON} and steeper switching.

Here, I_{ON} is determined by the mixture effect of magnitude of E_G for BTBT at the source-to-channel junction and electron mobility in the channel. Despite the small value of Ge band gap at the source-to-channel junction, larger value of electron mobility of GaAs about $8000 \text{ cm}^2/\text{V s}$ results in excellent transition probability. In that situ, I_{ON} converges to that of Ge JLTFT while I_{OFF} is kept lower than other features as shown in Fig. 5, which is the best performance achievable by the group III–IV semiconductor materials.

One of the main obstacles of Ge JLTFT is high leakage OFF current as shown in Figs. 5 and 6. A smaller band gap of Ge enhances the tunneling current by gate-induced drain leakage (GIDL) at the channel-to-drain junction when a negative gate voltage is applied. Figure 6 illustrates I_D – V_{GS} curves for Ge JLTFT and the proposed IH-JLTFT based on Ge–Al $_x$ Ga $_{1-x}$ As–Ge system for aluminum mole fraction $x = 0, 0.15$ and 0.3 . It is clear that the current drivability is reduced as x composition increases. For the value of $x = 0.15$, I_{ON} of Ge JLTFT and a Ge–Al $_x$ Ga $_{1-x}$ As–Ge H-JLTFT are comparable, but I_{OFF} of the latter is much lower. By introducing more Al atoms, band gap gets larger which is the technique for suppressing I_{OFF} . On the other hand, the electron mobility is degraded which lowers I_{ON} . As a result, the analysis results support that introducing a heterojunction formed by Ge and Al $_x$ Ga $_{1-x}$ As enables to expect improved I_{ON} due to a small E_G of the source-side

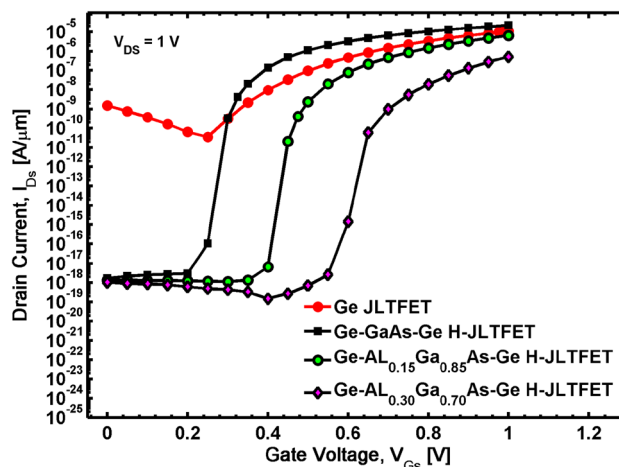


Fig. 6 Comparison between Ge JLTFT and Ge–Al $_x$ Ga $_{1-x}$ As–Ge H-JLTFTs with different Al compositions

Ge and high electron mobility of Al $_x$ Ga $_{1-x}$ As channel. It is also retaining I_{OFF} sufficiently low by a large E_G of Al $_x$ Ga $_{1-x}$ As which reduces GIDL at the same time.

3.2 Design improvement in the nanowire IH-JLTFT

It is necessary to optimize the proposed device performance by introducing more mole fraction x of aluminum in the channel side Al $_x$ Ga $_{1-x}$ As. Figure 7 illustrates the transfer curves for the proposed IH-JLTFTs with different Al composition (x) values at a given $V_{DS} = 1 \text{ V}$. It is explicit from the figure, as the Al fraction gets further, E_G become larger and in sequence effectively suppressed ON-state tunneling current (I_{ON}). From the I_{OFF} and ambipolar behavior points of view, the I_{OFF} current conductivity

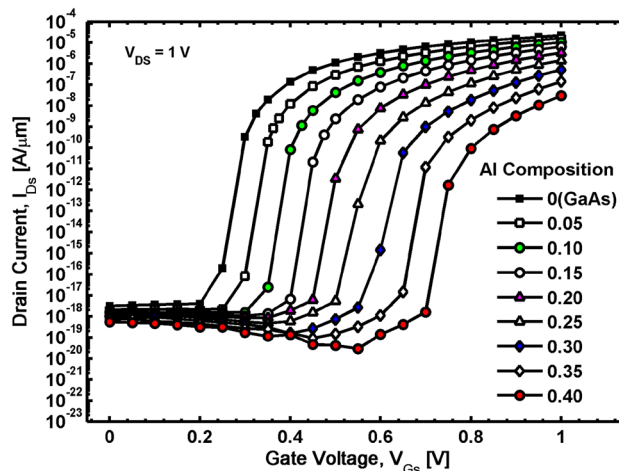


Fig. 7 Transfer characteristics curves of Ge–Al $_x$ Ga $_{1-x}$ As–Ge IH-JLTFTs with different Al atoms fractions in the channel

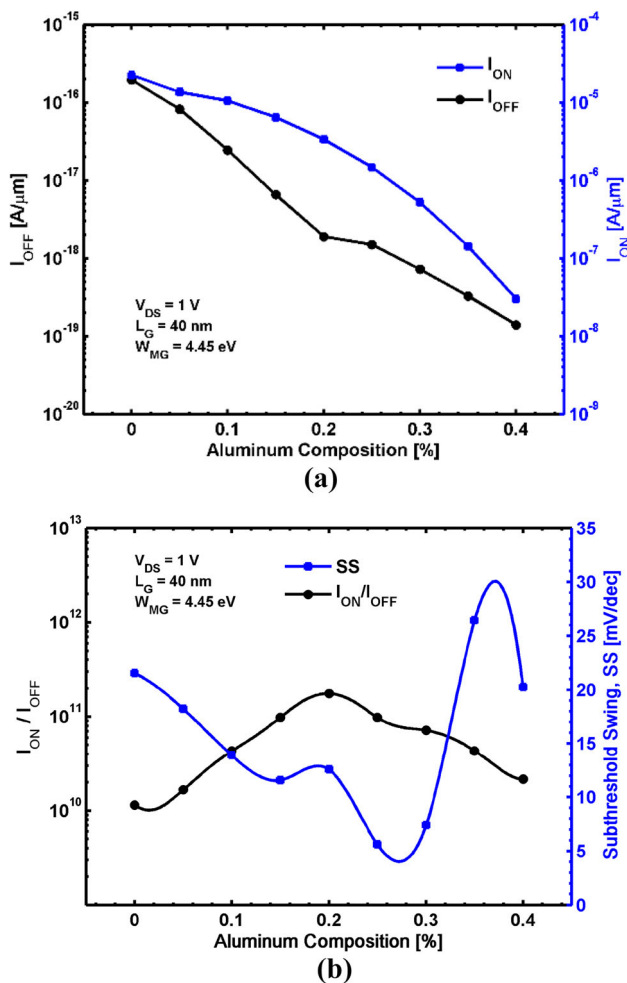


Fig. 8 **a** Variations of the OFF-state current I_{OFF} and ON-state current I_{ON} ; **b** variation of the ON/OFF current ratio and the subthreshold swing SS. The MG length is 40 nm, and its workfunction is $W_{MG} = 4.45$ eV

becomes a few lower and consequently limited ambipolar behavior substantially due to gate-induced drain leakage (GIDL) at the drain and channel junction. Figure 8 presents the extracted I_{ON} , I_{OFF} , SS and I_{ON}/I_{OFF} as a function of Al composition where mole fraction $x = 0$ of Aluminum corresponds to Ge–GaAs–Ge H-JLTFET. As shown in Fig. 8a, it is observed that both I_{ON} and I_{OFF} decrease as mole fraction x increases. These metrics are in trade-off relation, and higher I_{ON} and lower I_{OFF} cannot be obtained at the same time. Hence, it is necessary to put a weight on a narrowed number of parameters of interest in determining the Al fraction. Also, Fig. 8a reveals that the permissible x values required to meet HP application should be limited between 0 and 0.2 due to the reason that the upper limit of I_{ON} (minimum I_{ON}) is in Al mole fraction $x = 20$ %. The average subthreshold swing and the ON/OFF current ratio as a function of x are presented in Fig. 8b. It was already shown that the proposed IH-JLTFETs had better SS

characteristics than other homo- and heterostructure JLTFETs in Figs. 5 and 6. The obtained SS values in Fig. 8b were below 25 mV/dec and reduced monotonically up to an Al composition of 0.25, where a local minimum was observed. Although the SS characteristics were significantly degraded at $x = 0.4$, it was still very low value. Since low SS and high I_{ON}/I_{OFF} are desirable for HP applications, altogether it can be seen from Fig. 8 that the value of $x = 20$ % is a suitable choice when I_{ON}/I_{OFF} and SS are 1.77×10^{11} and 12.6 mV/decade, respectively. It is observed that the proposed Ge– $\text{Al}_x\text{Ga}_{1-x}\text{As}$ –Ge H-JLTFET with the variation of Al composition is well suited for HP logic technology. Also, $x = 20$ % can be good selection for I_{ON} , I_{OFF} , SS, I_{ON}/I_{OFF} point of view, simultaneously with remarkable simplicity in the fabrication progress.

4 Conclusion

In summary, we have examined a gate-all-around type I heterostructure junctionless TEFT (IH-JLTFET) contingent upon Ge– $\text{Al}_x\text{Ga}_{1-x}\text{As}$ –Ge heterostructure which has been designed and optimized in terms of Al fraction and its performance characteristics were explored using 2D numerical simulation. When mole fraction x of aluminum for active region $\text{Al}_x\text{Ga}_{1-x}\text{As}$ was selected to be 0.2 as an optimum value, device metrics have reasonable value to meet HP logic requirements. For 40-nm active region, very low I_{OFF} leakage current $\sim 1.9 \times 10^{-17}$, high ON/OFF current ratio (I_{ON}/I_{OFF}) about 1.77×10^{11} and steep subthreshold swing (SS) of order of 12.6 mV/decade at the $V_{DS} = 1$ V are extracted. Due to these superior characteristics for ultra-scaled geometries within its compatibility with nanowire structure, Ge– $\text{Al}_x\text{Ga}_{1-x}\text{As}$ –Ge H-JLTFET would be a promising candidate to complementary MOS-FET technology.

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