Appl. Phys. A (2016) 122:588
DOI 10.1007/s00339-016-0116-6

Applied Physics A
Materials Science & Processing

CrossMark

Modified dislocation filter method: toward growth of GaAs on Si by metal organic chemical vapor deposition

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Received: 14 December 2015 / Accepted: 3 May 2016 / Published online: 11 May 2016
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Abstract In this paper, metamorphic growth of GaAs on (001) oriented Si substrate, with a combination method of applying dislocation filter layer (DFL) and three-step growth process, was conducted by metal organic chemical vapor deposition. The effectiveness of the multiple InAs/GaAs self-organized quantum dot (QD) layers acting as a dislocation filter was researched in detail. And the growth conditions of the InAs QDs were optimized by theoretical calculations and experiments. A 2-μm-thick buffer layer was grown on the Si substrate with the three-step growth method according to the optimized growth conditions. Then, a 114-nm-thick DFL and a 1-μm-thick GaAs epilayer were grown. The results we obtained demonstrated that the DFL can effectively bend dislocation direction via the strain field around the QDs. The optimal structure of the DFL is composed of three-layer InAs QDs with a growth time of 55 s. The method could reduce the etch pit density from about 3×10^6 cm^{-2} to 9×10^5 cm^{-2} and improve the crystalline quality of the GaAs epilayers on Si.

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1 Introduction

The heteroepitaxy of GaAs on Si substrate is of great interest because of its potential applications in the optoelectronic integrated circuits and optoelectronic devices. For the integration with integrated circuit devices, high-quality GaAs epilayers on Si are required. The major bottleneck problem required to be solved is the formation of high-density threading dislocations (TDs). The TDs result from the lattice mismatch between the III–V compounds like GaAs and Si [1, 2]. And the presence of anti-phase domains also results in high dislocation density in III–V materials [3]. The growth of GaAs on Si by molecular beam epitaxy (MBE) was firstly reported in the 1980s [4], and it was also achieved by metal organic chemical vapor deposition (MOCVD) in the same year [5]. Both of these researches used a two-step growth method. Since then, various dislocation reduction techniques such as thermal cycle annealing (TCA) [6], strained-layer superlattices (SLS) [7, 8], an amorphous Si buffer layer [9], selective evaporation of dislocated region [10], selective area or patterned growth [11], aspect ratio trapping (ART) [12, 13], AlSb buffer layer [14] and compliant substrates [15] have been proposed.

In recent years, there have been several novel methods reported to further improve the crystalline quality of metamorphic growth of GaAs/Si films. Among them, the three-step growth method [16, 17] and the dislocation filter layer (DFL) with multilayer quantum dots (QDs) [18–20] have obtained commendable experiment results. The three-step growth method is a modified two-step growth method by inserting an intermediate-temperature (IT) layer between the low-temperature (LT) layer and the high-temperature (HT) layer. It can effectively decrease the surface roughness and TD density [16] of the grown GaAs epilayers. In addition, the DFL with InAs QDs can reduce

the dislocation density by bending dislocation direction with the strong strain field around the QDs. When the dislocation propagates near the QDs, they would be exerted by strong Peach–Koehler forces [21], then the propagation of dislocations would be eventually blocked, and the quality of GaAs/Si films would be improved. However, the dislocation density of GaAs/Si epilayer which only use the three-step growth method or the DFL with QDs individually does not meet the requirement for fabricating high-quality devices. The three-step growth method can reduce dislocation density and improve the surface morphology in GaAs/Si epilayers [16], and such obtained GaAs/Si epilayers acting as buffer layers can enhance the crystalline quality of the QDs [22]. Moreover, the DFL with such QDs not only remains no dislocation, but also has good effectiveness of blocking dislocations. Thus, the combination of these two methods can give full play to their advantages. By the theoretical analysis and experimental optimization, the combination is more effective at improving the crystalline quality of GaAs/Si epilayers. In this study, we combine the DFL and the three-step growth method together. The theoretical calculation is conducted to optimize the size and the layer number of InAs QDs as the DFL. Experiments for adjusting growth time and layer number of the DFL are performed too. Then, the optimized DFL structure composed of three-layer self-organized InAs QDs with 55 s growth time is determined. The measurement results show that the etch pit density (EPD) of the GaAs/Si epilayers obtained is as low as 9×10^5 cm^{-2}.

2 Analysis

Figure 1 shows the cross-sectional view of the growth process and growth conditions for GaAs/Si samples with InAs QDs as DFL and three-step method in this study. The effectiveness of dislocation bending is theoretically analyzed in this section.

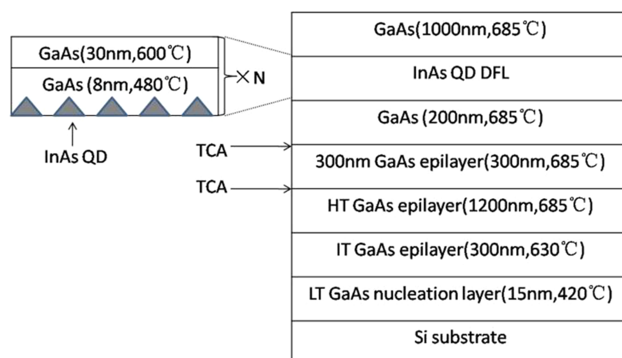

Fig. 1 Schematic of epitaxial structure, growth process, and growth conditions of GaAs/Si samples with InAs QDs as DFL

To block the propagation of TDs in GaAs/Si lattice-mismatched heterostructures, the self-organized multilayer InAs/GaAs QDs are used as a three-dimensional (3-D) dislocation filter. In this study, the influence, of QD size and QD layer number, on the effectiveness of the DFL is analyzed by a quasi-3-D model of strain–dislocation interaction. The optimized structure of the DFL will be determined through the theoretical calculation. The optimization of the DFL makes it to more effectively block TDs and reduce the dislocation density of the upper GaAs epilayer. Normally, the QDs with proper size are coherently strained and dislocation-free. If the size of QDs continues increasing beyond a critical size, coherent growth will become incoherent growth with the generation of misfit dislocations. Since the QDs as DFL should remain free of dislocations, the size of the QDs was considered smaller than the critical size in our analysis.

The TDs are generated at the interface of GaAs/Si films and then propagate toward the multilayer QDs. Being equal to or greater than the dislocation self-energy ΔE_{dis}, the strain energy ΔE_{rel} releases due to the generation of the misfit dislocation and the TD direction is changed [23, 24].ΔE_{rel} and ΔE_{dis} are described by the following equations.

$$\frac{\Delta E_{dis}}{L} = \frac{1}{2\pi} \frac{G_{buff} G_{dot}}{G_{buff} + G_{dot}} \left(\frac{1 - v\cos^2\beta}{1 - v} \right) b^2 \left[\ln\left(\frac{2r}{b}\right) + 1 \right] \quad (1)$$

$$\frac{\Delta E_{rel}}{L} = \frac{2G_{dot}(1 + v)}{(1 - v)} f_{eff} b_{eff} h \quad (2)$$

In the equations, L is the length of the mismatch dislocation, G_{buff} (G_{dot}) is the shear modulus of buffer layer (dots), v indicates the Poisson ratio ($\cong$0.3 for GaAs and InAs), β represents the angle between the dislocation line and the Burger's vector, b is the Burger's vector, b_{eff} is a component of b parallel to the interface of buffer layer and QD layer, and h is the QD height. r represents an outer cutoff radius of the dislocation bending area, which is assessed by the distance to the nearest dislocation-free space. $f_{eff} = f\sqrt{1 - \exp(-\kappa/p)}$ denotes the effective lattice mismatch between the QD and the underlying layer ($\kappa \approx 0.09$ from the valence force field model [25]). We assume that the self-organized QD is in a pyramidal shape with base width W and height $h = pW$, where p is height–width ratio of a single QD [18, 23, 24].

With Eqs. (1)–(2), the bending area—underlying the QD within which a threading dislocation direction can be bent when $\Delta E_{dis} \leq \Delta E_{rel}$—can be calculated. As shown in Fig. 2a, the bending-area ratio of a single QD is defined as the bending area divided by the area of the QD base, and the bending-area ratio of a single QD layer is that the bending area of QDs divided by the area of QD layer, shown in Fig. 2b. According to our previous experiments [20, 26], the QD height is chosen changing from 1.5 to

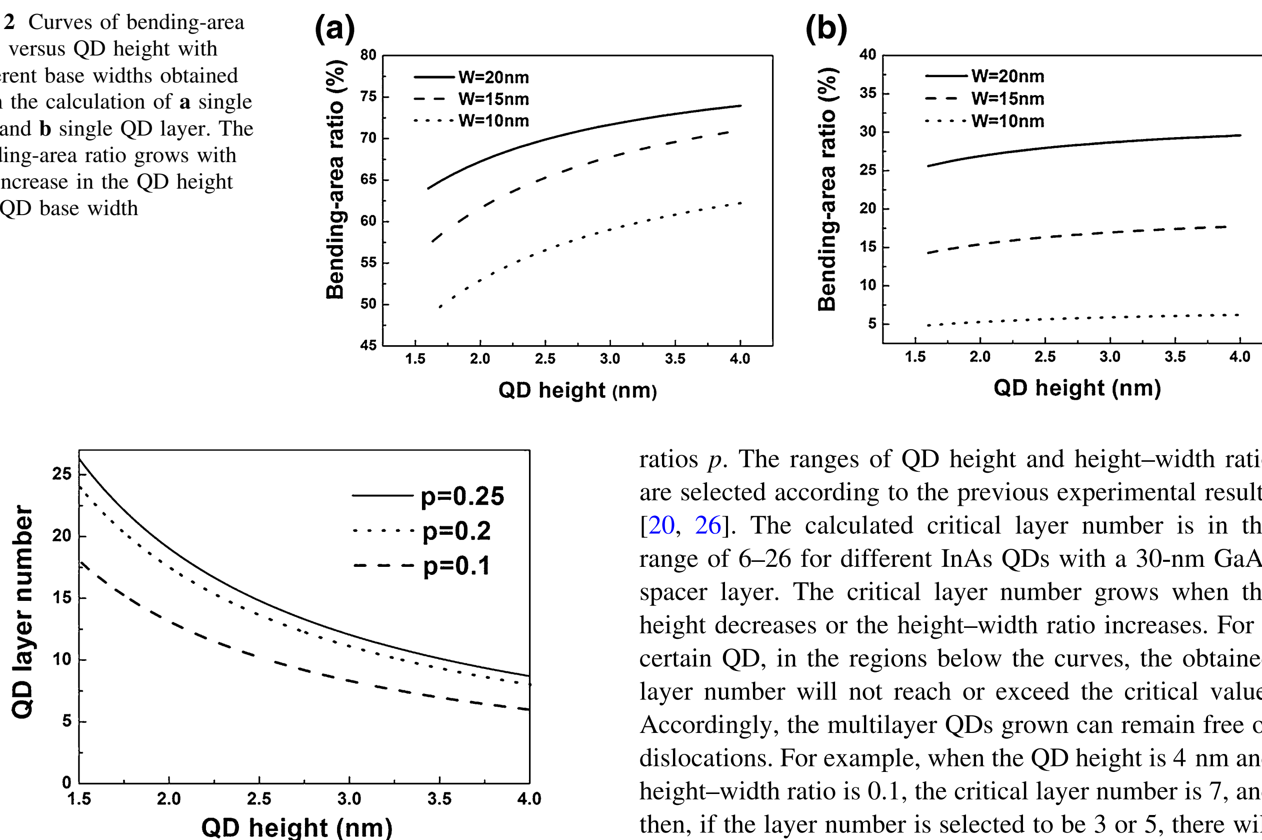

Fig. 2 Curves of bending-area ratio versus QD height with different base widths obtained from the calculation of **a** single QD and **b** single QD layer. The bending-area ratio grows with the increase in the QD height and QD base width

Fig. 3 Critical layer number for multilayer InAs QDs with different height–width ratios obtained from the calculation. The critical layer number decreases with the increase in the QD height

4 nm and the QD density is 10^{11} cm^{-2} in the theoretical calculation, and the results are shown in Fig. 2. The curves in both figures represent the bending-area ratio with different base widths of 10 nm, 15 nm, and 20 nm, respectively. It shows that the bending-area ratio grows as the QD height h and the QD base width W increase in Fig. 2a, but the bending-area ratio of single QD layer only significantly grows with increasing W in Fig. 2b. The highest bending-area ratios are about 75 % for a single QD and about 30 % for a single QD layer in Fig. 2a and b, which appear at a QD height of 4 nm and a base width of 20 nm.

On the one hand, when too many QD layers are grown, a mass of strain will be accumulated, which will be released by generating single-kink and double-kink misfit dislocation loops [18]. On the other hand, when too few QD layers are grown, the effectiveness of the DFL for bending dislocation direction will be deteriorated. So we need to find out the optimal number of layers for the DFL. By using the above equations, the critical layer number could be estimated, which is the largest layer number of the QDs before generating misfit dislocations [18, 27].

Figure 3 shows the critical layer number for multilayer InAs QDs with different QD heights h and height–width ratios p. The ranges of QD height and height–width ratio are selected according to the previous experimental results [20, 26]. The calculated critical layer number is in the range of 6–26 for different InAs QDs with a 30-nm GaAs spacer layer. The critical layer number grows when the height decreases or the height–width ratio increases. For a certain QD, in the regions below the curves, the obtained layer number will not reach or exceed the critical value. Accordingly, the multilayer QDs grown can remain free of dislocations. For example, when the QD height is 4 nm and height–width ratio is 0.1, the critical layer number is 7, and then, if the layer number is selected to be 3 or 5, there will be no dislocation generated from the DFL.

The calculation results also indicate that the QDs with bigger size are more suitable as the DFL. Moreover, the critical layer number is less for the bigger size QDs. If the resulted layer number is too few, the performance of the DFL will be deteriorated. So we need to balance the trade between the QD size and the QD layer number to optimize the effectiveness of the DFL. When the base width of a single QD decreases, the bending-area ratio of single-layer QD declines dramatically. In this situation, even if layer number increases, the effectiveness of blocking dislocations would be not enhanced. So the better result between using the QDs with larger base width and the QDs with more layers will be determined through the experiment.

3 Experimental optimization of dislocation filters

According to our experiments of QD growth, the size of QDs can be easily controlled by manipulating the growth time, and the QD size affects the ability of the DFL to block dislocation [18]. In addition, the layer number of multiple QDs also has influence on the performance of DFL. In our experiments, the growth time of the QDs and the layer number of the DFL are optimized in sequence. And then, the improved conditions are used to grow GaAs/Si samples. In this section, our experiments on the growth

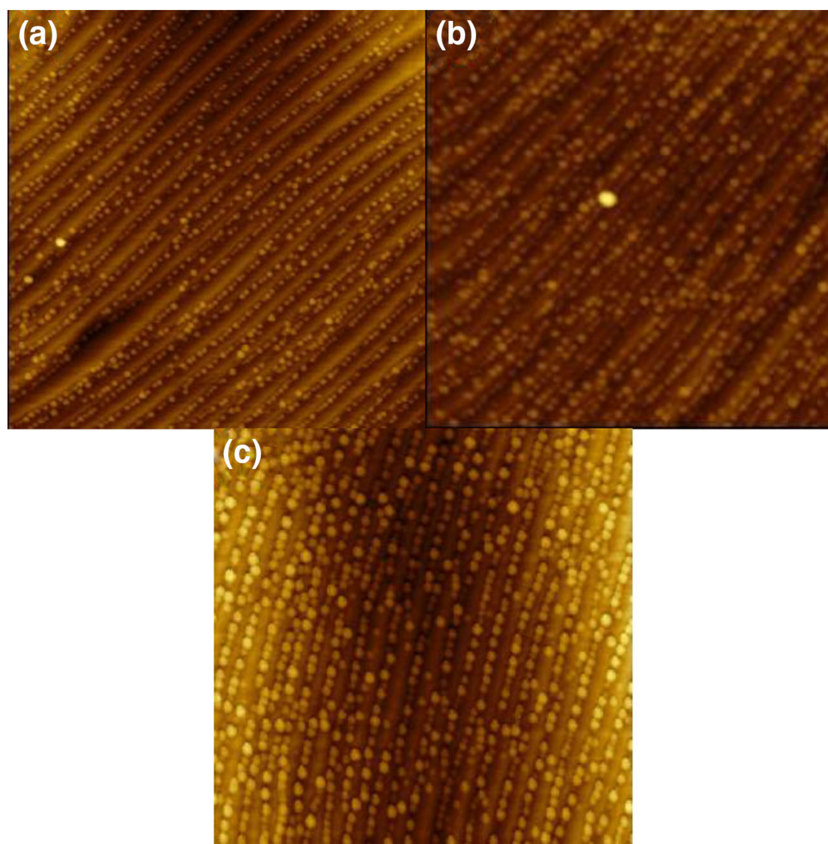

Fig. 4 (*Color online*) AFM images (1 μm × 1 μm) of the single-layer QDs with different QD growth times of **a** 55 s, **b** 60 s, and **c** 65 s. As the growth time increased, the size of the quantum dots became bigger and large clusters appeared

time of the QDs, the layer number of multilayer QDs, and the growth of GaAs/Si films with the DFL will be described.

The growth of GaAs on Si was carried out at a Thomas Swan 3 × 2 inch close-coupled showerhead MOCVD system. The carrier gas was Pd-cell purified hydrogen, and high-purity trimethylgallium (TMGa), trimethylindium (TMIn), and arsine were used as source materials. The misoriented Si (100) substrates were 4° off toward <011> for inhibiting the formation of anti-phase domains, and after chemical cleaning, the oxide was removed from the surface by dilute hydrofluoric acid (HF) solution. Our growth experiments were performed on a graphite susceptor with a constant pressure of 100 Torr. Firstly, the three-step growth of GaAs/Si films was conducted. For the three-step growth, a 15-nm-thick initial LT GaAs nucleation layer was grown at 420 °C, followed by a 300-nm-thick IT GaAs epilayer grown at 630 °C and a 1500-nm-thick HT GaAs epilayer grown at 685 °C. Secondly, in order to obtain a higher crystalline quality of metamorphic GaAs, the TCA was also inserted in the process of the three-step growth. Every TCA step contained three cycles. In each cycle of the TCA process, the GaAs/Si wafers were first heated to 750 °C in 7 min; then, the temperature was stabilized for 5 min; after that, the wafers were cooled down to 350 °C in 7 min; finally, the temperature was held for 6 min. During the whole TCA process, the GaAs/Si wafers were in an arsine and hydrogen ambient. Lastly, 200-nm-thick GaAs were grown on the top. We used the above process to grow GaAs on Si as GaAs virtual substrates, and the InAs QDs were grown on them for optimizing growth conditions.

Apart from the growth conditions those optimizing, other fixed growth conditions of QDs are as follows: growth temperature, V/III ratio, and growth rate are 480 °C, 6, and 0.036 ML/s, respectively; the thickness and growth temperature of the cap layer are 8 nm and 480 °C; the thickness and growth temperature are 30 nm and 600 °C for the space layer between QD layers [20, 28].

At first, a single layer of InAs QDs was grown with different growth times of 55 s, 60 s, and 65 s, and observed by atomic force microscope (AFM), while the other conditions were fixed. The AFM images of the samples are shown in Fig. 4. We found that when the growth time was 55 s, their size and distribution were nearly uniform, while only a few small size clusters were generated. When the growth time was 60 s or 65 s, the size of QDs increased and the distribution of QDs became uneven with the appearance of big clusters. The appearance of the big clusters implied that the QD size was beyond the critical

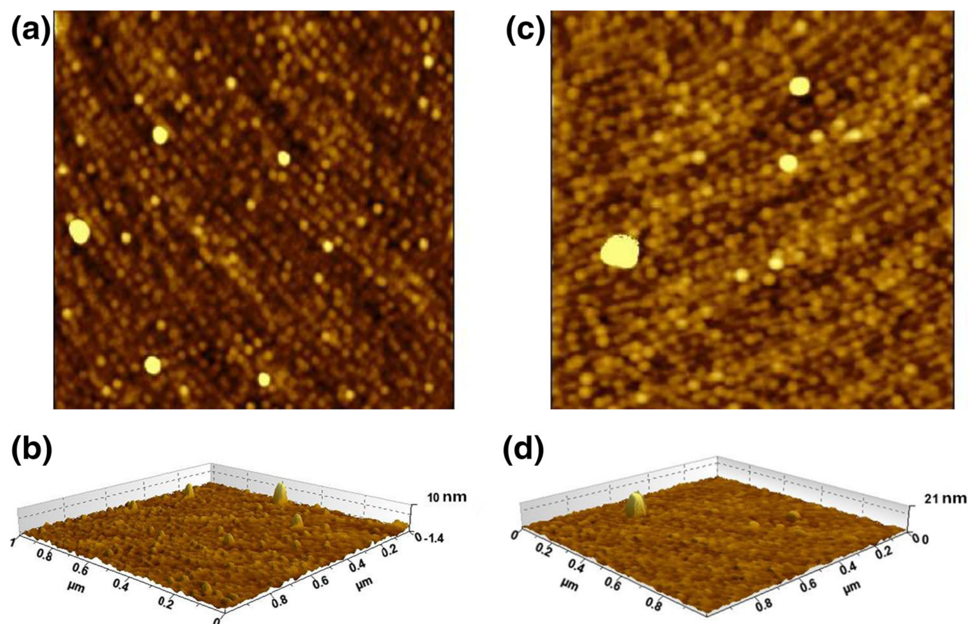

Fig. 5 (*Color online*) AFM images (1 µm × 1 µm) of InAs QDs grown with different layer numbers, **a** the plane view and **b** the three-dimensional view of the three-layer InAs QDs, **c** the plane view and **d** the three-dimensional view of the five-layer InAs QDs. More large clusters appeared in the sample with five-layer QDs

size with the generation of misfit dislocations [23]. And the QDs as DFL should remain not dislocated. So according to the analysis of the above results, the optimized growth time of QDs was chosen to be 55 s. Basing on the theoretical calculation, the larger dots were more suitable as dislocation filters. Hence, the growth time less than 55 s was unnecessary to consider.

Then, the contrast experiment for layer number of the QDs was performed. According to theoretical optimization and our previous works, we grew two samples with three layers and five layers of QDs, respectively, shown in Fig. 5. The growth conditions were same as the single-layer QDs. Comparing with the three-layer QDs, more big clusters appeared in the five-layer QDs. The dislocations were generated universally in the DFL along with the large clusters. And basing on our experiments, the layer number of more than five had exceeded the actual critical layer number of the multiple QDs and dislocations formed [20]. Hence, the three-layer QDs were considered more suitable as the DFL in this experiment.

To directly observe the DFL with InAs QDs, transmission electron microscope (TEM) measurement was taken. Several typical areas were selected to view from the two samples with different layer numbers of the QDs. As shown in Fig. 6a, the five-layer InAs QDs generated dislocations themselves, and the dislocations propagated upward in the regions marked by white frames. The reason was that the strain accumulation of five-layer QDs was very large and many big islands appeared with the generation of dislocations in the DFL, while there was no dislocation generated from the DFL with the three-layer QDs, as shown in Fig. 6b. Therefore, the three-layer InAs QDs structure was chosen as the DFL. Finally, the growth time of QDs with 55 s and the structure of the DFL with three-layer QDs were determined through experimental optimization. Comparing with our previous works using a five-layer QDs structure as the DFL, the growth conditions and the structure of the DFL were improved [20]. The general trend of the experimental results was consistent with theoretical calculation.

Basing on the above experiment results, we grew the sample with three-layer QDs as the DFL and three-step growth method. The sample of GaAs/Si epilayer was grown by MOCVD according to the epitaxial structures, as shown in Fig. 1. After the three-step growth, the DFL was grown using the same conditions of the above experiments. Finally, 1-µm GaAs was grown, and the growth conditions were the same as the HT GaAs epilayer.

4 Results and discussion

The sample was fabricated using the above growth process and growth conditions. Then, the EPD was used to estimate dislocation density and observe the improvement in the material quality of GaAs on Si. Otherwise, TEM measurements were taken to accurately evaluate the dislocation density and elucidate the kinetics of the defects.

4.1 EPD

The EPD was obtained after etching the sample with molten KOH. The GaAs epilayers were etched about 300 nm at about 310 °C with an etching rate of 150 nm/min. Then, the sample was dipped in $HCl:H_2O = 1:20$ solution for 5 min to remove the residual KOH. After

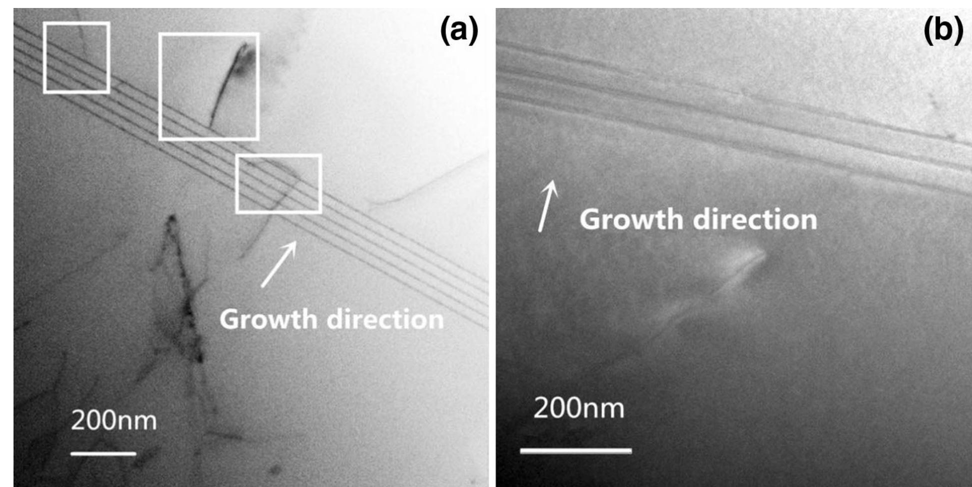

Fig. 6 Cross-sectional TEM images of two samples, **a** the sample with five layers QDs and three-step method growth, and **b** the sample with three-layer QDs and three-step method growth. The dislocations generated in the sample of five layers QDs, but not generated in that of three-layer QDs

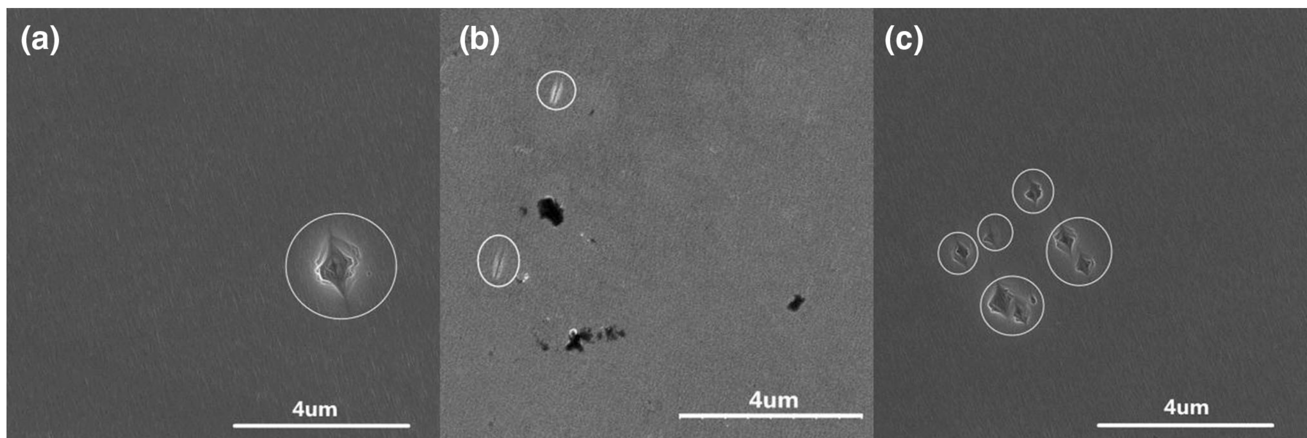

Fig. 7 Etch pit density SEM morphologies of three samples, respectively, with **a** DFL and three-step growth method, **b** three-step growth method only, and **c** DFL only. All the etch pits were marked by the white circles. Fewer etch pits presented in (**a**) with the combination of the two methods than in (**b**) and (**c**)

etching, the sample was observed by scanning electron microscope (SEM). The etch pit morphology is shown in Fig. 7a. The EPD of the sample was 9×10^5 cm^{-2}. The etching pits mainly concentrated in a few small regions, and no etching pit occurred in most of the regions of the sample. The reason was that the big clusters appeared, and the crystalline quality of QDs themselves deteriorated in these regions, which resulted in the generation of dislocations. The EPD decreased significantly compared to the sample using only the three-step growth method or the DFL, as shown in Fig. 7b, c [16, 20].

4.2 TEM

Figure 8 shows the TEM images of the regions of the GaAs/Si interface and the DFL in the sample. It can be found that high dislocation density at the GaAs/Si interface was shown in Fig. 8a, and in some areas, most dislocations either glided or annihilated when they penetrated to the surface during the TCA step in the process of the epitaxial growth. And the dislocations those were not blocked can propagate to the upper layers. As shown in Fig. 8b, the TEM images demonstrated evidential bending behavior of dislocation direction by the DFL in the region marked by the white frame. Dislocations were blocked and could not pass to the above GaAs epilayer while propagating toward the DFL. In addition, the dislocations did not occur in the DFL. So the DFL can effectively reduce TDs and improve the crystalline quality of the upper GaAs epilayer.

The measurement results of EPD and TEM indicated that the dislocation density of the GaAs/Si epilayer was reduced by the combination method of applying the DFL with three-layer QDs and the three-step growth method, and the combination of the two methods can effectively give full play to their advantages [16, 18, 20].

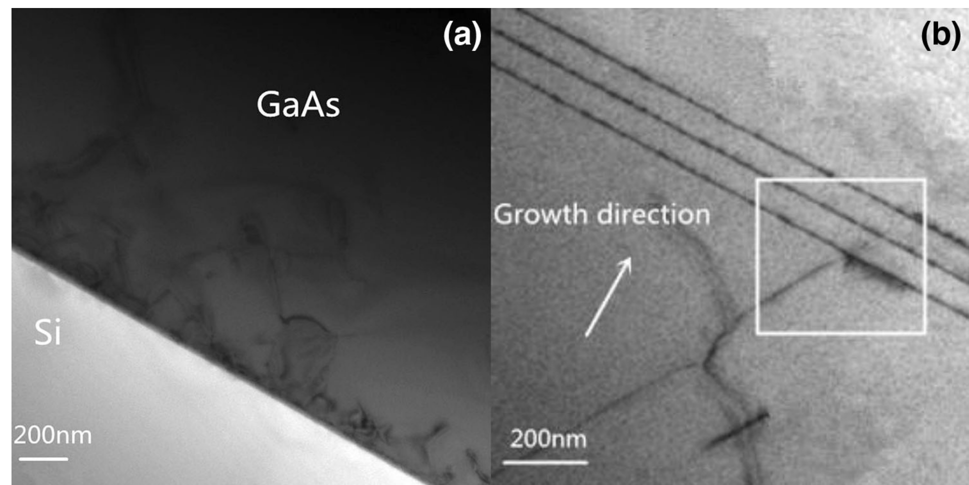

Fig. 8 Cross-sectional TEM figures of the samples, **a** the interface of GaAs/Si, **b** dislocation propagation in DFL with three-layer InAs QDs

5 Summary and conclusion

We demonstrated that the method including the DFL with InAs QDs and the three-step growth process can effectively improve crystalline quality of metamorphic GaAs on Si. In this study, a 3-μm-thick metamorphic GaAs/Si with low EPD of 9×10^5 cm^{-2} was obtained, and evident bending behavior of dislocations by the DFL was shown. As a result of the deviation between theoretical calculation and actual situation in the experiment, the actual experiment results have not reached the theoretical results. But the results of theoretical calculation can provide the guide for our experiments. Optimization of the experimental conditions would be further conducted to improve the crystalline quality of GaAs on Si. We believe that our research could provide a potential way of making low-cost and high-quality monolithically integrated III–V optoelectronic devices on Si.

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