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Annealing effects on the electrical, structural and morphological properties of Ti/p-GaN/Ni/Au Schottky diode

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Abstract Rapid thermal annealing effects on the electrical, structural and surface morphological properties of a fabricated Ti/p-GaN Schottky diode (SD) have been investigated. The AFM results showed that the surface morphology of the Ti/p-GaN SD is reasonably smooth at different annealing temperatures. The estimated Schottky barrier height (SBH) of the as-deposited and 200 °C annealed Ti/p-GaN SDs is found to be 0.88 eV (*I–V*)/1.02 eV (*C–V*) and 0.91 eV (*I–V*)/1.11 eV (*C–V*). Results showed that the SBH increases to 0.98 eV (*I–V*)/1.26 eV (*C–V*) upon annealing at 300 °C for 1 min in N_2 ambient. However, the SBH slightly decreases to 0.94 eV (*I–V*)/1.17 eV (*C–V*) after annealing at 400 °C. Using Norde method and Cheung's functions, the series resistance, SBH and ideality factor of the Ti/p-GaN SD are estimated and discussed at various annealing temperatures. Also, the difference between the SBHs calculated by *I–V* and *C–V* methods are discussed. Further, the interface state density N_{ss} of the Ti/p-GaN SD is calculated and it is found to be decreases upon annealing at 300 °C and then slightly increases after annealing at 400 °C. Experimental electrical results are also correlated with the interfacial microstructure of the Ti/p-GaN SD. The SIMS and XRD results revealed that the increase or decrease in the SBHs of the Ti/p-GaN SD upon annealing could be attributed to the formation of Ti–N and Ga–Ti interfacial phases at the interface.

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1 Introduction

In recent years, gallium nitride (GaN) is one of the promising semiconductor materials among wide band gap semiconductors for the development of high-power, high-frequency and high-temperature electronic devices such as metal–semiconductor field effect transistors (MESFET), high electron mobility transistors (HEMTs) [1, 2], blue/ultraviolet light emitting devices [3, 4], sun blind solar detectors [5], and Schottky rectifiers [6]. The understanding of the electrical and surface properties of metal–GaN interfaces are important in order to control the complex devices [7, 8]. The rectifying contacts that have high Schottky barrier height (SBH) and good thermal stability are critical for the realization of electronic devices. Hence, the development of Schottky contacts to GaN with good thermal stability, high barrier height (BH) and low leakage current is still a scientific challenge.

A higher SBH ($q\phi_b$) is expected for p-GaN since the sum of the BHs of *n* and p-GaN adds up to the GaN band gap of 3.4 eV [9, 10]. However, there is a quite large discrepancy in the reported SBH values for most metals on p-GaN, ranging from ~0.5 to 2.9 eV even for the same metal [11–16]. Several researchers have made attempts to form Schottky contacts with different metal schemes on p-type GaN [12, 17–25]. For example, Yu et al. [12] investigated the electrical properties of Ni/p-GaN Schottky diode (SD) by current–voltage–temperature (*I–V–T*) and capacitance–voltage (*C–V*) characteristics. They reported that the BH values ranging from 2.68 to 2.87 eV (*C–V*). Kim et al. [17] investigated the SBH of Ti/Al/p-GaN Schottky junction by *C–V* measurements at 1.5 kHz. They found that the maximum BH (1.43 eV) was obtained at 300 K. Tan et al. [18] fabricated the Cr/p-GaN SDs and investigated its electrical characteristics by current–voltage

(I–V) at different annealing temperatures (500–1000 °C) and reported that the SBH of the diode was drastically increased to 1.01 eV after annealing at 600 °C and then decreased to 0.61 eV upon annealing at 700 °C for 5 min. Tsai et al. [19] found that the Pt/SiO_2/GaN MIS devices exhibited better hydrogen-sensing ability than the Pt/GaN (MS). Thus the SiO_2 insulator surface plays a strikingly important role in producing the excellent hydrogen-sensing response. Tsai et al. [20] studied hydrogen-sensing properties of a Pt/oxide/GaN metal–oxide–semiconductor type SD. They reported that the shift in I–V curves and decrease in turn-on voltage are found to be caused by the lowering of SBH in the hydrogen-containing environment. Fukushima et al. [21] fabricated the rare earth metals Dy, Er, and Gd Schottky contacts on p-GaN and reported that the SBH were 1.91, 2.38, and 2.16 eV from I–V and 1.79, 1.78 and 1.70 eV from C–V measurements respectively. Park et al. [22] reported that the SBHs of Ti, Cu, Pd, and Pt contacts were 0.85, 070, 0.61, and 0.59 eV, respectively, using thermionic emission (TE) model. Jang et al. [23] studied the temperature-dependent electrical characteristics of non-alloyed Ti/p-GaN SBD in the temperature range of 293–443 K. They reported that the measured effective BH was 2.1(±0.03) eV which was in good agreement with the theoretical value. Choi et al. [24] investigated carrier transport characteristics and surface states at semipolar (11–22) p-GaN SD with different Schottky metal contacts (Ti, Cu, Ni and Pt). They reported that the slope (S)-parameter ($d\Phi_b/d\Phi_m$) of semipolar p-GaN was estimated to be close to zero, indicates that the surface Fermi level was almost perfectly pinned due to the presence of a high density of deep-level defects. Furthermore, Naganawa et al. [25] studied the electrical characteristics of low-Mg-doped p-GaN Schottky contacts with ten different metal electrodes. They demonstrated that the ten different kind of metal contacts showed high BH ranges from 1.6 to 2.5 eV and low BH ranges from 0.7 to 1.7 eV.

The main objective of our work is to investigate the electrical and structural properties of a fabricated Ti/p-GaN SD at different annealing temperatures. Until now, there is limited research work reported on the electrical and structural characteristics of p-GaN diodes. Jang et al. [23] investigated the temperature-dependent electrical characteristics of the Ti/p-GaN SD and reported that the electrical and carrier transport mechanism of the diode. There are no detailed reports on the electrical, structural and surface morphological characteristics of the Ti/p-GaN SD as a function of annealing temperature. Hence, the present work, investigated the electrical, structural and surface morphological characteristics of the Ti/p-GaN SD as a function of annealing temperature. Moreover, the investigated electrical results are correlated with the interfacial microstructure of the diode at different annealing temperatures. Further, the secondary ion mass spectrometer (SIMS) depth profile and X-ray diffraction (XRD) measurements are used to analyze the interfacial and structural properties of the Ti/p-GaN SD as a function of annealing temperature.

2 Experimental details

1.5-μm-thick Mg-doped p-GaN films grown on c-plane sapphire substrate (0001) by metal organic chemical vapor deposition (MOCVD) technique were used in this work. The carrier concentration of the films was determined to be 1.13×10^{17} cm^{-3}. To remove contaminants, the p-GaN films were subjected to organic solvents like acetone, methanol and ethanol by means of ultrasonic agitation for 5 min in each step and rinsed in deionized (DI) water. Then, the GaN films dipped into boiling aqua regia HNO_3:HCl (1:3) for 10 min to remove the native oxides and then the films were rinsed with DI water. Finally, the films were dried with high-purity nitrogen gas. After cleaning process, Ni (50 nm) and Au (100 nm) films were sequentially deposited on the half portion of the p-GaN surface by electron beam evaporation technique. The films were subsequently subjected to annealing at 650 °C for 3 min in nitrogen atmosphere for forming ohmic contact. Next, 0.7-mm-diameter Schottky dots were formed on the other portion of the p-GaN film by evaporation of titanium (Ti) with 50 nm thick via stainless steel metal mask using a e-beam evaporation technique. All evaporation process was made under a vacuum pressure of 5×10^{-6} mbar. The schematic diagram of the Ti/p-GaN SD is shown in Fig. 1. The Ti/p-GaN SDs were subjected to an annealing at 200, 300 and 400 °C for 1 min in N_2 ambient using a rapid thermal annealing system to evaluate the thermal stability of the SDs. First, to characterize the surface morphology of

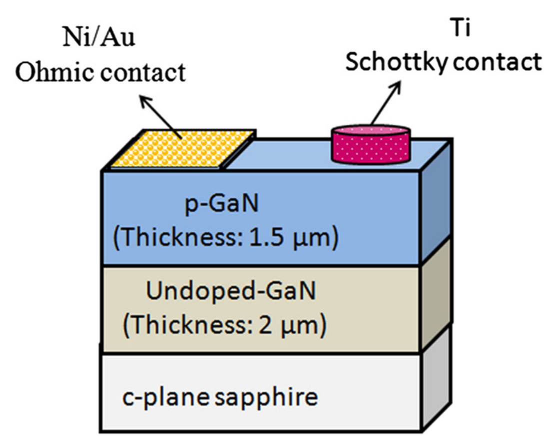

Fig. 1 Ti/p-GaN/Ni/Au Schottky device structure

the Ti/p-GaN SD as a function of annealing, atomic force microscopy (AFM) (Model No: a MOD-1M plus, Make: nano focus; Operating mode; Non contact, tip size <10 nm) was also employed. Using a Keithley source meter (Model No. 2400) and automated deep-level spectrometer (SEMILAB DLS-83), the current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) measurements of the Ti/p-GaN SD were taken at room temperature. SIMS (CAMECA IMS 7f magnetic sector SIMS) depth profile and XRD (X'PERT POWDER, PANALYTICAL using Cu Kα radiation) were employed to examine the intermixing of the metal and GaN layer and to identify the interfacial phases that were formed at different annealing temperatures.

3 Results and discussion

The surface roughness of the metal film on semiconductor plays a vital role in the determination of the electrical properties of devices. In order to evaluate, the surface morphology of the metal film on GaN surface, AFM was performed at different annealing temperatures. The AFM images of the Ti Schottky contact before and after annealing at 400 °C are shown in Fig. 2. The scanned area of the diode is 1 × 1 μm^2. For the as-deposited contact, the surface morphology is reasonably smooth with a root-mean-square (RMS) roughness of 1.124 nm as shown in Fig. 2a. When the contact is annealed at 300 °C, Fig. 2b, the surface morphology of the Ti Schottky contact is slightly decreases with a RMS roughness of 1.778 nm. However, for the contact annealed at 400 °C (Fig. 2c), the surface morphology of the Ti Schottky contact increases with a RMS roughness of 1.204 nm as compared to the 300 °C annealed contacts. These results demonstrated that the surface morphology of Ti Schottky contact did not suffer significantly at elevated temperatures.

The forward and reverse bias ln*I*–*V* characteristics of Ti/p-GaN SD at different annealing temperatures are shown in Fig. 3. The measured reverse leakage current is found to be 1.968×10^{-8} and 1.087×10^{-8} A at 1 V for the as-deposited and 200 °C annealed contacts, respectively. It is found that the reverse leakage current decreases to 8.924×10^{-11} A at 1 V when the contact is annealed at 300 °C. However, it is noted that the reverse leakage current increases to 5.508×10^{-10} A at 1 V upon annealing at 400 °C. Observations reveal that the electrical properties of 300 °C annealed contact improved compared to as-deposited and 400 °C annealed contact. According to TE theory, the SBH and ideality factor of the diode are estimated by the following equation [26, 27]

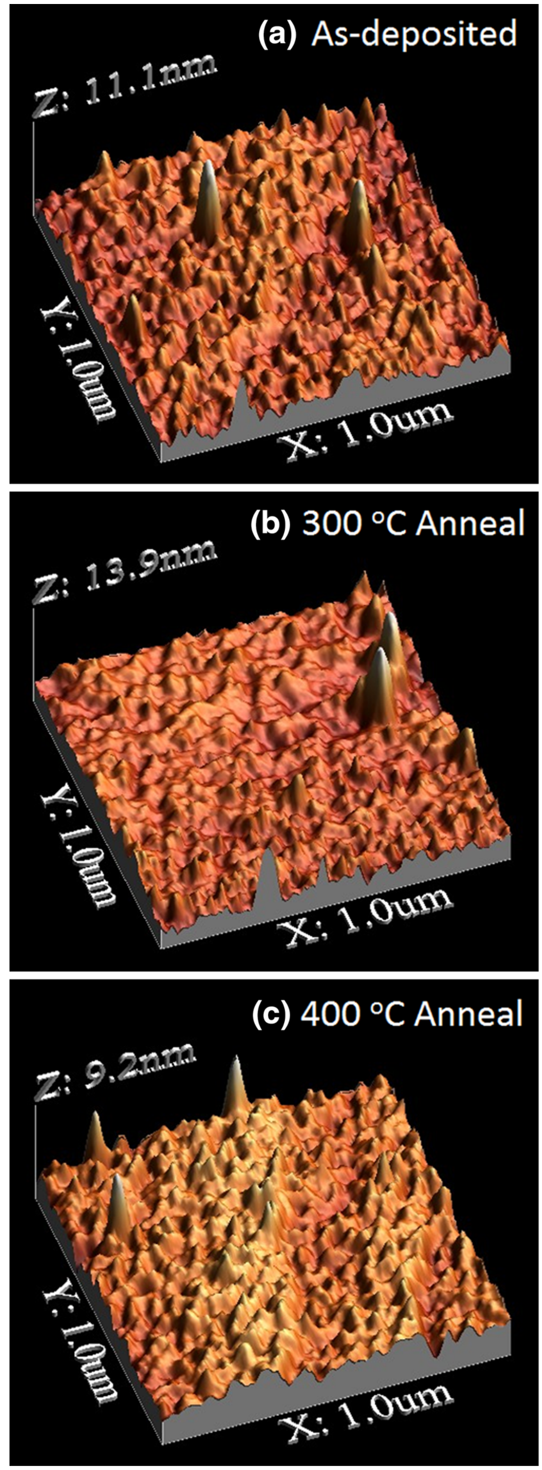

Fig. 2 AFM images of the Ti/p-GaN SD: **a** as-deposited, **b** 300 °C annealed and **c** 400 °C annealed contacts

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nk_BT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{k_BT}\right)\right] \qquad (1)$$

where V is the applied voltage, IR_s is the voltage drop across the R_s of the diode, n is the ideality factor, k_B is the

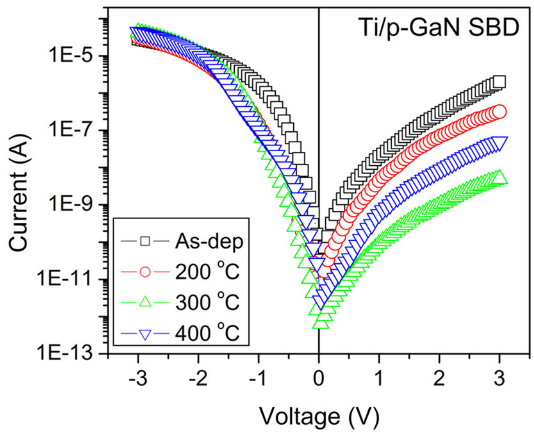

Fig. 3 The current–voltage (I–V) characteristics of the Ti/p-GaN SD as a function of annealing temperature

Boltzmann's constant, T is the absolute temperature in Kelvin, and q is the charge of electron. I_0 is saturation current which is derived from the linear portion intercept of the ln$I$–V plot at $V = 0$ and it is given by

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_b}{k_B T}\right) \quad (2)$$

where A, A^* and Φ_b are the Schottky contact area, effective Richardson constant (72 A cm^{-2} K^{-2}) for p-GaN ($A^* = 4\pi m^* qk^2/h^3$, $m^* = 0.60m_o$) [25] and the zero-bias BH, respectively. The ideality factor n can be obtained from the slope of the linear region of the forward bias $\ln(I) - V$ plot. The calculated ideality factor values of the Ti/p-GaN SD are found to be 1.65 for as-deposited, 1.59 for 200 °C, 1.25 for 300 °C and 1.48 for 400 °C annealed contacts, respectively. These results show that the ideality factor of the p-GaN SD is greater than one for the as-deposited and annealed contacts. This may be due to one or the combination of various effects such as leakage current, series resistance, interface states, tunneling process and non-uniformity distribution of the interfacial charges [28, 29]. Another reason may be the image force lowering of the Schottky barrier at the interface, generation and recombination current within the depletion region [30], defects states in the semiconductor band gap [31] and SBH inhomogeneity [32]. Calculations showed that the SBH of the as-deposited and 200 °C annealed Ti/p-GaN SD are 0.88 and 0.91 eV. However, the SBH increases to 0.98 eV for the contact annealed at 300 °C for 1 min in N_2 ambient. Further, the SBH slightly decreases to 0.94 eV when the contact is annealed at 400 °C. Considering the above results, 300 °C is a suitable annealing temperature for forming an excellent Ti/p-GaN SD lead to maximum BH and ideality factor near to unity compared to the as-deposited and 400 °C annealed contacts. Hence, the optimum annealing temperature for the Ti/p-GaN SD is 300 °C.

Due to the effect of series resistance (R_s) and interface state density (N_{ss}) at the interface, the forward bias I–V characteristics of the Ti/p-GaN SD deviates significantly from the linearity at high voltage region. The R_s is one of the crucial parameters in the downward curvature region of the forward bias ln(I)–V plot. However, the ideality factor n and BH Φ_b are significant in both the linear and downward curvature region of ln(I)–V plot. Therefore, Cheung's functions were employed [33] to evaluate the R_s, n, and Φ_b of the Ti/p-GaN SD in the downward curvature region. The Cheung's functions can be written as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{k_B T}{q}\right) \quad (3)$$

$$H(I) = V - n\left(\frac{k_B T}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (4)$$

and $H(I)$ is given as follows:

$$H(I) = IR_s + n\Phi_b \quad (5)$$

Figure 4a, b shows the plots of dV/d(ln$I$) versus I and $H(I)$ versus I for the Ti/p-GaN SD as a function of annealing temperature. The R_s and n values of the Ti/p-GaN SD are estimated to be 56 kΩ and 1.91 for as-deposited, 34 kΩ and 1.80 for 200 °C, 23 kΩ and 1.58 for 300 °C, and 26 kΩ and 1.82 for 400 °C, respectively, from dV/d(ln$I$) versus I plot (Fig. 4a). Moreover, $H(I)$ versus I plot (Fig. 4b) gives a second determination of series resistance R_s, which can be used to check the consistency of Cheung's approach. From $H(I)$ versus I plot (Fig. 4b), the R_s and Φ_b of the Ti/p-GaN SD are determined to be 76, 51, 33 and 35 kΩ, and 0.90, 0.93, 0.99 and 0.96 eV for as-deposited and 200, 300 and 400 °C annealed contacts, respectively. The BHs Φ_b obtained from $H(I)$ versus I plot are comparable with those obtained from the forward I–V characteristics. However, the series resistance calculated from the dV/d(ln$I$) versus I plots are almost similar to those obtained from $H(I)$ versus I plots, implying their consistency and validity. Moreover, the ideality factors obtained from the dV/d(ln$I$) versus I plot and the forward bias ln(I)–V plot are quite different from each other, which may be due to the existence of series resistance and interface states, and to the voltage drop across the interface layer.

Moreover, Norde [34] has proposed an alternative method to calculate the effective BH and series resistance of the Ti/p-GaN SD. The modified Norde function is given below by

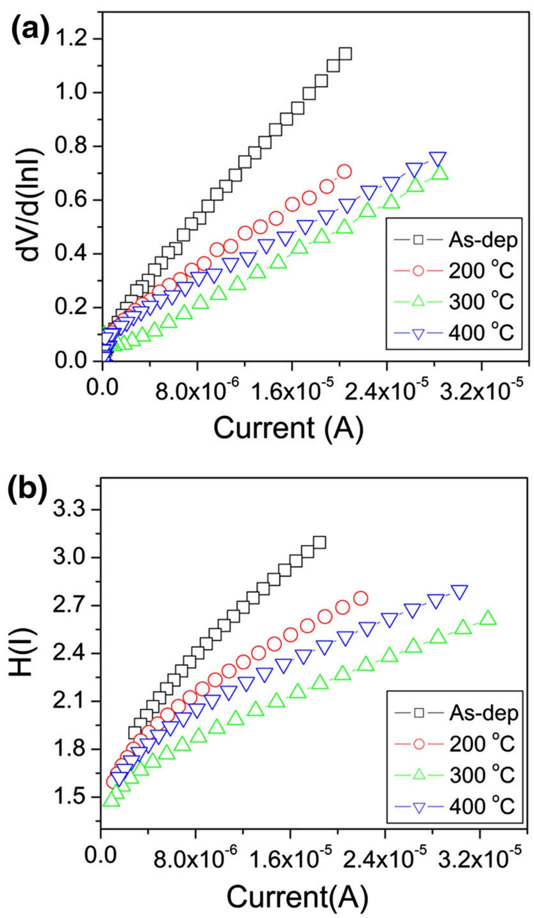

Fig. 4 **a** dV/d(ln$I$) versus I and **b** $H(I)$ versus I plots for the Ti/p-GaN SD as a function of annealing temperature

$$F(V) = \frac{V}{\gamma} - \frac{k_B T}{q} \ln\left[\frac{I(V)}{AA^* T^2}\right] \quad (6)$$

where γ is an (dimensionless) integer greater than the value of the n, and $I(V)$ is the current obtained from the I–V curve. Norde function $F(V)$ versus V is plotted by using Eq. (6) for the Ti/p-GaN SD as a function of annealing temperature shown in Fig. 5. The value of SBH of the diode can be obtained using the following equation

$$\Phi_b = F(V_{min}) + \frac{V_{min}}{2} - \frac{k_B T}{q} \quad (7)$$

here $F(V_{min})$, V_{min} and I_{min} are the minimum value of the $F(V)$, the corresponding voltage and current, respectively. Also, the series resistance R_s of the Ti/p-GaN SD can be determined from the modified Norde function using the following equation

$$R_s = \frac{k_B T(\gamma - n)}{q I_{min}} \quad (8)$$

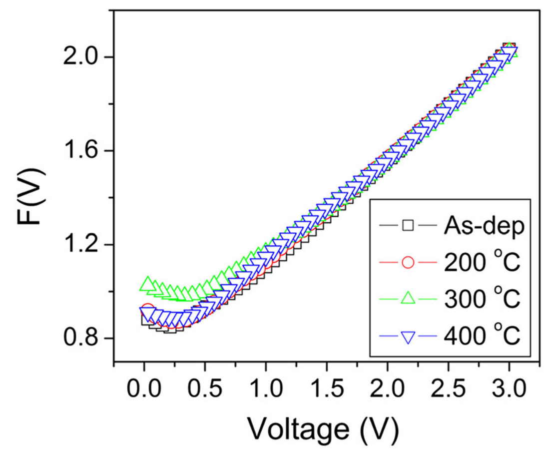

Fig. 5 Norde plot of the Ti/p-GaN SD as a function of annealing temperature

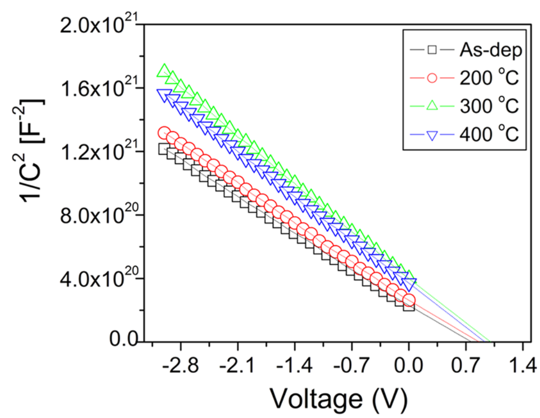

Fig. 6 Plot of $1/C^2 - V$ characteristics of the Ti/p-GaN SD as a function of annealing temperature

The Φ_b and R_s values of the Ti/p-GaN SD are determined as 0.93 eV, 2.4 MΩ for as-deposited, 0.95 eV, 111 MΩ for 200 °C, 1.11 eV, 175 MΩ for 300 °C, and 0.98 eV, 16 MΩ for 400 °C, respectively. There is quite a difference between the series resistance obtained from the Cheung's and Norde methods. This may be due to the Cheung's method is only applied for the non-linear region, while Norde method is applied for the entire forward bias ln(I)–V plot of the diode. The large values of R_s obtained from the Norde method may be attributed to decrease in the exponentially increasing rate in current due to space charge injection between metal–semiconductor at higher forward bias voltage. Also, the higher value of R_s is attributed to non-suitability of the Norde model for high ideality factor ($n > 1$) of the rectifying junctions.

The C–V characteristics of the Ti/p-GaN SD are measured in the dark at a frequency of 1 MHz. Figure 6 shows a plot of $1/C^2$ as a function of bias voltage for the as-deposited and annealed at 200, 300 and 400 °C. In SD, the depletion capacitance can be expressed as [27]

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_s q N_d A^2}\right)\left(V_{bi} - \frac{k_B T}{q} - V\right) \quad (9)$$

where ε_s is the permittivity of the semiconductor ($\varepsilon_{GaN} = 9.5\varepsilon_o$), A is the diode area, and N_a is the carrier concentration. The plot of $1/C^2$ versus V gives V_o (x-intercept at V_o), V_o is related to the built-in-potential V_{bi} given by $V_{bi} = V_o + kT/q$, T is the absolute temperature. The BH (Φ_b) can be deduced by the relation $\Phi_{b(C-V)} = V_{bi} + V_n$, where V_n can be determined from the equation $V_n = (kT/q)\ \ln(N_v/N_A)$, where N_v is the density of effective states in the valence band of p-GaN given by $N_v = 2\left(2\pi m^* kT/h^2\right)^{3/2}$, where $m^* = 0.60 m_o$ [21] and its value is $N_v = 1.17 \times 10^{19}$ cm^{-3} at room temperature. The extracted SBHs of Ti/p-GaN SD from C–V plots of the as-deposited and annealed contacts at 200, 300 and 400 °C are 1.02, 1.11, 1.26 and 1.17 eV, respectively. The calculated electrical parameters of the Ti/p-GaN SD at different annealing temperatures are summarized in Table 1. It is seen from Table 1 that the obtained SBH values from I–V method are lower than those obtained from C^{-2}-V curves. This discrepancy between the SBHs obtained from $\Phi_{b(C-V)}$ and $\Phi_{b(I-V)}$ is mainly due to the barrier inhomogeneity in the metal–semiconductor interface [35, 36]. Specifically, the C–V measurement averages over the entire area plus measures to describe Schottky barrier diode since the capacitance is insensitive to potential fluctuations on a length scale of less than space charge width. But the current across an interface with several spatial fluctuations depends exponentially on BH and the capability of a current to flow preferentially through barrier minima. Hence, the SBH extracted from I–V measurements are lower than those extracted from C–V measurements [37, 38]. Another reason might be partly due to the image force barrier lowering, quantum mechanical tunneling and edge leakage current effects [27]. Fontaine et al. [39] have demonstrated that the surface damage at the metal–semiconductor interface affects the I–V measurements since defects may act as recombination centers for trap-assisted tunneling current. Also, Geng et al. [40] have revealed that the pinholes come from the extended coreless dislocations, which originate in the GaN buffer layer, resulting in a high leakage current and low BH.

Table 1 The calculated barrier height, ideality factor, series resistance and interface state density of the Ti/p-GaN SD diode by I–V and C–V methods at different annealing temperatures

Parameter	As-dep.	200 °C	300 °C	400 °C
From I–V characteristics				
Barrier height, Φ_b (eV)	0.88	0.91	0.98	0.94
Ideality factor, n	1.65	1.59	1.25	1.48
From Cheung's method dV/d(ln$I$) versus I				
Series resistance, R_s (kΩ)	56	34	23	26
Ideality factor, n	1.91	1.80	1.58	1.82
$H(I)$ versus I				
Series resistance, R_s (kΩ)	76	51	33	35
Barrier height, Φ_b (eV)	0.90	0.93	0.99	0.96
From Norde's method				
Barrier height, Φ_b (eV)	0.93	0.95	1.11	0.98
Series resistance, R_s (MΩ)	2.4	111	175	16
From C–V characteristics				
Barrier height, Φ_b (eV)	1.02	1.11	1.26	1.17
Interface state density, N_{ss} ($\times 10^{12}$ cm^{-2} eV^{-1})	1.617	1.413	1.014	1.457

The interface states play a vital role on the electrical characteristics of the SD. Card and Rhoderick [41] has proposed that the ideality factor n becomes greater than unity when metal–semiconductor diode having interface states is in equilibrium with the semiconductor. The energy distribution curves of the interface states (N_{ss}) in equilibrium with the semiconductor can be deduced by taking the voltage-dependent ideality factor and effective BH from the forward I–V data. Then, the N_{ss} is described as

$$N_{SS} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \quad (10)$$

where δ is the thickness of the interfacial layer, $\varepsilon_i = 3.8\varepsilon_o$ and $\varepsilon_s = 9.5\varepsilon_o$ are the permittivity of the interfacial layer and semiconductor, N_{ss} is the interface state density, and W_D is the width of the space charge region. Using the equation $n(V) = V/(kT/q)\ln(I/I_s)$ [38], the voltage-dependent ideality factor is determined. Moreover, for p-type semiconductor, the energy of interface states E_{ss} with respect to top of the valance band E_v at the surface of the semiconductor is expressed as [38, 42]

$$E_{ss} - E_v = q(\Phi_e - V) \quad (11)$$

here Φ_e is the effective BH and it is given by [43]

$$\Phi_e = \Phi_b + \beta V \quad (12)$$

were

$$\beta = 1 - \frac{1}{n(V)} \quad (13)$$

The interface states density (N_{ss}) of the Ti/p-GaN SD can be determined at each annealing temperature using Eqs. (10)–(13) along with the forward bias I–V characteristics. Figure 7 represents the interface state density (N_{ss}) versus energy distribution plots of the Ti/p-GaN SD at different annealing temperatures. Clearly, it can be observed from Fig. 7, the N_{ss} value decreases with an

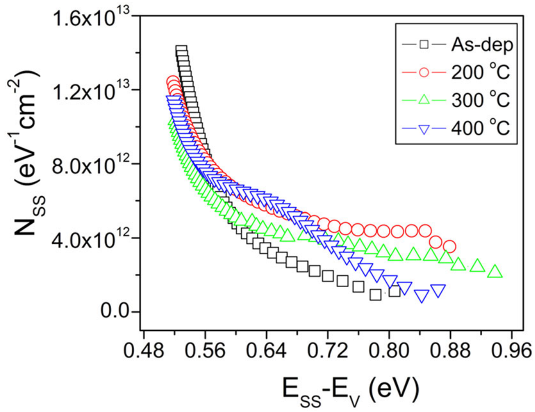

Fig. 7 Density of interface states N_{ss} as a function of $E_{ss} - E_v$ for the Ti/p-GaN SD as a function of annealing temperature

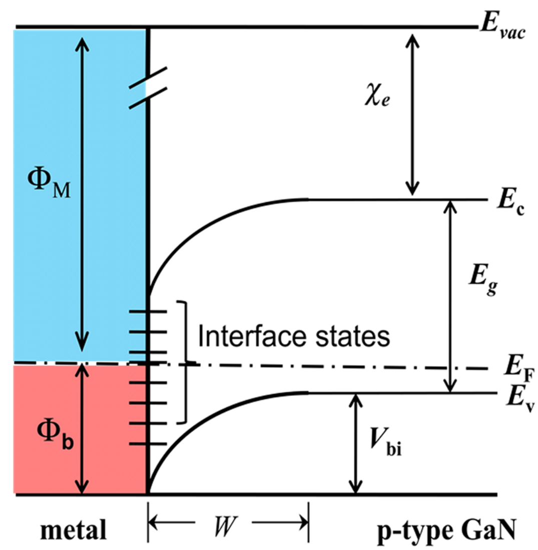

Fig. 8 The energy band diagram of Ti/p-GaN Schottky diode with interface states: where Φ_b is the Schottky barrier height, Φ_m is the metal work function, χ_e is the electron affinity of semiconductor, E_g is the energy gap, V_{bi} is the built-in potential and W is the depletion width

increase in the $E_{ss} - E_v$ value, and increase in N_{ss} from mid gap toward the top of the valance band. The estimated N_{ss} of the Ti/p-GaN SD are found to be 1.617×10^{12} eV^{-1} cm^{-2} for as-deposited, 1.413×10^{12} eV^{-1} cm^{-2} for 200 °C, 1.014×10^{12} eV^{-1} cm^{-2} for 300 °C and 1.457×10^{12} eV^{-1} cm^{-2} for 400 °C annealed contacts, respectively. It is noted that the N_{ss} decreases for the contact annealed at 300 °C and then slightly increases upon annealing at 400 °C. This is probably due to the variation of the series resistance (R_s) upon annealing temperature and the change in the charge of the interface states. Thus the interface state energy distribution due to the potential drop across the interfacial layer varies with bias. It alters the diffusion potential and therefore, the depletion capacitance [27, 28, 44]. Based on the results, the N_{ss} and R_s can affect the electrical characteristics of the Ti/p-GaN SD. The energy-level band diagram of the Ti/p-GaN junction with an interface states is shown in Fig. 8.

The SIMS and XRD studies were carried out to correlate the electrical properties of the Ti/p-GaN SD with the microstructural properties at different annealing temperatures. The SIMS depth profiles of Ti/p-GaN SD at different annealing temperatures are shown in Fig. 9. The SIMS depth profile of as-deposited Ti/p-GaN SD reveals that there is an interface region between the Ti and the p-GaN layers (Fig. 9a). This indicates that the possible reaction of Ti with p-GaN layer. For the contact annealed at 300 °C (Fig. 9b), there is some amount of N is out-diffused into Ti layer, which indicates the possibility of the reaction between Ti and N layers. As a result, the Ti–N interfacial phases are formed at the interface. The SIMS depth profile of 400 °C Ti/p-GaN SD shows (Fig. 9c) that there is some amount of Ga out-diffusion into Ti layer, resulting in the formation of Ga–Ti interfacial phases at the interface, as will be confirmed by XRD measurements. Besides, a small amount of oxygen is observed at the interface for all contacts, which may be partially originates from the p-GaN substrate surface and/or during metal deposition. It is worth noting that the Ti layer remains stable even after annealing at 400 °C.

Further, in order to examine the interfacial products that occurred at the interface of the Ti and the p-GaN at different annealing temperatures, XRD measurements were employed. The XRD plots of the Ti/p-GaN SD before and after annealing at 400 °C for 1 min in nitrogen ambient are shown in Fig. 10. The XRD plot of the as-deposited contact is shown in Fig. 10a. In addition to the characteristics peaks of GaN (002) (004), Ti (102), there are additional peaks observed, which are identified as $Ti_3N_{1.29}$ (006), $TiN_{0.26}$ (002), $Ti_4N_{2.33}$ (107) (1010) (116), TiN (220) and GaTi3 (110). When the contact is annealed at 300 °C, (Fig. 10b), new additional peaks are noted, which indicate the formation of new interfacial phases at the Ti and GaN layers compared to the as-deposited Ti/p-GaN SD. These peaks are identified as Ti_2N (101) (200) (213) (002) and $Ti_4N_{2.33}$ (009). Upon annealing temperature at 400 °C, (Fig. 10c), extra peaks are observed in addition to the peaks noted in the as-deposited and 300 °C annealed contact, which are identified as Ga_3Ti_2 (200), Ga_5Ti_3 (211), Ga_3 Ti_5 (212) and Ga_4 Ti_5(222).

According to the above experimental results presented, the variation in the SBH upon annealing could be explained as follows. The electrical measurements revealed that the SBH is increased when the contact is annealed at 300 °C and then slightly decreased after annealing at 400 °C. This could be attributed to the interfacial reaction between metal and GaN, and their alloys which extend to GaN films. The

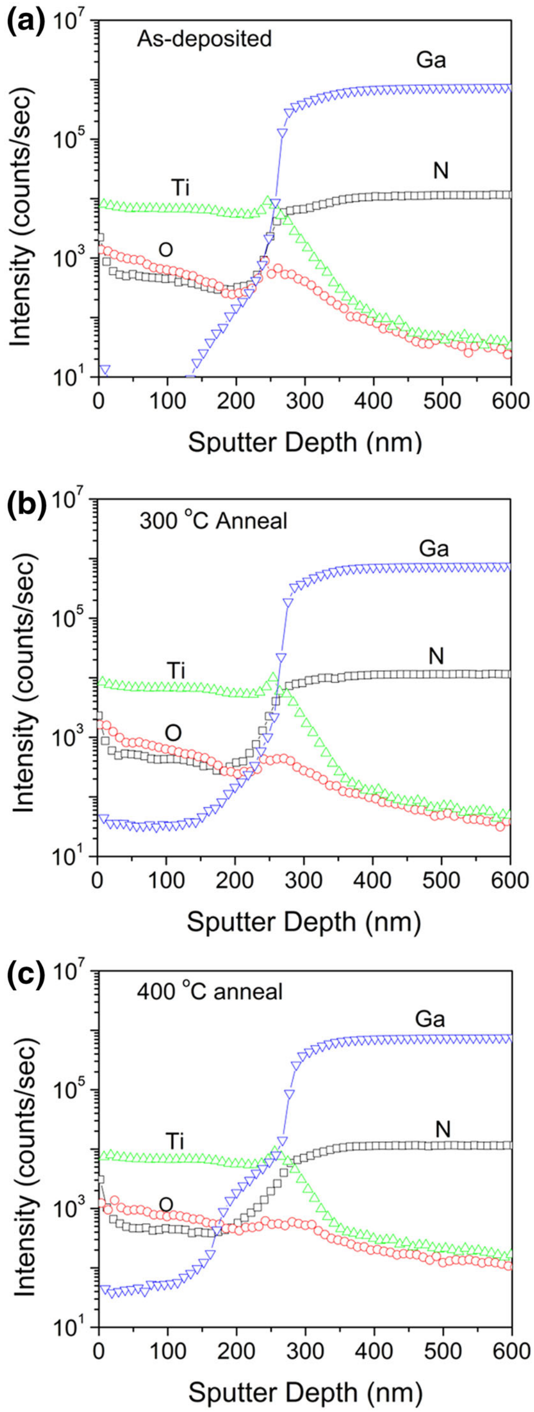

Fig. 9 SIMS depth profiles of the Ti/p-GaN SD: **a** as-deposited, **b** 300 °C annealed and **c** 400 °C annealed contacts

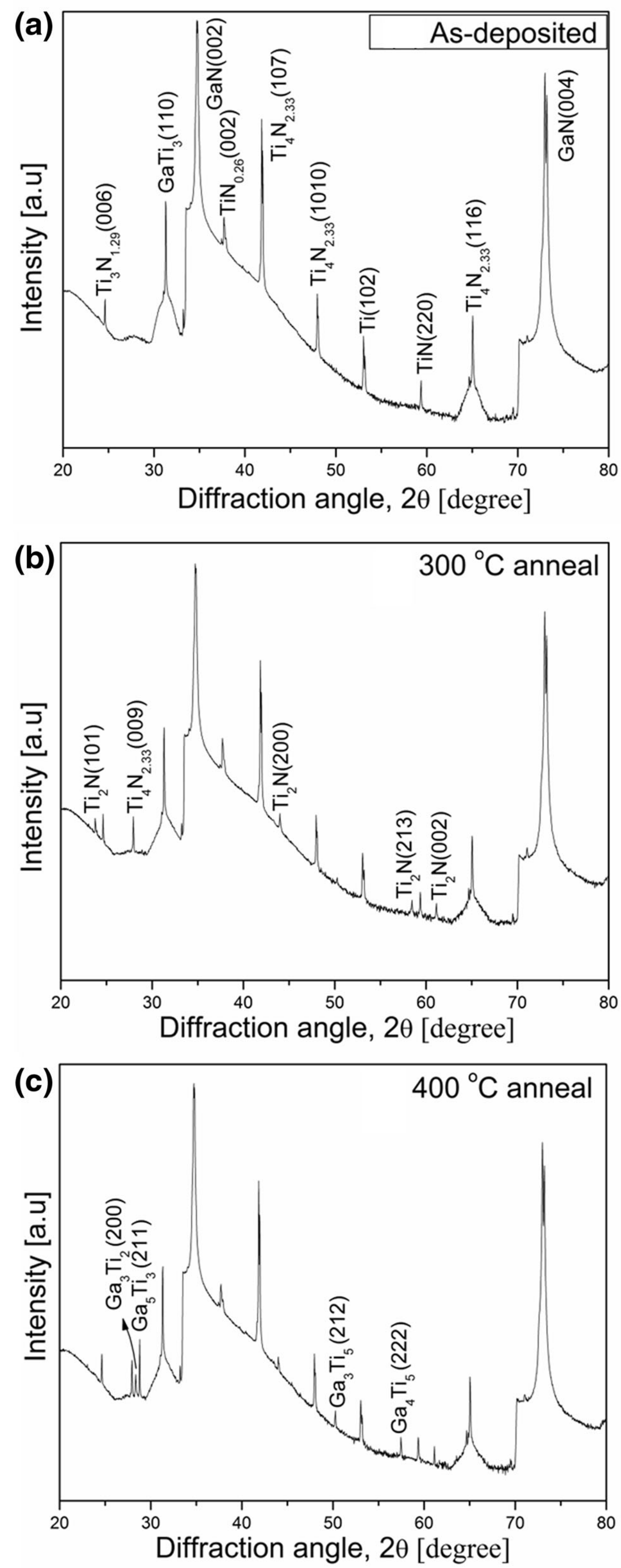

Fig. 10 XRD plot of the Ti/p-GaN SD: **a** as-deposited, **b** 300 °C annealed and **c** 400 °C annealed samples

SIMS and XRD results revealed that the out-diffusion of the N from the p-GaN film into Ti layer, which indicates the formation of nitride phases (Ti–N) at the interface (as shown by XRD results Fig. 10a, b). As a result, there is an accumulation of N vacancies at the region near the surface of the p-GaN layer. Thus, the increase in positive charges at the interface probably arise due to hole traps localized at the GaN surface. This causes an increase in the SBH of Ti/p-GaN SD upon annealing temperature at 300 °C. In p-type semiconductor substrate, Monch [45] has demonstrated that positively charged interface defects will increase the SBH, while negatively charged interface defects will decrease the SBH. Therefore, the charge on the defect states must balance in the depletion layer, which means that only donor-like states can be operative in the p-type material for increase in the SBH [46]. Moreover, the decrease in the SBH of Ti/p-GaN SD after annealing at 400 °C could be attributed to the reaction of Ti with Ga atoms, resulting in the formation of Ga–Ti interfacial phases at the interface (as evidence from XRD results Fig. 10c). The formation of Ga-phases may create gallium vacancies in GaN near junction. These vacancies act as acceptor-like states, thus reducing the SBH upon annealing temperature. Several researchers [47–52] had reported that the SBH would be influenced by the interfacial alloys products at metal–GaN interface.

4 Conclusions

Using *I–V*, *C–V*, SIMS, XRD and AFM techniques, the electrical, structural and morphological properties of a fabricated Ti/p-GaN SD have been investigated at different annealing temperatures. The surface morphology of the Ti/p-GaN SD is considerably smooth at various annealing temperatures. The SBH of as-deposited and annealed at 200 °C Ti/p-GaN SDs are found to be 0.88 eV (*I–V*)/1.02 eV (*C–V*) and 0.91 eV (*I–V*)/1.11 eV (*C–V*). However, the SBH increases to 0.98 eV (*I–V*)/1.26 eV (*C–V*) for the Ti/p-GaN SD annealed at 300 °C for 1 min in nitrogen ambient. Further, the SBH slightly decreases to 0.94 eV (*I–V*)/1.17 eV (*C–V*) after annealing at 400 °C. Besides, the series resistance, SBH and ideality factor of the Ti/p-GaN SD are also estimated by Norde method and Cheung's functions at various annealing temperatures. The series resistances calculated from $dV/d(\ln I)$–I plot are comparable with those calculated from $H(I)$–I plot. The discrepancy between the SBHs obtained by *I–V* and *C–V* methods are described and discussed. Moreover, the interface state density of the Ti/p-GaN SD decreases upon annealing at 300 °C (1.014×10^{12} eV^{-1} cm^{-2}) and then slightly increases after annealing at 400 °C (1.457×10^{12} eV^{-1} cm^{-2}). Based on the above results, the series resistance and interface state density play a vital role on the electrical properties of the Ti/p-GaN SD. The SIMS and XRD results revealed that the formation of Ti–N interfacial phases at the interface may be the cause for increase in the SBH upon annealing at 300 °C. The decrease in the SBH of the 400 °C annealed contacts may be due to the formation of Ga–Ti interfacial phases at the interface. Experimental results showed that the Ti Schottky contact is promising electrode for the fabrication of high-power device applications.

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