Appl. Phys. A (2015) 119:133–139
DOI 10.1007/s00339-015-9028-0

Applied Physics A
Materials Science & Processing

Pd/In/Ni/Au contact to N-polar n-type GaN fabricated by laser lift-off

J. Ma · Z. Z. Chen · S. Jiang · Q. Q. Jiao · J. Z. Li · S. X. Jiang · Y. L. Feng · T. J. Yu · G. Y. Zhang

Received: 2 September 2014 / Accepted: 29 January 2015 / Published online: 6 February 2015
© Springer-Verlag Berlin Heidelberg 2015

Abstract Pd/In/Ni/Au contacts to N-polar n-GaN were investigated to obtain low contact resistance and high thermal stability contacts. Two-step thermal annealing method was developed to form the PdIn and InGaN alloys successively, which were clarified by Auger electron spectroscopy and transmission electron microscopy measurements. The lowest specific contact resistivity was achieved as 5.4×10^{-5} Ω cm^2 when the sample was annealed under 250 °C for 600 s and 500 °C for 30 s in N_2 ambient in sequence. It was observed that Pd/In fusion was occurred at the first annealing step. The PdIn alloy can well act as the blocking layer to prevent the outdiffusion of Ga atoms from n-GaN and low work function material as well. The second annealing step led to some content InGaN formation. PdIn contact to InGaN may get a small Schottky barrier height and some effective electron accumulation at the GaN/InGaN interface, which decreases the specific contact resistivity of Pd/In/Ni/Au to N-polar n-GaN.

1 Introduction

Vertical structure LED (VSLED) is of great importance because of the excellent performances on current spreading and heat dissipation when the LED epilayer is transferred to thermal and electrical conductive substrate like silicon [1, 2]. N-polar n-GaN will be exposed when the sapphire substrate is removed. The earlier reports showed that ohmic contacts to N-polar n-type GaN were difficult to make because of the inverse polarization direction compared to Ga-polar GaN [3, 4]. Although the polarization induced band bending for N-face GaN is smaller than that for its opposite [5, 6], the Al-based contacts to N-polar n-type GaN are suffered from the electron depletion at the interface of AlN/GaN and the outdiffusion of Ga atoms from the N-polar surface [3, 4, 7, 8]. Many efforts are paid to the blocking layers between the metals and the nitride for Ga outdiffusion and/or AlN formation, such as Pd [7], TiN [8], AlGa [9], W [10], Cr [11], AlN [12], Ga residual [13], Mo [14], Ta [15], and so on. The blocking layers are effective when the thermal annealing temperature is below 300 °C. Some of them can be sustained above 300 °C, but the contact resistance cannot be improved further. It is notable that AlN layer formation may take a role in the thermal stability under high temperature [7, 12], while many researchers believe it negative to form excellent ohmic contact to N-polar n-GaN. The ohmic contact formation may be not due to AlN layer, but due to the heavy doping of AlN [12] or the intermetallic reactions [7]. Al-based contact seems hard to obtain low resistance and high thermal stability simultaneously yet.

On the other hand, In-based contacts are supposed to well resolve the electron depletion at the interface [16]. Because of the large piezoelectric polarization for strained InN, the carriers in GaN will accumulate at the interface of N-polar InN/GaN. Moreover, Walle et al. [17] predicted that the Fermi level of InN was located in the conduction band, and the intrinsic electron concentration in InN layer was very high. However, indium is an active metal with low melting point, and it is not stable under high annealing temperature. In-based contact seems to be poor in the thermal stability. Wong et al. [1] successfully used PdIn alloy as wafer bonding layer for laser lift-off process. This

J. Ma (✉) · Z. Z. Chen · S. Jiang · Q. Q. Jiao · J. Z. Li · S. X. Jiang · Y. L. Feng · T. J. Yu · G. Y. Zhang
State Key Laboratory for Artificial Microstructures and Mesoscopic Physics, School of Physics, Peking University, Beijing 100871, China
e-mail: mjphy@pku.edu.cn

bonding layer has low resistance to shear stress at bonding temperature below 200 °C. After bonding, high melting point alloys, PdIn or $PdIn_3$, are formed, with the melting points as 709 and 664 °C, respectively. Venugopalan et al. [18] found that the lower work function of indium might lower the work function of the PdIn phase, and PdIn contacts were more stable than Pd-only contacts to n-GaN. According to the binary phase diagram [19], Pd is likely reactive to Ga to form nine different gallides. PdIn scheme with these advantages looks likely to be thermal stable and low resistance ohmic contacts to N-polar n-GaN. However, few works were reported about the PdIn ohmic contact to N-polar GaN.

In this work, we have achieved low resistance ohmic contact of Pd/In/Ni/Au to N-polar n-GaN by two-step thermal annealing. It was found that the PdIn alloy was formed after annealing at 200–300 °C for the first step. In(Ga)N layer would be formed at the interface of metal/GaN under successively higher temperature annealing. The circular transferring line method (CTLM), Auger electron spectroscopy (AES) and transmission electron microscopy (TEM) measurements were performed to investigate the formation mechanism of PdIn ohmic contact to N-polar n-GaN.

2 Experiment

N-type GaN wafer was grown on (0001) sapphire substrate by metal organic chemical vapor deposition (MOCVD). The wafer thickness is about 7 μm, and the doping concentration was about 10^{18} cm^{-3}. The wafer was bonded to Si substrate using Au–Au bonding technique. Laser lift-off (LLO) was performed using YAG:Nd laser ($\lambda = 355$ nm) to remove the sapphire substrate. Then, the wafer was dipped into HCl solution, and Ga particulate residual was removed from the exposure N-polar GaN surface. Photolithography was performed to prepare the CTLM pattern, the inner diameter of the circular ring is 100 μm, and the outside increases from 110 μm to 160 μm, with the spacing increment of 10 μm. Then, Pd/In/Ni/Au (20/60/50/200 nm) was deposited on N-polar GaN by electron beam evaporator. The contacts with CTLM pattern were obtained by lift-off process. Then, the samples were annealed in N_2 ambient using a two-step annealing strategy: the first step with a low temperature about 200–300 °C for a long time about 600 s, while the second step with a higher temperature about 500 °C and shorter time about 30 s. Then, electrical measurements were performed at room temperature using a HP4155 semiconductor parameter analyzer. Thus, current vs voltage (*I–V*) curves between the contacts on two side of the ring were measured, and the specific contact resistivities were obtained by CTLM for each sample. Auger electron spectroscopy (AES) and transmission electron microscopy (TEM) measurements were also performed on Pd/In/Ni/Au/N-polar GaN samples by nano-scanning Auger system (PHI-700) and F30 system, respectively. Energy-dispersive X-ray spectroscopy (EDS) was measured in F30 system too, which could obtain the composition distribution in microstructures.

3 Results and discussion

Figure 1a shows the typical *I–V* curves of Pd/In/Ni/Au contacts to N-polar n-GaN before and after thermal annealing under different conditions. The first steps were performed under 250 °C for 600 s, and the second steps were under 300, 400, 450, 500, and 600 °C for 30 s, respectively. Sample annealed at 250 °C for 600 s without the second step was also performed. The as-deposited sample shows rectification characteristics because of the work function of Pd is as high as 5.1 eV [20]. After first annealing step at 250 °C for 600 s, the PdIn alloy starts to be formed and lower work function of PdIn leads to the smaller Schottky barrier height (SBH) [18], and thus, the *I–V* curve shows less rectified. When the sample was annealed under 300 °C, the contact became better but kept to be rectification. The contact became ohmic when the annealing temperature was above 400 °C. The higher annealing temperature, the steeper the *I–V* curves' slopes are until 500 °C. When the annealing temperature is 600 °C, the *I–V* curve slopes becomes slower. The resistivities, ρ_c, of samples shown in Fig. 1a are shown in Fig. 1b. It mainly shows the impact of the second step on ρ_c. The lowest ρ_c approaches to 5.4×10^{-5} Ω cm^2 after 500 °C annealing. The ohmic contacts formation may be due to the formation PdIn and In(Ga)N, which will be discussed later. The annealing temperature should be below 600 °C because the n-GaN wafer suffered some cracking observed in optical microscope. The large uncertainties shown in the Fig. 1b may be due to Schottky junctions with nonuniform resistance of the metal–semiconductor–metal (MSM) and the cracking for low temperature below 300 and 600 °C thermal annealing, respectively.

If the sample is annealed without the first step and go through high temperature annealing directly, the sample is risked to heat instability because the melting point of indium is about 160 °C, and thus, metals upon indium would be "lift-off" when the indium layer melts quickly [16]. In this work, some samples were first annealed at 400 °C for 30 s, directly by one step. Most areas of the samples suffer from rough surface with crack, while only a few areas showed smooth surface and good ohmic contact, low ρ_c could be achieved in these few areas. The same results to samples annealed at 450 or 500 °C by one step.

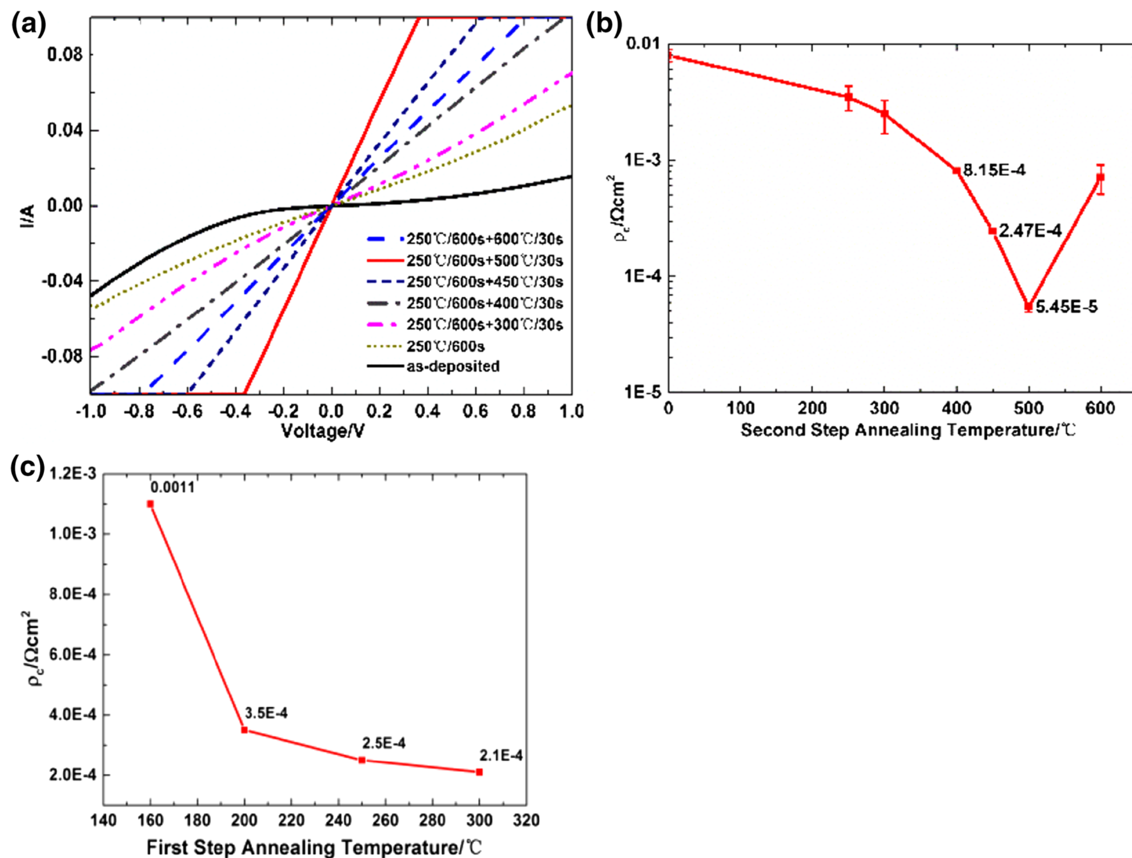

Fig. 1 **a** *I–V* curves of Pd/In/Ni/Au contacts to N-polar n-GaN under different annealing conditions. **b** ρ_c of samples in (**a**). **c** ρ_c of samples of which the first steps are 160, 200, 250, 300 °C for 600 s, respectively, and the second steps are all at 450 °C for 30 s

Two-step thermal annealing processes are usually used to avoid the instability of low melting point metal [21]. The first step annealing with low temperature but long time was proposed to form the alloy of Pd and In, while PdIn alloy is of high melting point [1]. The first step was thermal annealing at 160, 200, 250, and 300 °C for 600 s, respectively, while the second step was annealing kept at 450 °C for 30 s. The results are shown in Fig. 1c. It clearly shows that ρ_c decreases with the annealing temperature of the first step increasing, and it tends to be saturated when the temperature reaches about 300 °C. However, the first annealing temperature could not be higher than 300 °C because the morphologies are degraded on the contact surfaces. Wong et al. found that the Pd/In bilayer was melted to form PdIn alloy at or below 200 °C, while the PdIn's melting point is as high as above 600 °C [1]. With the annealing temperature increasing, the formation of PdIn alloy is sufficient, and then, the SBH to n-GaN is lower and more Ga outdiffusion is prevented. These behaviors result in the low contact resistances.

AES depth profiles of Pd/In/Ni/Au contacts to N-polar n-GaN are shown in Fig. 2. The samples include as-deposited, thermal annealing at 250 °C/600 s, 250 °C/600 s + 400 °C/30 s and 250 °C/600 s + 500 °C/30 s, respectively, corresponding to Fig. 2a–d. Figure 2a shows the individual metal layers in the as-deposited samples. The overlap between the neighbor layers are due to the Ar^+ sputtering processes on the metal grain boundaries and/or inhomogeneous metal layer. The Ni profiles are abnormally in a long range because sputtered Ni is likely re-deposited on the sample when the contact is etched, which is also named as "preferential sputtering" [22]. It is certain that n-GaN is mostly contacted to Pd layer, so the *I–V* curve for the as-deposited sample is rectified. When the annealing time reaches 250 °C,Fig. 2b shows more Pd and In overlap and PdIn alloy formation to a certain content. That should contribute to the improvement of the *I–V* curve at 250 °C, as shown in Fig. 1a. It indicates that the SBH decreases as the PdIn formation. The complete overlap of the profiles of Pd and In is shown in Fig. 2c as the annealing temperature reaches 400 °C. This means Pd/In mixed thoroughly, and most of them may form PdIn alloys. When PdIn contacts to the majority of n-GaN, ohmic contact can be achieved due to the lower and thinner SBH, as shown in Fig. 1a. When the temperature increases to 500 °C, some indium may enter into the n-GaN internal and the metal demarcation

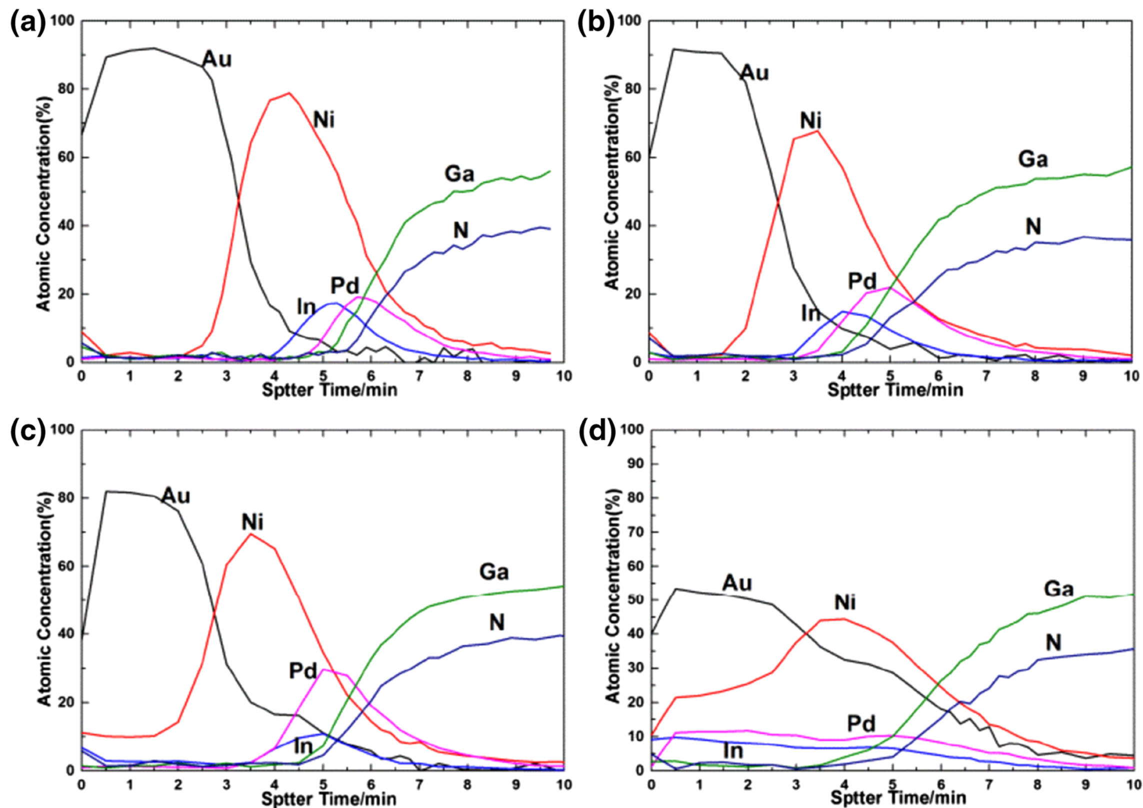

Fig. 2 AES depth profiles of Pd/In/Ni/Au contacts to N-polar n-GaN with different annealing conditions: **a** as-deposited, **b** 250 °C/600 s, **c** 250 °C/600 s + 400 °C/30 s, **d** 250 °C/600 s + 500 °C/30 s

was disappeared, as shown in Fig. 2d. The lowest ρ_c are obtained which may be due to the InGaN layer formation. The mechanism will be discussed in the following. On the other hand, the outdiffusion of the all the metals maybe a problem, because a lot of high work function metals contact to N-polar n-GaN would degrade the contact characteristics. The upper Ni blocking layer should be substituted to more stable metals, such as W [10] and Mo [14].

The microstructures are also studied by cross-sectional TEM and EDS at the interface of metal/n-GaN under different annealing conditions. Cross-sectional TEM image of as-deposited sample is shown in Fig. 3a, and four distinguishable layers are observed as Pd, In, Ni, Au, respectively. According to the higher density of metal Pd, the mole ratio of Pd/In is about 0.6. The thicknesses of metals in Fig. 3a are basically same as the evaporator setting values. When the samples were annealed under the condition of 250 °C/600 s + 400 °C/30 s, as shown in Fig. 3b, Pd/In bilayer becomes a single layer of PdIn alloy. The boundaries of Au/Ni, Ni/PdIn are both distinguishable. It indicates that the Ni prevents the Au diffusion well. EDS measurement shows that there are negligible metals penetrated into n-GaN. A bright boundary at interface of PdIn/n-GaN may be due to the TEM specimen preparing. These results agree with the AES and *I–V* measurements above. Figure 3c shows the TEM images of the sample annealed under the condition of 250 °C/600 s + 500 °C/30 s. No boundaries are observed along the vertical direction to the sample surface in the metals. The contrast was changed in the region of 10 nm near the metal/GaN interface in n-GaN epilayer. The darker fluctuation interfaces (red marked) mean some reactions occurred between semiconductor and metal by indium and/or other metals penetrated into the n-GaN. Figure 4 shows high angle annular dark-field (HAADF) TEM image and two EDS profiles at different positions of the annealed sample same as that in Fig. 3c. HAADF image in Fig. 4a shows the contrary contrast comparing to the bright-field TEM image in Fig. 3c. It also shows that there are no obvious boundaries in the metal. There are two contrasts at the interface in n-GaN side. One is slight white, and the other is gray similar to the n-GaN internal. Two red lines (Line 1 and Line 2) penetrate from metal into the two regions, respectively. EDS profiles scanning along the red Line 1 and Line 2 are shown in Fig. 4b, c. EDS profile along Line 1 shows that some indium penetrates into n-GaN, while Au, Pd interrupted at the interface in the slight white area. The indium content in this region is about 10 %, and the width is about 40 nm. EDS profile along Line 2 shows no obvious metal including indium penetrated into n-GaN in the gray area. The

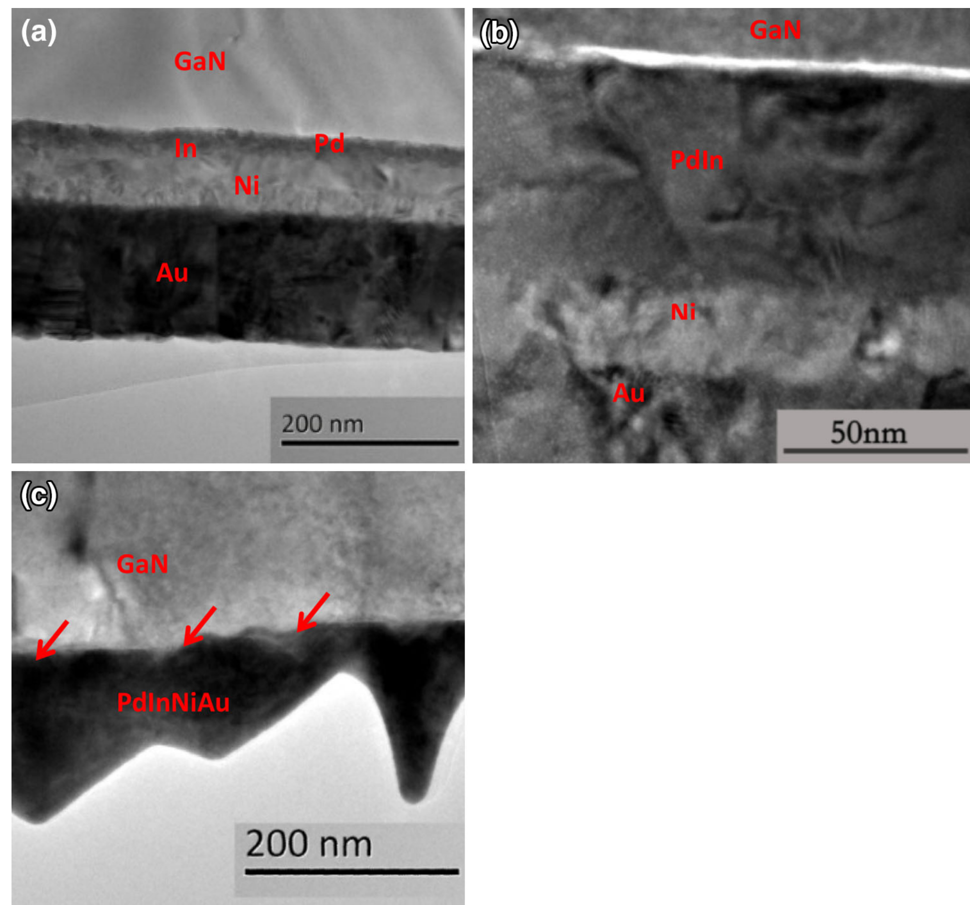

Fig. 3 Cross-sectional TEM images of the samples under different annealing conditions: **a** as-deposited, **b** 250 °C/600 s + 400 °C/30 s, **c** 250 °C/600 s + 500 °C/30 s

indium diffusion into n-GaN was confirmed and InGaN could be regarded to form in partial region at the metal/GaN interface. InGaN formation may play an important role in the reduction of Pd/In/Ni/Au contact resistance to N-polar GaN. On the other hand, it is notable that there are no Ga outdiffusion into metals even the annealing temperature is high as 500 °C. PdIn alloy can effectively act as blocking layer, which is also another advantage for ohmic contact formation.

According to the above results, the formation of ohmic contact of Pd/In/Ni/Au to N-polar n-GaN can be explained by the band diagram, as shown in Fig. 5. When the metal is deposited to N-polar GaN, it shows Schottky contact because the work function of Pd is high as 5.1 eV, which is much more than that of n-GaN as 4.2 eV. Pd/GaN structure leads to high and wide of Schottky barrier at the interface, as shown in Fig. 5a, which causes the rectification characteristics and high contact resistance. When it is annealed under 200–300 °C, PdIn alloy starts to form. The work function of In is about 4.1 eV, so linear interpolations of the alloys of PdIn and $PdIn_3$ are 4.6 and 4.35 eV, respectively. The SBH of the PdIn contact to GaN is decreased. However, certain content Pd remains contacting to n-GaN, so the contact characteristics is improved but keeps to be Schottky contact. The contact becomes ohmic until the sample is annealed under 400 °C. Both AES and TEM results show Pd/In bilayer becomes a single layer. It should be noticed that the diffusions of Ga and In at the interface of metal/GaN are negligible. The formation of ohmic contact can be supposed to the result of low work function of PdIn or PdIn3 alloy. Here, the contact is regarded as pure PdIn/GaN, and the height and width of Schottky barriers become smaller, as shown in Fig. 5b. The lower SBH and thinner Schottky barrier width are benefit to carrier tunneling and overflow, which result in the ohmic contact at the annealing temperature of 400 °C. The specific resistance become even lower when it is annealed above 500 °C. It is observed some indium diffusion into GaN in TEM image, and thus, InGaN could be formed at partial region at the interface. According to the AES and EDS results, the indium content incorporated into n-GaN is about 10 %, and region width is about 40 nm. The spinodal decomposition would be occurred in the formation of InGaN binary [23]. The work function of n-$In_{0.1}Ga_{0.9}N$ is about 0.3 eV higher than that of n-GaN because of the InN special energy band structures [17]. So, the work function of InGaN is almost equal to that of PdIn. The phase separated InGaN layer shows no effective piezoelectric

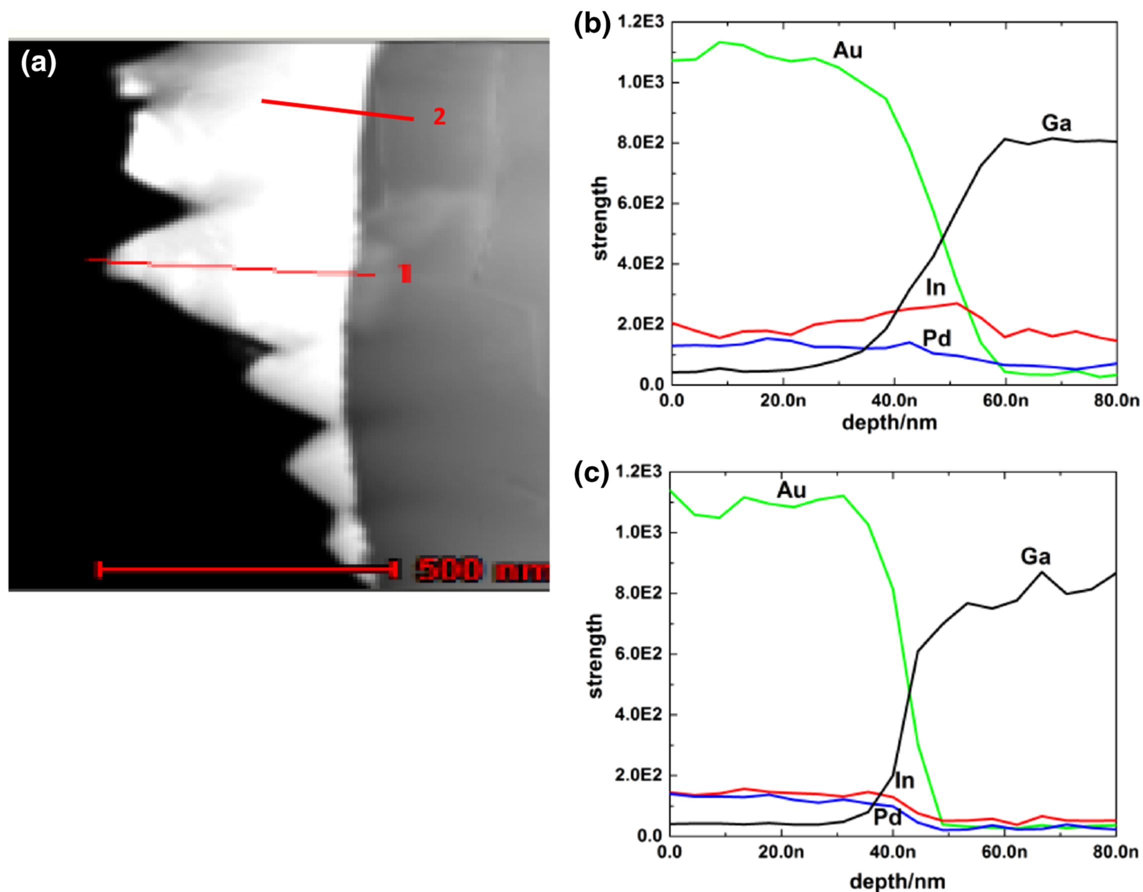

Fig. 4 **a** HAADF TEM image of Pd/In/Ni/Au contact to n-GaN annealed under 250 °C/600 s + 500 °C/30 s. EDS profiles along **b** *Line 1* and **c** *Line 2* which are *red* marked in (**a**)

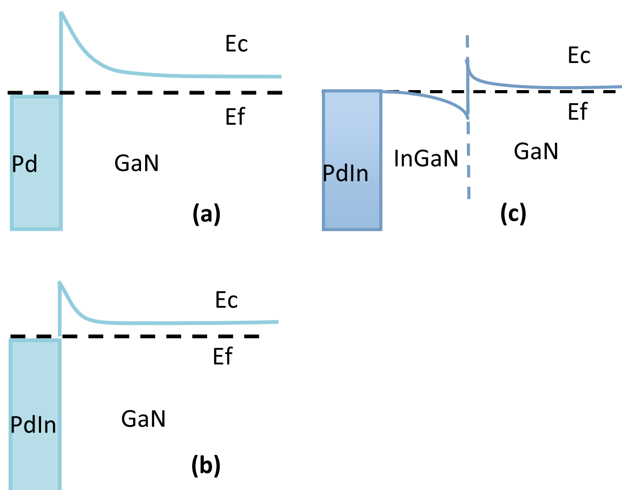

Fig. 5 Band diagram of Pd/In/Ni/Au ohmic contact. The interface changes as the annealing process **a** Pd/GaN, **b** PdIN/GaN, **c** PdIn/InGaN/GaN

polarization because most strain is relaxed. The spontaneous polarization can also be neglected because the positive polarization charges at the contact interface [5]. So, the energy band bending occurs at the heterostructure of InGaN/GaN. It is well known the carriers in wide-band semiconductor will flow into the shallow one. It produces a barrier in n-GaN side and a well in InGaN side. The conduction band offset is about 0.3 eV, so the barrier of n-GaN is smaller than 0.3 eV. Thus, band scheme of PdIn/InGaN/GaN can be drawn as in Fig. 5c. There are no Schottky barriers at InGaN/PdIn. There is electron accumulation in the InGaN side and a very small potential barrier in the n-GaN side. This scheme is favorable to form ohmic contact to N-polar GaN, and thus, the negative effects caused by AlN/N-polar GaN could be eliminated. It is notable that no Ga diffusion is also observed under 500 °C annealing, and this may be contributed from the resist of Pd, as studied in previous works [7, 18].

4 Conclusion

In this work, we proposed Pd/In/Ni/Au to be an effective structure to achieve ohmic contact to N-polar n-GaN. The specific resistance was achieved as low as 5.4×10^{-5}

Ω cm^2. Two-step annealing process with the first step being low temperature but long time and the second step being high temperature but short time was put forward and help to form PdIn alloy and then InGaN binary. The formation of PdIn which effectively prevents the outdiffusion of Ga form n-GaN strengthens the thermal stability of the contact. PdIn/InGaN/GaN contact is the key to obtain low specific resistance ohmic contact for lower SBH and electron accumulation at the interface of GaN/InGaN. Furthermore, the blocking layer structure and the annealing process should be optimized to avoid Au diffusion onto the surface of N-polar n-GaN.

Acknowledgments This work was supported by National Key Basic Research Program of China under Grants No. 2011CB301905, 2013CB328705 and National Natural Science Foundation of China under Grants No. 61334009, 60876063.

References

1. W.S. Wong, T. Sands, N.W. Cheung, M. Kneissl, D.P. Bour, P. Mei, L.T. Romano, N.M. Johnson, Appl. Phys. Lett. **77**, 2822 (2000)
2. T. Fujii, Y. Gao, R. Sharma, E.L. Hu, S.P. DenBaars, S. Nakamura, Appl. Phys. Lett. **84**, 855 (2004)
3. J.S. Kwak, K.Y. Lee, J.Y. Han, J. Cho, S. Chae, O.H. Nam, Y. Park, Appl. Phys. Lett. **79**, 3254 (2001)
4. H.W. Jang, J.H. Lee, J.L. Lam, Appl. Phys. Lett. **80**, 3955 (2002)
5. U. Karrer, O. Ambacher, M. Stutzmann, Appl. Phys. Lett. **77**, 2012 (2000)
6. A. Rizzi, H. Lüth, Appl. Phys. Lett. **80**, 530 (2002)
7. T. Jang, S.N. Lee, O.H. Nam, Y. Park, Appl. Phys. Lett. **88**, 193505 (2006)
8. J.-W. Jeon, T.-Y. Seong, H. Kim, K.-K. Kim, Appl. Phys. Lett. **94**, 042102 (2009)
9. J.-W. Jeon, S.-H. Park, S.-Y. Jung, S.Y. Lee, J. Moon, J.-O. Song, T.-Y. Seong, Appl. Phys. Lett. **97**, 092103 (2010)
10. Y.H. Song, J.H. Son, B.J. Kim, H. Yu, C.J. Yoo, J.-L. Lee, Appl. Phys. Lett. **99**, 233502 (2011)
11. J.-W. Jeon, S.Y. Lee, J.O. Song, T.-Y. Seong, Curr. Appl. Phys. **12**, 225–227 (2012)
12. J. Liu, F. Feng, J. Zhang, L. Jiang, F. Jiang, Thin Solid Films **520**, 2155–2157 (2012)
13. J. Deng, Z. Chen, S. Wang, F. Yu, S. Qi, T. Yu, G. Zhang, Phys. Status Solidi C **9**(3–4), 527–529 (2012)
14. L. Redaelli, A. Muhin, S. Einfeldt, P. Wolter, L. Weixelbaum, M. Kneissl, IEEE Photon. Technol. Lett. **25**(13), 1278 (2013)
15. J.-S. Park, J. Han, T.-Y. S, Opt. Express **22**(S3), A759 (2014)
16. S.Y. Moon, J.H. Son, K.J. Choi, J.-L. Lee, H.W. Jang, Appl. Phys. Lett. **99**, 202106 (2011)
17. C.G. Van, I. de Walle, I. Neugebauer, Nature **423**, 626 (2003)
18. H.S. Venugopalan, S.E. Mohney, J.M. DeLucca, R.J. Molnar, Semicond. Sci. Technol. **14**, 757–761 (1999)
19. T.B. Massalski, H. Okamoto (eds.), *Binary Alloy Phase Diagrams* (ASM, Materials Park, 1996)
20. D.R. Lide (ed.), *CRC Handbook of Chemistry and Physics*, 89th edn. (CRC/Taylor and Francis, Boca Raton, 2009)
21. Z.Z. Chen, Z.X. Qin, C.Y. Hu, Mater. Sci. Eng., B **111**(1), 36–39 (2004)
22. Z. Xu, W. Chen, Vac. Sci. Technol. (in Chinese) **5**(45) (1985)
23. I. Ho, G.B. Stringfellow, Appl. Phys. Lett. **69**, 2701 (1996)