# Low-power phase change memory with multilayer TiN/W nanostructure electrode

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**Abstract** In this paper, multilayer TiN/W with interfacial nanostructure is used as electrode for application in low-power phase change memory (PCM). Compared with single-layer electrode, multilayer electrode has much lower thermal conductive due to the interfacial scattering effect. PCM based on multilayer electrode with different thickness ratio of TiN and W was fabricated and characterized. The device properties including operation voltage and endurance depended critically on the multilayer structure rather than the thickness ratio of TiN and W. The low operation voltage and long cycle life of multilayer-electrode-based PCM result from the increase in overall thermal resistance due to the low thermal conductivity of multilayer electrode.

## 1 Introduction

To break up the bottlenecks of continuous scaling, a number of emerging electronic memory technologies are proposed and considered to be alternatives for replacement of currently mainstream FLASH for future nonvolatile memory technologies. These novel electronic memories include phase change [1], resistive [2], ferroelectric [3], and magnetoresistive random access memories [4]. Phase change memory (PCM) is closest to industry adoption among them

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and has been put into mass production for mobile applications based on 45 nm technology node [5]. It is noted that there is a continuously increasing interest in PCM due to the fact that fundamentally there is no known limit for scaling the device dimensions even well beyond the sub-10 nm regime [6]. The principle of PCM is based on chalcogenide materials that change from a disordered, amorphous structure to a ordered, crystalline structure when an electrical pulse is applied. The reversible order–disorder transition generates a huge resistivity change that can be easily translated into 0 and 1 states of binary data corresponding to the high and low resistive states.

In the process of accelerating commercialization of PCM technology, minimizing the reset current and power has been the most urgent target since the large programming current limits the cell selector downscaling as well as the adoption of PCM in many applications [7]. A large number of research works focus on this problem. Several approaches in terms of phase change material and cell structure are proposed and expected to achieve this goal. To reduce the reset current, one way is to employ phase change materials with low melting point as well as low thermal conductivity since phase change materials are at the heart of PCM. Yoon et al. proposed the Sb<sub>65</sub>Se<sub>35</sub> materials with thermal conductivity of 0.2 W/cm K and melting point of about 560 °C [8]. The reset current of Sb<sub>65</sub>Se<sub>35</sub> device demonstrated about one order of magnitude lower than that of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> (GST). From the point of view of reducing the thermal conductivity, artificially superlattice-like nanostructure was applied to phase change materials such as SbTe/GaSb [9] and SbSe/GaSb [10] for the low-power PCM. Formation of nanocomposite cluster is another effective method to reduce the reset current. Lee et al. [11] reported that the formation of several tens of nanometer scale clusters of GST self-encapsulated by SiO<sub>x</sub>

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could reduce the reset current by 32 % due to the thermal and electrical confinement of the heat and current path as well as the reduction in the effective volume of the phasechanging region.

Since reset current decreases with decreasing the effective contact area between bottom electrode and phase change layer (PCL), many device structures have been explored for low-power PCM. The edge-contact-type cell demonstrated a very low reset current (about 200 µA) with 0.24 µm technology [12]. However, it occupies a large layout area. Later, the cross-spacer PCM was fabricated and exhibited a reset current of 80  $\mu$ A for a 500-nm<sup>2</sup> cell [13]. The problem associated with this structure is the alignment tolerance. The "pore" structure is another technology that shows very small contact area and low reset current [14]. Phase change nanowires are also studied to diminish the reset current and power since the reset current of PCM scales with the programming volume. Xiong et al. [15] reported a self-align PCM nanowires with individual carbon nanotube electrodes. Such device achieved ultralow programming currents, outstanding on/off ratio, and good endurance. However, it is difficult to ensure the completion of mass production for these devices. For the lithographydependent memory devices, the scaling-down is becoming more challenging due to the diffraction limitation of optical lithography [16]. Engineering of electrode is an effective way to achieve low reset current and power since the high thermal conductivity of electrode materials such as W and TiN lead to significant heat consumption. The wasted power in terms of heat loss along electrode constitutes approximately 60 % of total energy for reset operation [17]. Wu et al. [18] reported that the ring structure of TaN/TiN serving as thermally confined electrode can significantly improve the heat dissipation as well as the cycling endurance. A 39-nm bottom electrode with a TaN thermal barrier and 1.5 nm of TiN conductor has demonstrated 90 % reduction of reset current [18]. Recently, phase change and dielectric materials were embedded with multilayer structure for low power by reducing the effective thermal conductivity [9, 19].

In our previous study, the top electrode with TiN(5 nm)/W(5 nm) structure was proposed to confine the heat dissipation and achieve the low power [17]. However, the properties of multilayer structure with different thickness ratio of TiN and W were not yet systematically studied. And it is unclear whether the low power can be achieved for PCM based on other composition of multilayer electrode. In this paper, the thermal and electrical conductivities of multilayer electrode were measured, and the thermal stability is estimated. The device properties of multilayer-electrode-based PCM were systematically studied.

#### 2 Experimental

Transient thermoreflectance technique was employed to measure the thermal conductivity of TiN/W electrode, and the detail process can be found in our previous study. [17] Complementary metal-oxide semiconductor (CMOS) technology with node of 0.18 µm was employed to fabricate the mushroom-type PCM cells with W bottom electrode of 190 nm in diameter. The bottom electrode contact was fabricated by electrochemical plating (ECP) and chemical mechanical polishing (CMP) processes. Sequently, the phase change material was deposited and patterned by sputtering and lithography/etching methods, respectively. The schematic diagram of the PCM structure is shown in Fig. 1. Ga<sub>2</sub>Sb<sub>4</sub>Te<sub>3</sub> film shows fast speed and brilliant data retention [20, 21]. The switching between amorphous and crystalline states could be triggered by an electric pulse as short as 10 ns, and the temperature for 10 year data retention was about 100 °C higher than that of GST. Thus, 50-nm-thick Ga<sub>2</sub>Sb<sub>4</sub>Te<sub>3</sub> film is employed as PCL for PCM in this study. The periodical TiN and W layers were deposited alternately by magnetron sputtering to form multilayer nanostructure serving as top electrode. The thickness of each single layer such as TiN (3 nm) and W (7 nm) (3-7 for short) was controlled by adjusting the sputtering time. Other PCM cells with top electrode of TiN(5 nm)/W(5 nm) (5–5) and TiN(7 nm)/W(3 nm) (7–3) were also fabricated by the same method. The total thickness of top electrode is 50 nm. For comparison, PCMs based on the conventional electrode with single layer of 50-nm-thick TiN and W were fabricated using the same technology. Keithley 2602A parameter analyzer and Tektronix AWG5012b arbitrary waveform generator were used to measure the device properties of PCMs.

### 3 Results and discussion

The thermal conductivity of multilayer TiN/W with different thickness ratio is shown in Fig. 2. The thermal conductivities of 3–7, 5–5, 7–3, TiN, and W are about 0.43,



Fig. 1 Schematic diagram of PCM structure



Fig. 2 Thermal conductivities and resistivities of 3–7, 5–5, and 7–3 films

0.42, 0.44 26.72, and 73.14 W/m K. The measurement error associated with the thickness of sample and the genetic algorithms fitting procedure is less than 7 %. The values of thermal conductivities of single-layer TiN and W are in agreement with the references [22, 23]. The thermal conductivity of multilayer TiN/W film is far smaller than those of single-layer TiN, which is ascribed to the interface phonon scattering [24–26]. The low thermal conductivity helps to reduce the heat dissipation through the electrode and thus to enhance thermal efficiency of PCM cell.

Another important factor relating to power is the resistivity of electrode since large amounts of energy for dissipation will be consumed by its self-heating effect [27]. The resistivities of samples were determined by Hall measurement system which is based on the Van der Pauw method. Hall System can be employed for automatic measurements of resistivity, mobility, and carrier concentration of a wide range of samples. The resistivities of 3–7, 5–5, and 7-3 were about  $6.4 \times 10^{-5}$ ,  $1.1 \times 10^{-4}$ , and  $3.0 \times 10^{-4} \Omega$  cm, respectively, which are comparable with single-layer TiN  $(1 \times 10^{-4} \Omega \text{ cm})$ and W  $(0.6 \times 10^{-5} \,\Omega$  cm, as shown in Fig. 2. The crystalline resistivity of PCL is about  $3.5 \times 10^{-2} \Omega$  cm [28], which is much larger than those of electrodes. Thus, the drive power originates from the Joule heating produced by the PCL for set and reset operations. The self-heating energy generating from electrodes can be neglected due to the low resistivity of multilayer TiN/W film.

Figure 3a shows the cell resistance versus voltage (R–V) characteristics of PCMs based on multilayer and singlelayer electrodes. Set and reset operations were reversibly done at 20 ns pulses. The resistance ratio of reset to set state achieves at least one order of magnitude. For set operation, unlike single-layer-TiN- and w-based PCMs exhibiting a gradual decline in the resistance, 3–7- and 5–5-based ones have a one-step jumping from reset to set states with the increasing pulse amplitude. It indicates that

3-7- and 5-5-based PCMs possess a more reliable set operation under shorter pulse. The minimum values of set voltage are smaller than those of single-layer-TiN- and W-based ones, as shown in Fig. 3a. The minimum values of reset voltage are comparable and ranges from 3 to 3.2 V for 3-7-, 5-5-, and 7-3-based PCMs. Single-layer-TiNand W-based PCMs have the reset voltages of 3.5 and 4 V. respectively. Figure 3b shows the reset voltage distributions of PCMs with different electrodes. Multilayer electrodes have nearly the same range of reset values which are smaller than those of single-layer TiN and W electrodes. The minimum energy necessary for reset operation  $(E_{reset})$ can be estimated by  $V_{\text{reset}}^2/R_{\text{set}} \times t_{\text{reset}}$ . The required average  $E_{\text{reset}}$  of multilayer, single-layer TiN and W were calculated to be around 3.6, 5.0, and 12.8 pJ, respectively. Multilayer structure could be preferable for application in low-power consumption PCM device. It is suggested that the multilayer electrode confines heat better than the single-laver electrode.

Endurance of device cells is tested since it is another important figure of merit for PCM. Electric pulse with 2.6 V-200 ns is employed for set operation and 3.8 V-100 ns for reset operation. Figure 4(a) shows the endurance distribution results of 3-7-, 5-5-, and 7-3-based PCMs. The data were collected from five samples. The endurances of 3-7- and 5-5-based PCMs have the cycle number ranging from  $10^6$  to  $10^7$ . The minimal cycle number (<10<sup>5</sup>) of 20 % 7-3-based PCM may be accounted to variation of fabrication technology and an inappropriate parameter for operation. The cell resistance distribution at set and reset states of PCMs is shown in Fig. 4b. The resistance ratio of reset and set state achieves at least one order of magnitude for all devices. The cycle life of PCM is measured at high ambient temperature (120 °C). The electric pulses with 1.8 V-200 ns and 3.6 V-50 ns were alternately applied to 5-5-based PCM for set and reset operations, respectively. Since the TiN-based PCM requires larger set and reset voltages for switching (see Fig. 3a), the electric pulses with 2 V-200 ns and 4.2 V-50 ns were employed for endurance test. Figure 4c shows the endurance distribution of the 5–5and TiN-based PCM at 120 °C. 5-5-based PCM exhibits a longer cycle life than TiN-based one even at high ambient temperature, suggesting the stable and reliable interface of multilayer structure. The better endurance performance of 5-5-based PCM results from the low electrical and thermal stress as a result of low operation voltages [29]. Figure 4d shows cycle-to-cycle cell resistance distribution at set and reset states. The set resistance of 5-5-based PCM is smaller than that of TiN-based one, and the reset resistance is opposite. Thus, 5-5-based PCM has larger on/off ratio (about 22.8) compared with TiN-based one (about 13.3). In addition, the resistance distribution curves seem steeper for 5–5, suggesting its better resistance distribution.



Fig. 3 a R-V curves of all PCMs under 20 ns for comparison; b reset voltage distributions of PCMs with different electrodes



Fig. 4 a Endurance distribution results of multilayer-electrode-based PCMs; b cell resistance distribution at set and reset states of PCMs. c Endurance and d cell resistance distributions of the 5–5- and TiN-based PCMs at 120  $^{\circ}$ C

The switching speed of PCM is limited to the set operation time since it requires relatively long time to completely crystallize the amorphous region. Figure 5a, b shows cell resistance as a function of pulse width both at 25 and 120 °C for the 5–5-based and TiN-based PCMs, respectively. It is shown that the reset resistance decreases from about  $2 \times 10^6$  to  $3 \times 10^5 \Omega$ , and the set resistance decreases from around  $5 \times 10^4$  to  $1.5 \times 10^4 \Omega$  as the



Fig. 5 Cell resistance as a function of pulse width both at 25 and 120 °C for the a 5-5-based and b TiN-based PCMs

temperature increases from 25 to 120 °C for both PCMs, which results from the existence of lots of thermal energy for switching at a higher temperature. The pulse width decreases with the increasing value of voltage for set operation due to the equivalent energy required to crystallize the programming region. The minimum pulse width required for set operation is as short as 5 ns (the limit of instruments) at 25 or 120 °C for both PCMs. Growth-dominated crystallization mechanism of Ga<sub>2</sub>Sb<sub>4-</sub> Te<sub>3</sub> could be responsible for the ultrafast switching speed [20, 30]. With the pulse width of 5 ns, the minimum voltages of set operation are 2.1 and 2.5 V for 5-5- and TiN-based devices, respectively, at 25 °C. And they decrease to 1.6 and 1.8 V at 120 °C (see Fig. 5). It is shown that 5-5-based PCM has smaller value of set voltage than the TiN-based one no matter what the ambient temperature is, further suggesting lower power of the 5-5-based PCM.

The power consumption of PCM depends critically on reset operation since reset programming consumes the largest energy to reach the melting temperature ( $T_{\rm m}$ ) of phase change material. Generally, the minimum power necessary for reset operation ( $P_{\rm reset}$ ) is proportional to the overall thermal conductivity ( $\sigma_{\rm TLH}^{\rm total}$ ) of PCM [31],

$$P_{\text{reset}} = \sigma_{\text{TH}}^{\text{total}} (T_{\text{m}} - T_{\text{ambient}})$$
(1)

where  $T_{\text{ambient}}$  is the ambient temperature. And  $\sigma_{\text{TH}}^{\text{total}}$  can be deduced from the parallel thermal conductivities of the PCL, bottom and top electrodes, namely [27]

$$\sigma_{\rm TH}^{\rm total} = \sigma_{\rm TH}^{\rm PCL} + \sigma_{\rm TH}^{\rm bottom} + \sigma_{\rm TH}^{\rm top} \tag{2}$$

where  $\sigma_{TH}^{PCL}$ ,  $\sigma_{TH}^{bottom}$ , and  $\sigma_{TH}^{top}$  are thermal conductivities of PCL, bottom and top electrodes, respectively.

The relationship between  $P_{\text{reset}}$  and the minimum reset voltage ( $V_{\text{reset}}$ ) can be described as follows

$$P_{\text{reset}} = V_{\text{reset}}^2 / R_{\text{set}}.$$
(3)

The overall set resistance ( $R_{set}$ ) of PCM is dominated by the PCL. Since the resistivity of multilayer TiN/W is comparable with those of single TiN and W (see Fig. 2),  $R_{set}$  of PCM based on TiN/W is approximately equal to that of PCM based on TiN as well as W. The multilayer TiN/W has lower reset voltage, as shown in Fig. 3, and thus demonstrates the lower  $P_{reset}$ .

Combining Eqs. (1)-(3), the reset voltage can be expressed by

$$V_{\text{reset}} = \sqrt{(\sigma_{\text{TH}}^{\text{PCL}} + \sigma_{\text{TH}}^{\text{bottom}} + \sigma_{\text{TH}}^{\text{top}}) \cdot R_{\text{set}} \cdot (T_{\text{m}} - T_{\text{ambient}})}.$$
(4)

It is shown that the reset voltage of PCM depends crucially on the thermal conductivities of the layers. The thermal conductivity of multilayer TiN/W is much lower than that of single-layer TiN as well as W, which results in the lower reset voltage of PCM based on multilayer TiN/ W. Therefore, low thermal conductivity of the multilayer TiN/W is responsible for low power of the device.

Two-dimensional finite element method was employed to analyze the thermal distribution of PCM cell. The relationship among temperature (*T*), thermal conductivity ( $K_{\text{th}}$ ), and electrical conductivity ( $\sigma$ ) follows the heat equation

$$\rho C_p \frac{\partial T}{\partial t} = K_{\rm th} \cdot \nabla^2 T + |J|^2 / \sigma \tag{5}$$

where  $\rho$ ,  $C_p$ , and J are density, heat capacity, and current density, respectively. The temperature profile in every subdomain can be obtained by calculating heat flux on closed surfaces based on Gauss's law,

$$Q = \int_{A} q \cdot dS \tag{6}$$

where Q and q are the distributed power in subdomains and the heat flux out of subdomain surface S. COMSOL Multiphysics solver was employed to simulate the reset operation with a pulse of 2.9 V–100 ns. Figure 6a–c shows the thermal distribution of 3–7-, 5–5-, and 7–3-based PCMs. Their maximum temperatures are about 770, 780, and 764 °C, respectively, which are higher than melting point of PCL (around 600 °C). Thus, the Joule heating induced by the input pulse is sufficient to melt the originally crystalline programming region. The molten programming area quenching into amorphous state leads to the abrupt increase in device resistance, as a consequence, the reset operation is completed. Figure 6d, e is the thermal distribution of TiN- and W-based PCMs. It is shown that the maximum temperature is around 400 °C for both PCMs, less than the melting point of PCL. Thus, the programming area is still in crystalline state, and device resistance remains unchanged. A larger magnitude of input pulse is required in order to complete the reset operation for the TiN- and W-based devices. It is suggested that the multilayer electrode can serve as thermal barrier to ensure the efficient heat effect on PCL. Figure 6f shows the temperature profile of PCM in which both top and bottom electrodes were composed of multilayer TiN/W. The distributional temperature is higher than other devices (see Fig. 6) due to the better heat resistant of multilayer electrode. Thus, engineering multilayer interface is an effective way to restrict the heat loss from the electrode.



Fig. 6 Thermal distribution simulation of PCM based on: a 3–7, b 5–5, and c 7–3, d TiN, e W, and f both top and bottom electrodes with multilayer nanostructure



Fig. 7 a Schematic cross-sectional structure of PCM; b temperature profile along the central axis of the device



Fig. 8 a Normalized resistance versus isothermal time. b Failure time as a function of reciprocal temperature

In order to visually compare the heat collecting effect of PCMs, the temperature profile along the central axis of device is plotted in Fig. 7. It is shown that the single-layer-TiN-electrode-based PCM has a higher temperature along the central axis of devices compared with single-layer-Welectrode-based one due to the low thermal conductivities of TiN. The thermal profiles almost overlap each other for 3-7-, 5-5-, and 7-3-based PCMs since 3-7, 5-5, and 7-3 have the approximately equal thermal conductivities as well as the electrical conductivities. It is also shown that the multilayer-electrode-based PCMs have a higher temperature along the central axis than single-electrode-based PCMs at the same input pulse of 2.9 V-100 ns, which can be accounted for the better heat confinement of multilayer electrode. It is suggested that a lower voltage can complete the reset operation, and corresponding power is reduced for multilayer-electrode-based PCMs. The position pertaining to the maximum temperature shifted to the top electrode for 3-7-, 5-5-, and 7-3-based PCMs due to the less heat loss along the top electrode compared to bottom electrode. If bottom electrode is fabricated by the multilayer construct as the same as top electrode, the minimum reset voltage and power would further decrease, as evidenced by its outstanding temperature profile (marked by "both," see Fig. 7b).

Data retention is another important factor to affect the application of PCM. The relationship between device resistance and elapsed time was measured at different holding temperature for 5–5-based PCM cell. Figure 8a shows the normalized resistance versus isothermal time. The temperature for 10-year data retention  $(T_{10-y})$  can be obtained from the extrapolated fitting curve based on the Arrhenius equation:  $t = \tau \exp(E_a/k_BT)$ , where  $\tau$ ,  $E_a$ , and  $k_B$  are a proportional time constant, crystallization activation energy, and Boltzmann's constant, respectively. The

failure time (t) is defined as the elapsed time when the device resistance decreases to half of the original reset resistance at the holding temperature (T). Figure 8b shows failure time as a function of reciprocal temperature. It is shown that the 5–5-based device cell can maintain data for 10 years at about 100 °C, which meets the data-retention demand of consumer electronics products.  $E_a$  is calculated to be about 2.75 eV and to overcome such a large energy barrier can account for the good data retention of the device cell.

## 4 Conclusions

In summary, PCMs based on the multilayer top electrode with different thickness ratio of TiN and W were fabricated and systematically characterized for performance improvement. Reversible set and reset operations can be completed, and the devices demonstrate high operation repeatability, even at 120 °C. 3-7, 5-5, and 7-3 have nearly the same operation voltage, state resistance, and endurance distributions. With the same pulse width, the minimum set and reset voltages are significantly smaller than those of single-layer-electrode-based PCMs. The low power of multilayer-electrode-based PCM results from the low thermal conductivity of multilayer TiN/W as a result of the scattering effect. The thermal distribution of PCM that was simulated by a two-dimensional finite analysis confirms the low power of multilayer-electrodebased PCMs. Engineering the electrode with multilayer structure is an effective way to develop low-power PCM.

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- 1. M. Wuttig, N. Yamada, Nat. Mater. 6, 824 (2007)
- F. Pan, C. Chen, Z.-S. Wang, Y.-C. Yang, J. Yang, F. Zeng, Progr. Nat. Sci. Mater. Int. 20, 1 (2010)
- 3. J. Junquera, P. Ghosez, Nature 422, 506 (2003)
- J.-M. Hu, Z. Li, L.-Q. Chen, C.-W. Nan, Nat. Commun. 2, 553 (2011)
- 5. A.L. Lacaita, A. Redaelli, Microelectron. Eng. 109, 351 (2013)
- R. Jeyasingh, L. Jiale, M. A. Caldwell, D. Kuzum, and H. S. P. Wong, in *Phase Change Memory: Scaling and applications*. Custom Integrated Circuits Conference (CICC) (IEEE, San Jose, California, USA, 2012), p. 1
- R. Bez, S. Bossi, B. Gleixner, F. Pellizzer, A. Pirovano, G. Servalli, and M. Tosi, in *Phase Change Memory development trends*. Memory Workshop (IMW) (IEEE International, Seoul, Korea, 2010), p. 1
- 8. Y. Sung-Min, L. Nam-Yeal, R. Sang-Ouk, C. Kyu-Jeong, Y.S. Park, L. Seung-Yun, Y. Byoung-Gon, K. Myung-Jin, C. Se-Young, M. Wuttig, IEEE Electron Device Lett. **27**, 445 (2006)
- 9. T.C. Chong, Appl. Phys. Lett. 88, 122114 (2006)
- Y. Hu, X. Feng, S. Li, T. Lai, S. Song, Z. Song, J. Zhai, Appl. Phys. Lett. 103, 152107 (2013)
- T.-Y. Lee, K.H.P. Kim, D.-S. Suh, C. Kim, Y.-S. Kang, D.G. Cahill, D. Lee, M.-H. Lee, M.-H. Kwon, K.-B. Kim, Y. Khang, Appl. Phys. Lett. 94, 243103 (2009)
- 12. Y. H. Ha, J. H. Yi, H. Horii, J. H. Park, S. H. Joo, S. O. Park, U. I. Chung, and J. T. Moon, in *An edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption*. Symposium on VLSI Technology. Digest of Technical Papers. (IEEE, Kyoto, Japan, 2003), p. 175
- 13. W. S. Chen, C. Lee, D. S. Chao, Y. C. Chen, F. Chen, C. W. Chen, R. Yen, M. J. Chen, W. H. Wang, T. C. Hsiao, J. T. Yeh, S. H. Chiou, M. Y. Liu, T. C. Wang, L. L. Chein, C. Huang, N. T. Shih, L. S. Tu, D. Huang, T. H. Yu, M. J. Kao, and M. Tsai, in A Novel Cross-Spacer Phase Change Memory with Ultra-Small Lithography Independent Contact Area. Electron Devices Meeting, IEDM (IEEE International, Washington, DC, 2007), p. 319
- M. Breitwisch, T. Nirschl, C. F. Chen, Y. Zhu, M. H. Lee, M. Lamorey, G. W. Burr, E. Joseph, A. Schrott, J. B. Philipp, R. Cheek, T. D. Happ, S. H. Chen, S. Zaidi, P. Flaitz, J. Bruley, R. Dasaka, B. Rajendran, S. Rossnage, M. Yang, Y. C. Chen, R.

Bergmann, H. L. Lung, and C. Lam, in *Novel Lithography-Independent Pore Phase Change Memory*. IEEE Symposium on VLSI Technology (IEEE, Kyoto, Japan, 2007), p. 100

- F. Xiong, M.-H. Bae, Y. Dai, A.D. Liao, A. Behnam, E.A. Carrion, S. Hong, D. Ielmini, E. Pop, Nano Lett. 13, 464 (2012)
- 16. W.I. Park, B.K. You, B.H. Mun, H.K. Seo, J.Y. Lee, S. Hosaka, Y. Yin, C.A. Ross, K.J. Lee, Y.S. Jung, ACS Nano 7, 2651 (2013)
- Y. Lu, S. Song, Z. Song, L. Wu, A. He, Y. Gong, F. Rao, B. Liu, Appl. Phys. Lett. **101**, 113104 (2012)
- J. Y. Wu, M. Breitwisch, S. Kim, T. H. Hsu, R. Cheek, P. Y. Du, J. Li, E. K. Lai, Y. Zhu, T. Y. Wang, H. Y. Cheng, A. Schrott, E. A. Joseph, R. Dasaka, S. Raoux, M. H. Lee, H. L. Lung, and C. Lam, in A Low Power Phase Change Memory Using Thermally Confined TaN/TiN Bottom Electrode, 2011, p. 3.2.1
- D. Loke, L. Shi, W. Wang, R. Zhao, L.-T. Ng, K.-G. Lim, H. Yang, T.-C. Chong, Y.-C. Yeo, Appl. Phys. Lett. 97, 243508 (2010)
- K.F. Kao, C.M. Lee, M.J. Chen, M.J. Tsai, T.S. Chin, Adv. Mater. 21, 1695 (2009)
- Y. Lu, S. Song, Z. Song, W. Ren, Y. Cheng, B. Liu, Appl. Phys. Express 4, 094102 (2011)
- W. Lee, M. Siddik, S. Jung, J. Park, S. Kim, J. Shin, J. Lee, S. Park, M. Son, H. Hwang, IEEE Electron Device Lett. 32, 1573 (2011)
- 23. K. Nitta, T. Nohira, R. Hagiwara, M. Majima, S. Inazawa, J. Appl. Electrochem. 40, 1443 (2010)
- 24. G. Chen, Phys. Rev. B 57, 14958 (1998)
- 25. X.Y. Yu, G. Chen, A. Verma, J.S. Smith, Appl. Phys. Lett. 67, 3554 (1995)
- 26. G. Chen, M. Neagu, Appl. Phys. Lett. 71, 2761 (1997)
- U. Russo, D. Ielmini, A. Redaelli, A.L. Lacaita, IEEE Trans. Electron Devices 55, 506 (2008)
- H. Zhu, J. Yin, Y. Xia, Z. Liu, Appl. Phys. Lett. 97, 083504 (2010)
- C. Kim, D. Kang, T.-Y. Lee, K.H.P. Kim, Y.-S. Kang, J. Lee, S.-W. Nam, K.-B. Kim, Y. Khang, Appl. Phys. Lett. 94, 193504 (2009)
- L. van Pieterson, M.H.R. Lankhorst, M. van Schijndel, A.E.T. Kuiper, J.H.J. Roosen, J. Appl. Phys. 97, 083520 (2005)
- A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, in *Scaling Analysis of Phase-Change Memory Technology*, 2003 (Electron Devices Meeting, 2003), p. 699