Degradation sources of CdTe thin film PV: CdCl$_2$ residue and shunting pinholes

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Abstract The present work considers two observable phenomena through the experimental fabrication and electrical characterization of the rf-sputtered CdS/CdTe thin film solar cells that extremely reduce the overall conversion efficiency of the device: CdCl$_2$ residue on the surface of the semiconductor and shunting pinholes. The former happens through nonuniform treatment of the As-deposited solar cells before annealing at high temperature and the latter occurs by shunting pinholes when the cell surface is shunted by defects, wire-like pathways or scratches on the metallic back contact caused from the external contacts. Such physical problems may be quite common in the experimental activities and reduce the performance down to 4–5 % which leads to dismantle the device despite its precise fabrication. We present our electrical characterization on the samples that received wet CdCl$_2$ surface treatment (uniform or nonuniform) and are damaged by the pinholes.

1 Introduction

Recently, we have theoretically modelled the chalcogenide thin film solar cells from different aspects of band gap grading (from both valence and conduction bands) [1, 2] as well as generation-recombination mechanisms [3]. Currently, it is well known that CdCl$_2$ treatment prior back contacting the cell can greatly improve the electrical characteristics and stability of CdTe solar cells [4, 5]. The suggested reasons are that this treatment can: increase the grains size to about 1–2 μm [6], reduce the surface and interfacial energy [7] and randomise the orientation of CdTe film [8]. The bigger grains and fewer boundaries in thin films lead to longer minority carrier lifetime and lower resistivity due to less grain boundaries. CdCl$_2$ treatment and annealing at high temperature either during or after CdTe deposition is a commonly used process to increase the grains size, density of the CdTe film and recrystallization. However, this is a very critical step especially when the treatment with the CdCl$_2$ solution is not achieved by the dry vacuum process such as physical vapour deposition but through a wet surface treatment. Eventually, the problem arises when the residue of CdCl$_2$ is left on the film surface and may not be eliminated or washed out from the surface of the film due to formation of oxychlorides which are insoluble in water [9, 11]. Niles et al. [10] suggested that CdO, TeO$_2$ and TeCl$_2$O are building blocks for the surface Cl residue. This happens when CdCl$_2$ solution does not cover the cell surface uniformly and leaves residuals before the annealing process. The residue of CdCl$_2$ will be a solid barrier for the metallization of the back contact on the film surface. The other common issue which has comparable effect on the performance of the device comes from the shunting pinholes (weak-diodes) or wire-like shunting pathways through front and back contact. The defective pinholes or local spots on the surface of the solar cell can shunt the photocurrent through formation of a wire-like connection, thus decreasing the measured shunt resistance, open circuit voltage. Finally, the overall performance of the device is reduced extremely and the electrical parameters of the device are degraded [12]. Both above issues have been shown to reduce the conversion efficiency down to 4–5 % which leads to sample dismantle. We experimentally verify such strong effects of both degradation resources on the electrical parameters of the CdTe device

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and show how the series and shunt resistances as well as performance parameters degrade effectively.

2 Experimental procedure

In this study, CdS/CdTe samples were rf-sputtered in AJA system at 250 °C onto a rotating TEC15 glass substrate coated with a high resistive transparent (HRT) layer of SnO_2:F. The thin films were deposited at 10 mTorr argon pressure, 50 W rf power with a substrate temperature of 270 °C. A CdS layer of 60 nm thickness was chosen as the heterojunction partner (window) of CdTe cells. The sputtered CdTe thickness was 2.1 μm. During deposition, the sputtering rate was calculated using an in situ thickness monitor system and also verified by a DEKTAK profilometer after finishing the device. As-deposited CdS/CdTe films were then $CdCl_2$ treated and annealed at a high temperature of 387 °C as the standard activation temperature for sputtered cells. The treatment system includes a glass tube furnace in which the temperature is controlled by two halogen lamps on top and two other on bottom (750 W/lamp). The samples are activated between two graphite susceptors (9/16″ thick) for uniform heat distribution and two thermocouples to control the temperature of each side. After the heat treatment, the samples were blown N_2 gas to remove the dusts before Cu/Au back contact metallization (3.2 nm Cu and 20 nm Au) in a Bell-jar thermal evaporation system. Finally, a copper diffusion heat treatment of 150° for 45 min was performed in room air ambience [13]. We note the $CdCl_2$ treatment was achieved after a methanol rinse; the samples were treated by a syringe which sucks in and drops a few $CdCl_2$ solutions over the surface of the samples. This step is very critical since it is done by hand and depends mostly on the experience of the experimenter, considering the effects of this step is one of the targets of this manuscript. The electrical characterization was achieved under illumination of 100 mW/cm^2 through pogo-pin electrodes. A fan was cooling the characterization area to reduce the temperature effect on the current generation rate.

3 Results and discussion

3.1 $CdCl_2$ treatment

The common activation solution for almost all CdTe-based thin film solar cells is $CdCl_2$ solution. However, the method of activation is different depending on the thin film deposition method. For example, the films grown by the close-spaced sublimation technique receive $CdCl_2$ by evaporation [14]. The evaporated solution uniformly covers the thin film and it can be immediately inserted into activation system. However, this method is not used in many other techniques like rf-sputtering techniques which the treatment solution is dropped by hand using syringe or sucking tools. Attention must be paid to cover the entire sample uniformly and prevent the surface residuals. In our experiments, the sputtered CdS/CdTe sample is first cleaned by methanol and then is heated for some seconds. Next, a few drops of $CdCl_2$ solution are poured over the sample by syringe and we wait for the solution to cover all over the surface. However, this step is not easy to handle since $CdCl_2$ dries in some seconds before spreading over.

The difference between the uniform and nonuniform covered samples with $CdCl_2$ is clear by the white fringes, solids (salt) and lines which appear some seconds after this solution dries out. Ignoring this critical issue and heating the cell with such inappropriate treatment can lead to quite low performance and to dismantle the cell. Figure 1 shows the difference between uniform and nonuniform $CdCl_2$ treatments. The dense white areas in Fig. 1b (indicated by the arrows) are formed when the solution cannot spread over uniformly and instead leaves residuals in some track forms. To show the importance of this step, both samples have been annealed at 387 °C after the treatment and finished by the metallization.

The solubility properties and relatively high thermal stability of the residue suggest the presence of the oxychloride $Cd_3Cl_2O_2$ rather than $CdCl_2$ as the major chlorine-containing component. From various methods tested for their effectiveness in removing the residue, only HNO_3 etches removed all detectable traces of chlorine from the surface [9]. Our assumption was that the residue is primarily $CdCl_2$, which is soluble in both water and methanol. However, we found that much of the residue is insoluble in both water and methanol.

We activated the sample with residue at high temperature to test if the residue concentration and shape change, but the residue became even, more solid with whiter colour representing that the salt of $CdCl_2$ becomes more rigid after the annealing. This makes a physical barrier between the CdTe surface and the metal back contact later on. The results of annealing in Ar indicated that surface oxides form independent of whether oxygen is provided by the annealing ambient.

The relevant current–voltage curves are drawn for each sample in Fig. 2. The gap between the curves is significant. The efficiency of the nonuniform treated cell (with residuals) is 5.84 % while that of the uniformly treated one is about 11.83 %. This is a significant difference that was verified by repeating the treatment several times. A nonuniform treatment has a very strong influence on the performance because of the decrease in the V_{oc} and J_{sc}. Normally, when the solution residue over the cell, the

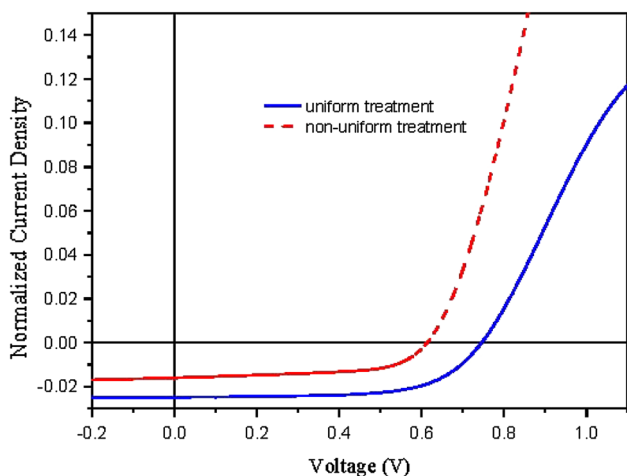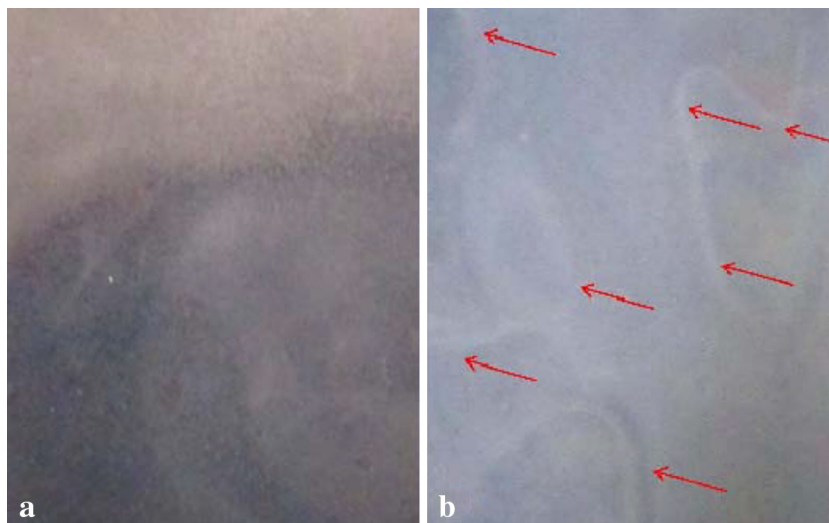**Fig. 1** The CdS/CdTe thin films treated with $CdCl_2$ solution. **a** Uniform and **b** nonuniform treatment (with $CdCl_2$ residue)

through a mask to provide a dot cell having an area of about 0.062 cm^2. The samples were characterized under 1 Sun illumination at room temperature. Clearly, the higher values of all the parameters are associated with the uniformly treated sample (green boxes). The nonuniformly treated sample (b) resulted in maximum values $V_{oc} = 613$ mV, $J_{sc} = 21.29$ (mA/cm^2), FF = 59.57 % and $\eta = 5.8$ %. The uniformly treated sample (a), $V_{oc} = 748$ mV, $J_{sc} = 24.87$ (mA/cm^2), FF = 65 % and $\eta = 12$ % were obtained. Almost all the parameters are in the upper 50 % of the box meaning that 35 cells have similar characteristics. Still some of the cells behave differently leading to a scattered data in the box plot. The reason for such different results can be due to surface shunting pathway or measurement tools effects. This will be discussed in the next section. Therefore, uniformly $CdCl_2$ treated cells behave quite better than the nonuniform ones as the treatment is expected to enlarge the grain boundaries (>1.7 μm) and show higher V_{oc} [13]. The sediment $CdCl_2$ solution appears as white tracks on the surface reduces. The uniform diffusion of chlorine into CdTe film and the grain boundaries are not expected to passivate well and the devices show poor electrical properties. A good chlorine activation significantly increases the minority carrier lifetime (higher J_{sc}) in CdTe and reduces the grain boundary recombination and native defects densities [16]. Then, the photo-current and open circuit voltage increase and the series resistance reduce. Furthermore, such sediment material on the surface of the cell will impede the perfect back contacting. The Cu diffusion from the Cu/Au contacts cannot passivate such solids and the series resistance, R_s, increases leading to a lower FF. The average R_s for sample (a) and (b) is 4.5 and 8 (Ω.cm^2), respectively. This higher R_s for sample (b) decreases the FF, consequently. Paudel et al. [17] suggested that an optimized

Fig. 2 The current–voltage characteristics of the cells prepared with *a* uniform and *b* nonuniform treatment (with $CdCl_2$ residue)

$CdCl_2$ solution is washed out by methanol and dried by heating for some seconds and the above process is repeated again. Disregarding such residuals lead to the low performance parameters in Fig. 2. Surprisingly, shaking the sample for some seconds after the $CdCl_2$ pouring can help to spread the solution all over the sample and to make a uniform treatment [15]. This avoids sediments of the solution on the cell surface and the rest of the solution goes to the edges out of the solar cell area.

Figure 3 displays the normalized electrical parameters in box plot: open circuit voltage V_{oc}, short circuit current J_{sc}, fill factor FF and efficiency (η) for the 35 cells fabricated on each of the two (*a*) and (*b*) samples. The horizontal axis in Fig. 3 is the number of the cells from 1 to 35. The open circuit voltage is compared in actual values as its values are already less than one. All the data were obtained after finishing the cell with Cu/Au back contact deposited
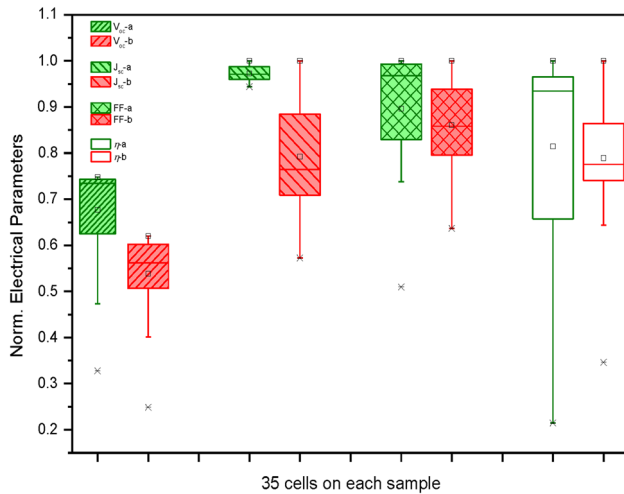
Fig. 3 The box plot of normalized electrical parameters obtained for the samples with *a* uniform and *b* nonuniform treatment (having residuals). The *middle line* of *box*: median; *small dot* inside the *box*: mean. The *upper line* of each *box* is the maximum value of the parameter and the *lower line* of the plot means the minimum data obtained for relevant parameter

Fig. 4 The current–voltage characteristics of the uniformly treated samples with shunting pinholes (scratched) and intact (not scratched) cells. The inset is the circuit of the shunting pathway due to pinholes which rob the current and leads to $-\Delta V_{oc}$

$CdCl_2$ treatment for an optimized Cu back contact thickness will increase the cell stability. The roll-over at high voltages in the current–voltage characteristics of the uniformly treated cell is ascribed to the Schottky barrier at the back contact which impedes the hole transport and limits the current. This roll-over could be removed by chemically etching the cell surface prior to treatment and metal deposition. This pre-treatment will create Te+ surface and passivate the holes at the back region. Probably, despite the uniform treatment, the surface of this sample was having oxidation which was not removed through washing by deionized water.

4 Shunting pinholes

The shunting pinhole can form due to the incomplete coalescence of the CdTe grains during deposition, because of defects in the underlying surface or microscopic contamination on the surface, surface shunting between the metallic back and conductive front layer (TCO) during fabrication or electrical characterization. Such shunting pinholes can also form when installing the sample in the thickness profiling system, current–voltage or capacitance–frequency characterization tools which slightly or strongly remove a small part of the surface material and make a big shunting resource. This phenomenon is quite probable in thin film fabrication laboratories and some of them can be seen by the naked eye and some of them are in the range of nanometres. Shunting pinholes are still worse than residues from the nonuniform treatment as they cannot be recovered
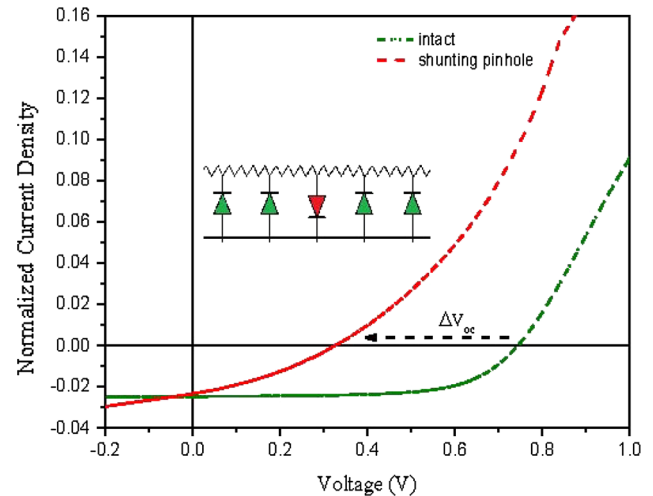
or cured. Karpov has quantitatively considered that such defective spots can change the distribution of electrical parameters (e.g. R_{sh}, V_{oc}) to strongly nonuniform electric potential and extremely reduce the device efficiency [18]. In our uniformly treated samples, the most destructive scratching resource was the characterization set-up when the cells go under contact with pogo pins and needles for the current–voltage or capacitance–frequency measurements. Any external contact to the cells must be done very delicately to avoid any local spot, scratch and removal. Anyway, repeating the electrical measurements with the needles will also destroy the back contacts unavoidably. The copper tape can be replaced in such cases, but it will also remove a thin layer of the metal when disconnecting. These kinds of disordered layers cause lateral shunting due to nonuniform topography and morphology [19]. The semiconductor nonuniformities were suggested to be filled by aniline mixtures (polyaniline) or even red-wine by electropolimerization of the aniline monomers (before metallization) which prevents the shunting of the front and back contacts [5, 8]. The current–voltage characteristics of two samples (uniformly treated) with shunting pinholes and intact, are displayed in Fig. 4. The intact sample is without scratches while the shunting pinholes come from the scratches caused by the pogo pins' contact on the surface of the metallic back contact. The shunting pinholes of our samples are mostly because of the scratches from the pogo pins used for electrical measurements. Clearly, there is a big difference in the open circuit voltage, $\Delta V_{oc,}$ between two samples. This is due to the high recombination rate in the scratched area which is acting as a shunting path through the back contact. The inset represents the
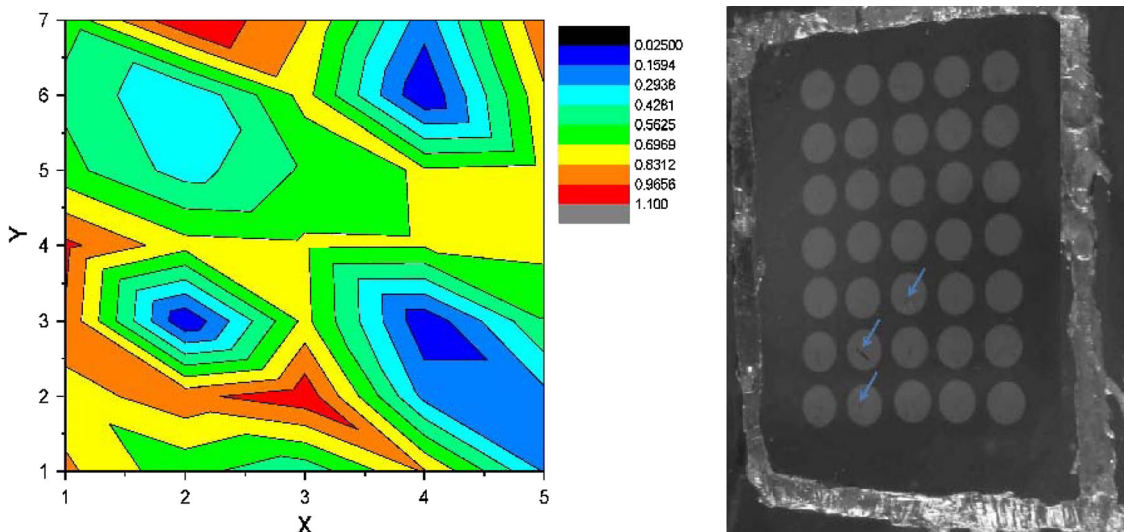
Fig. 5 Contour plot for the shunt resistance of the sample including shunting pinholes on the surface. The *blue* areas have the lowest R_{sh} due to pinholes while the *red* areas are intact cells
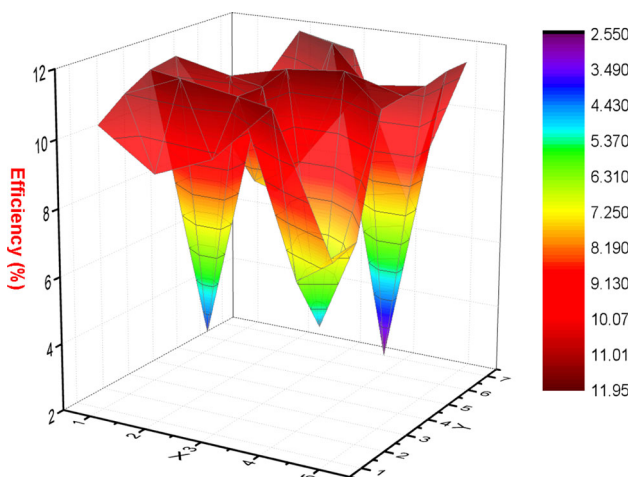

Fig. 6 *Left*: counterplot and *b*: 3D diagram of the efficiency for the sample with 35 solar cells deposited in 7×5 position. The *blue* and *red* areas have highest and lowest efficiency, respectively. The *blue* areas are with scratched surfaces

schematic circuit including a weak diode that takes into account such pinholes on the surface [16]. As it is deduced from the curve, the intact sample with no shunting defect has $V_{oc} = 746$ mV while the shunted one has $V_{oc} = 328$ mV. The $-\Delta V_{oc}$ of the damaged sample lowers the FF from 64.37 to 33.21 % and the efficiency from 11.90 to 2.55 %. The current density is almost not affected in this case. However, there are some of the cells which show a quite low current density as well.

This could be because of low carrier collection from the scratched cells. In our case, the back contact area is big enough to compensate such disability. In order to show the shunting areas with high recombination rate on our samples, R_s has been shown with a two-dimensional diagram in Fig. 5. The xy axes show the directions and number of the deposited solar cells. The blue and red areas are shunted and intact areas with higher and lower shunt resistances due to low and high recombination paths, respectively. The distribution of the low resistance elements, i.e., shunts, R_{sh}, shows that the cell has several scratches on the surface. The blue areas show a low R_{sh} of about 0.02–0.35 (k.Ω.cm^2), while it is about 0.7–1.2 (k.Ω.cm^2) for the red areas. The weak diodes cause lower V_{oc} leading to lower the local efficiency. Extending these damages to the panel scale where many of such small modules are integrated altogether makes these disorders much more important. Note that the disorders or shunts are also created under bias, long-term illumination or temperature fluctuations [20] and different analytical methods are needed to consider the influence of such failure mechanisms [21]. The systematic studies on the shunt resources by laser scribing as an intentional way to scratch the cell revealed that the local spots can cause variation in the electric field in a weak diode, accelerate the defect creation by excessive local carrier concentration or local corrosion and as a result degrade the cell in such way that cannot be recovered by light soaking or isolating the shunting areas [16]. We only considered the surface shunts and pinholes due to contacted pogo-pins during IV characterization. Delicate contact of these pins with the cell will not damage the surface. However, strong pressure has been considered to have reversible dependence on the solar cell parameters expected from the piezo-electric properties of CdS window layer [22]. For example, V_{oc} decreases with increasing the pressure as the piezoelectric charge density induces the voltage across the cell. The effect of surface erosion

(shunting pathways) on the efficiency of 35 solar cells is shown through counterplot and three-dimensional (3D) topography in Fig. 6a, b. The lower efficiencies appear as downward cones in the relevant positions. The lowest efficiencies (3–5 %) in blue colour are due to scratches while the red areas represent the safe cells with about 10–12 % of efficiency. Clearly, the most part of the cell exhibits high efficiency. Further studies on the disordered surfaces including scratch or local spots can be done by lock-in thermography of thin film CdTe/CdS solar cells. The spatial variations on the device surface influence the local characteristics. A bright spot on the back contact represents a weak diode with V_{oc} lower than the other parts [23]. At this time, there is no solution to recover the scratched pinholes. However, the laser scribing is proposed to isolate and cut the scratched area from the rest of the cell [19]. This technique can also leave metallic particles and to the removal of dust in the scribed area leading to new shunting pinholes. Therefore, care must be taken to avoid the occurrence of such local disorders. The solar panels are usually protected by a glass frame to avoid such physical problems which can also come from environmental impacts. There is a debate on how to get rid of the pinhole formation during the processing of different materials. Some of the laboratories use instead of a mechanical contact graphite-Hg paste or silver paste that of course can result in some other issue related to the different materials interfaces.

5 Conclusion

Two physical problems effective on the electrical parameters of rf-sputtered CdS/CdTe solar cells were considered; the nonuniform $CdCl_2$ treatment and surface scratches. Each issue is a common problem in thin film deposition laboratories and disregarding them leads to quite low performance and sample dismantles. The electrical characterization of the cells with nonuniform $CdCl_2$ treatment, which appears as white solid residuals on the cell surface, reduces the efficiency down to 4–5 %. This originates from both lower J_{sc} and V_{oc} as in nonuniform treatment; $CdCl_2$ cannot diffuse perfectly into the thin film structure to increase the grain size. The box plot of the electrical parameters shows that the lower J_{sc} and V_{oc}, FF and η are obtained through nonuniform treating of the cell. The other issue is the surface defective pinholes and shunting pathways which rob the current and reduce the performance to 3–5 %. We presented the efficiency of this sample (35 solar cells) in 3D plot to show how the scratched areas have lower efficiency than the safe ones. This low performance

is mostly determined by V_{oc} since the recombination rate increases in those spots. The 2D topography of the R_s and η for the shunted cells reveals that the local spots are low shunt resistance areas 0.1–0.4 (k.Ω.cm^2). This requires that the electrical needles contact the cell surface delicately. Electropolimerization of an organic material on the semiconductor CdTe surface before back contacting can avoid shunting pinholes.

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