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RAPID COMMUNICATION

Thermal conductivity of VLS-grown rough Si nanowires with various surface roughnesses and diameters

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Abstract In this paper, we synthesize VLS-grown rough Si nanowires using Mn as a catalyst with various surface roughnesses and diameters and measured their thermal conductivities. We grew the nanowires by a combination vapor-liquid-solid and vapor-solid mechanism for longitudinal and radial growth, respectively. The surface roughness was controlled from smooth up to about 37 nm by the radial growth. Our measurements showed that the thermal conductivity of rough surface Si nanowires is significantly lower than that of smooth surface nanowires and decreased with increasing surface roughness even though the diameter of the smooth nanowire was lower than that of the rough nanowires. Considering both nanowires were grown via the same growth mechanism, these outcomes clearly demonstrate that the rough surface induces phonon scattering and reduces thermal conductivity with this nanoscale-hole-free nanowires. Control of roughness induced phonon scattering in Si nanowires holds promise for novel thermoelectric devices with high figures of merit.

1 Introduction

The thermal conductivity reduction of nanowires due to the strong phonon boundary scattering is well known since it has been demonstrated experimentally and explained theoretically [1–7]. This reduced thermal conductivity is beneficial for the performance of thermoelectric devices. Recently, Hochbaum et al. [2] showed that thermal conductivity of electrolessly etched rough Si NWs was a factor of 5 to 10 times lower than that of smooth surface nanowires even though the diameters of the two nanowires were similar. This significant reduction could not be explained by the existing phonon boundary scattering so, this triggered many theoretical works [8–11]. For example, L. Liu and X. Chen [8] computed the thermal conductivity of rough Si NWs considering two geometrical parameters, amplitude and wavelength, in their characterization of surface roughness. They suggested that the thermal conductivity could be reduced when the wavelength of the roughness is small or the amplitude is large. Martin et al. [9] predicted that thermal conductivity of rough Si NWs is proportional to $(d/h)^2$, where d is the diameter and h is the surface roughness. Moore et al. [10], using a Monte Carlo simulation, concluded that the conventional surface scattering that was bounded between specular and diffuse reflection was not adequate to explain thermal conductivity in rough nanowires. Therefore, they suggested phonons scattered backward in the roughened surface. Chen et al. [11] suggested that phonon boundary scattering of rough NWs should depend on frequency since the conventional frequency independent phonon boundary scattering failed to explain thermal conductance in thin, rough nanowires.

However, nanoscale pores presented in the electrolessly etched nanowires [12] hinders one to be fully convinced that the surface roughness solely made contribution to the significant reduction in thermal conductivity. Recently, Hippalgaonkar et al. [13] reported thermal conductivity of rough Si nanowires and demonstrated that it is still lower than that

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of smooth Si nanowires. Their nanowires were synthesized by the wafer-scale etching technique. However, yet experimental data on thermal conductivity of rough NWs are so scarce [2, 13] that none of these theoretical studies have been verified yet due to the lack of rough surfaced nanowires that are enough to test the relationship. In this regard, the role of surface roughness on the phonon scattering is unclear and has to be clearly addressed by experiment. Herein, we report Si nanowires grown by a combination of vapor–liquid–solid (VLS) and vapor-solid (VS) mechanism using Mn as a catalyst. This approach makes it possible to develop and systematically vary rough surfaces in Si NWs without creating nanoscale holes in the NWs. Our measurements demonstrated significant thermal conductivity reduction in these rough surfaced Si NWs, as compared to smooth surfaced nanowires. The thermal conductivity decreased with increasing surface roughness.

2 Experimental methods

Rough surface Si NWs were grown on Si (100) substrates by the CVD process. Prior to growing nanowires, substrates were etched by wet chemicals to remove any residual contamination. Growth was initiated by introducing silicon chloride ($SiCl_4$, Aldrich, 99.999%) within a H_2 carrier gas into a hot-walled horizontal reactor, upon where the Si substrate was placed. $MnCl_2$(purity 99.99%) powder, as a precursor for the metal catalyst, was placed upstream of the horizontal reactor. The horizontal reactor was heated to 1000°C and held for 30 min. H_2 and Ar gas were introduced with a total gas flow rate up to 3500 sccm (linear velocity of 11 cm/s). For comparison, Si nanowires were also grown under the same conditions by using an Au and Pt catalyst in the form of 2 nm thin films on the substrates. Si NWs were characterized by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The composition of Si NWs and catalyst were analyzed by energy dispersive spectroscopy (EDS).

We used suspended membranes fabricated by the MEMS technique for thermal conductivity measurements. Details regarding the experimental procedure are available in the literature [14], so only a brief explanation is provided here. Essentially, this method is based on the standard heat-source and heat-sink method, which is scaled down to measure the thermal conductivity of a nanowire. The membrane consists of silicon nitride and a platinum coil. An isopropyl alcohol (IPA) solution containing Si nanowires was dropped onto the membranes, resulting in Si nanowires being present on the membranes after IPA evaporation. To enhance thermal contacts the between nanowire and membranes, Pt/C was deposited by an FEI Quanta 3D Dual Focused Ion Beam. Then, the device was packaged and placed on a variable temperature cryostat. One of the membranes was heated by applying a current to the Pt coil, which serves as a heater and thermometer. A fraction of the heat generated was transported through the nanowire and reached the other membrane. Thermal conductivity of the nanowire was extracted by calculating heat transported through the nanowire and the temperatures of the membranes. The temperature of the membranes was obtained by measuring the resistance of the Pt heater. Thermal conductivities of Si NWs were measured in the temperature range of 40–420 K, and all the measurements were conducted under high vacuum.

3 Results and discussion

Rough Si NWs were successfully grown on a Si (100) substrate by a VLS mechanism with assistance of an Mn catalyst. As shown in Fig. 1a, the Si NWs are tenths of μm in length and tenths of nm in diameter. Compared to other metal catalysts, such as Au or Pt [15], Mn catalysts lead to rather slow nanowire growth under the experimental conditions described above. The nanowires have metal globules at their tips, as shown in Fig. 1b. Figure 1c shows the EDS spectra of the nanowires and metal globules. The globules were a Si-Mn alloy consisting of about 64% Si and 36% Mn (see Fig. 1b). These globules clearly indicate that the nanowires were grown by the VLS mechanism with the assistance of Mn as a catalyst. We confirmed that there is no Mn in the nanowire body. Thus, Mn works as a typical VLS catalyst, i.e., the ratio of C_s/C_l of Mn, where C_s is the solubility of Mn in solid Si and C_l is the solubility of Mn in liquid Si, is quite low, and, thus, no Mn was incorporated into Si nanowires during growth [16].

In our investigation on the processing parameters, we found that a high carrier gas flow rate can induce surface roughening. For example, a rough nanowire shown in Fig. 1d was grown under a flow rate of 3000 sccm. As shown in Fig. 1d, the rough surface nanowires were typically tapered, with a typical diameter of 300 nm at the bottom to 50–70 nm at the tip, while the smooth surface nanowires had a uniform diameter along the growth direction. Moreover, the surface of the bottom portion of the nanowires was rougher. Figure 1e shows high-magnification TEM images of rough Si NWs, from top to bottom in the locations denoted in Fig. 1d. These images indicate that nanowires are tapered along the nanowire axis. Figure 1f shows representative selected area electron diffraction (SAED) patterns of the nanowires. The nanowires were single-crystal grown in the <111> direction with little dislocations or stacking faults.

The effect of gas flow rates on the surface roughening was investigated systematically. Figure 2a–d shows TEM

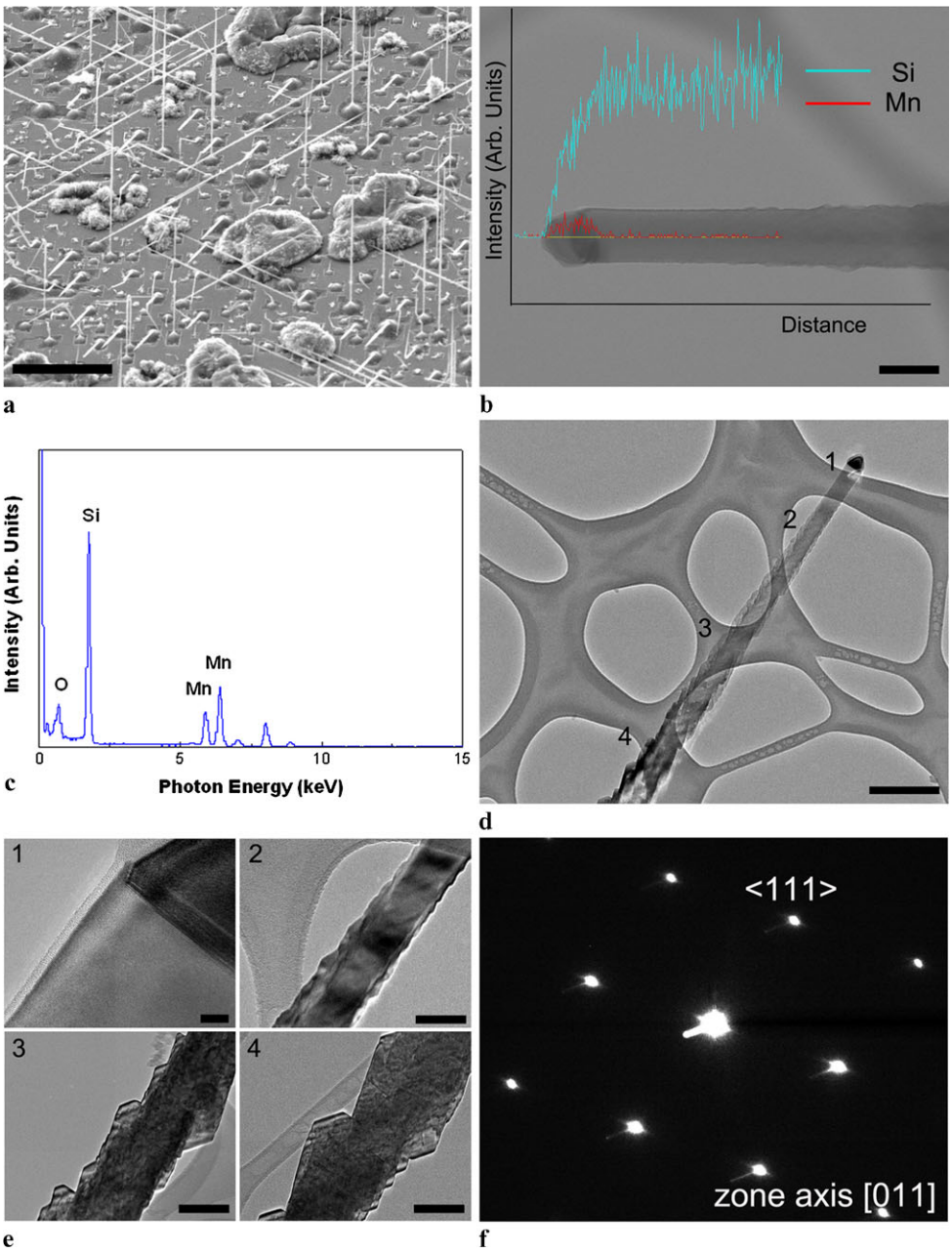

Fig. 1 **a** SEM image of rough surfaced Si NWs grown on bare Si (100) substrate; scale bar = 30 µm. **b–c** EDS spectra of the Si NWs and metal globules. The data show that the body of the nanowire is Si and the metal globule is an Mn-Si alloy, respectively, scale bar = 100 nm. **d** Low-magnification TEM image of rough surfaced Si NWs, scale bar = 200 nm. **e** High-magnification TEM images of rough surfaced Si NWs from top to bottom. These images indicate that nanowires are tapered along the nanowire axis, scale bars = 5 nm, 100 m, 100 nm, 100 nm, respectively. **f** SAED (selected area electron diffraction) pattern indicating that nanowires are grown in the <111> directions and are single crystalline structures

images of nanowires grown under different flow rates. H_2 gas flow rates used were 300 sccm (Fig. 2a), 2000 sccm (Fig. 2b), 2500 sccm (Fig. 2c), and 3000 sccm (Fig. 2d). Figure 2 clearly shows that the surface of the nanowires grown under low flow rates (e.g., 300 sccm) was smooth, while that of nanowires grown under high flow rates was rough. Figure 2e shows the variation in surface roughness as a function of flow rate. The definitions of diameter and roughness are shown as an inset in Fig. 2e. Roughness was measured from TEM images of nanowires using the arithmetic average method. Since the nanowires were tapered and rougher towards the bottom, the measurements were performed along the longitudinal direction of each nanowire and averaged. At a rate of 2000 sccm (linear velocity of 6.3 cm/s), the surface is smooth on an atomic scale and starts to become rough at flow rates above 2000 sccm, becoming rougher with higher flow rate. The roughness, h, was varied from smooth to 37 nm, depending on the flow rate.

As demonstrated above, Si nanowires with rough surfaces were grown successfully. The observations that (i) the diameter is tapered as a function of length and that (ii) no Mn exists in the nanowire body indicate that growth in the radial direction proceeds by the vapor-solid (VS) mechanism in the course of conventional longitudinal VLS growth. VS growth involves direct deposition of Si atoms from the vapor and is accompanied by surface roughening. Many previous studies

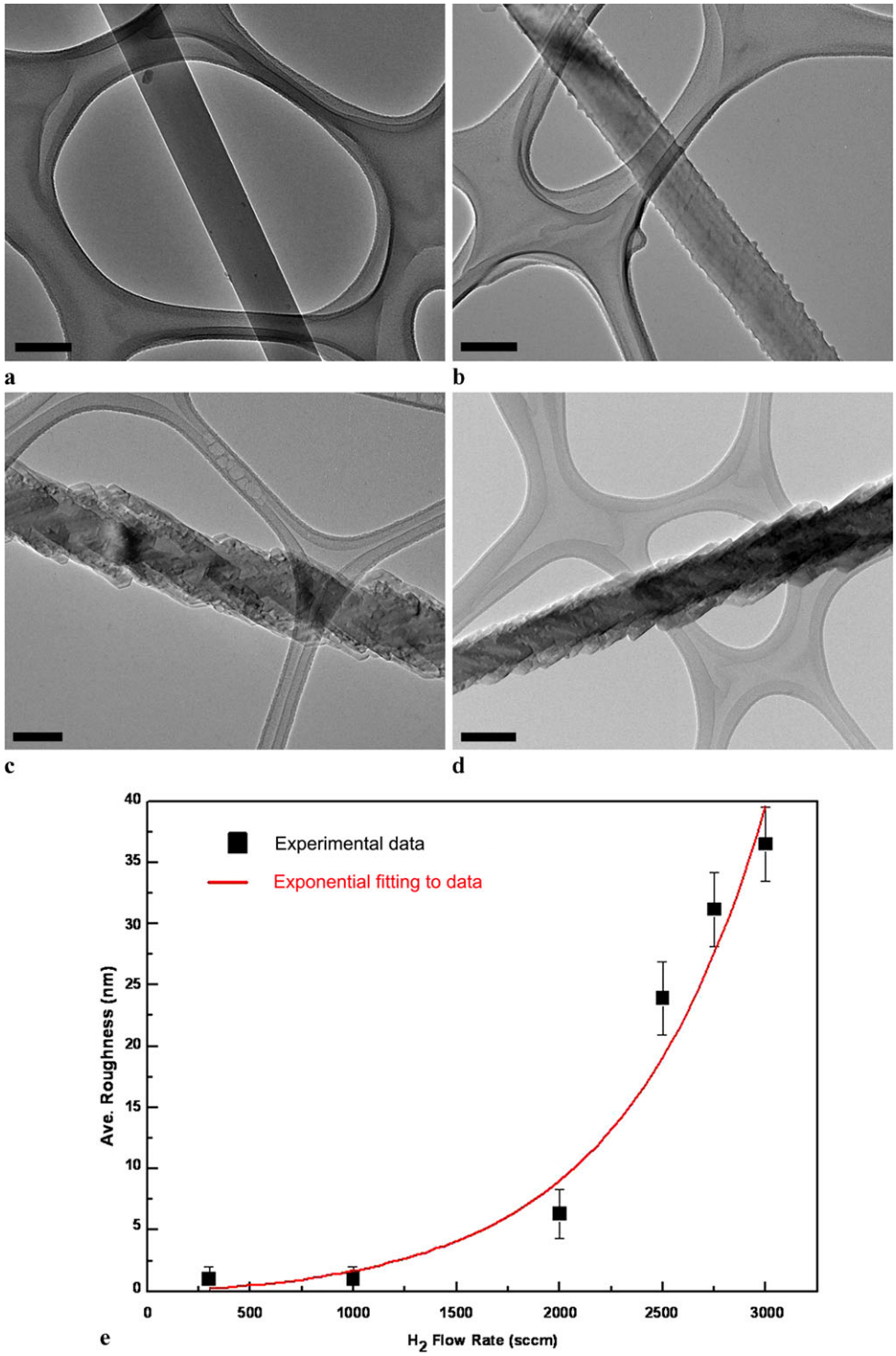

Fig. 2 **a** High-magnification image of the smooth surface Si NWs grown by conventional VLS method. The H_2 gas flow rate was 300 sccm, scale bar = 100 nm. **b–d** Surface roughnesses are varied by controlling the H_2 gas flow rate and the H_2 gas flow rate was 2000 sccm, 2500 sccm, 3000 sccm, respectively, scale bars = 100 nm, 100 nm, 100 nm, respectively. **e** Relation between the average surface roughness and H_2 gas flow rate. It is similar to a general exponential 2D growth fit. Inset shows a schematic of diameter and roughness used in this study

on the growth of Si nanowires showed no such radial VS growth observed in this study. According to crystal growth theory, VS growth on the crystalline surfaces consists of the following steps: (1) transport of atoms through the vapor phase to the crystalline surface, (2) impinging and adsorption of the atoms at crystalline surfaces, (3) sliding of the adsorbed atoms on the crystalline surfaces until they encounter thermodynamically unstable sites for adsorption, e.g., ledge sites, (4) movement of adsorbed atoms along the ledge to a kink [17] that acts as a sink for adsorbed atoms, and finally, (5) incorporation of the adsorbed atoms into the crystal at the kink. Among these steps, step (2) typically is the rate determining step under low supersaturation conditions [18], which is typical for the growth of nanowires [19]. Further-

more, the adsorption of atoms on the surface of nanowires should overcome the high chemical potential of a curved surface by the Gibbs–Thompson effect [20, 21]. Therefore, step (2) would strongly suppress radial VS growth in many of the previous studies and result in smooth surface Si NWs. However, the high flow rate of gas would enhance the adsorption rate of atoms on the crystalline surfaces by enhancing the effective collisions and impinging atoms from the vapor to the surface of the nanowires, inducing VS growth in the radial direction [22].

We also investigated the effect of a catalyst on the radial growth under high gas flow rates using Mn, Au and Pt catalysts. The longitudinal growth rates of Si nanowires varied by catalyst and was 11.9 μm/min, 5.2 μm/min and 1.3 μm/min for Pt, Au and Mn, respectively. Interestingly, radial growth was observed when the longitudinal growth rate was relatively slow. That is, this result was observed with Mn or Au but was not observed with Pt and may relate to the degree of supersaturation of reactants on the surface of the nanowires. With Pt catalyst, most of the reactants are consumed by the Pt catalyst that actively dissolves the Si atoms in the vapor, and, thus, most Si atoms are involved in longitudinal VLS growth, while few Si atoms are available for radial VS growth. On the contrary, Si atoms would be available for the radial VS growth with Mn catalyst, leading to longitudinal growth; thus, a portion of the Si atoms in the vapor phase may available for radial VS growth.

Formation of high-order side facets in the Si nanowires may also be ascribed to radial VS growth. Mn catalyst leads to growth of hexagonal nanowires (see Fig. 3a). Since the nanowires grew in the <111> direction, the sides are $(11\bar{2})$ facets that are high-order surfaces with a high density of kinks, ledges, and steps. These facets, thus, provide many preferable sites for the incorporation of Si atoms into the surface. Limited studies have shown that Si nanowires can have rough facets, formed by twins [23], Au-rich clusters [24], the absence of a stable orientation parallel to the wire growth direction, and dopants [25]. However, our nanowires have a stable growth orientation and showed no twins, Mn clustering, or dopants.

During the course of crystal growth, faceting can occur to minimize the surface energy by exposing facets having low surface energy [26]. This faceting depends on the γ^{sv} (solid/vapor surface energy) that varies with their orientations. In this study, the radial growth precedes in <112> direction and, thus, it will expose [112] facets. However, the [112] facets may have high surface energy. In case of Si, the Wulff construction indicates that the equilibrium crystal structures are consistent with a combination of lowest surface energy facets, i.e., the {111} and {100} planes along the <110> axis [26]. Meanwhile, our TEM characterization, as shown in Fig. 3b, c, indicates that the nanowires have

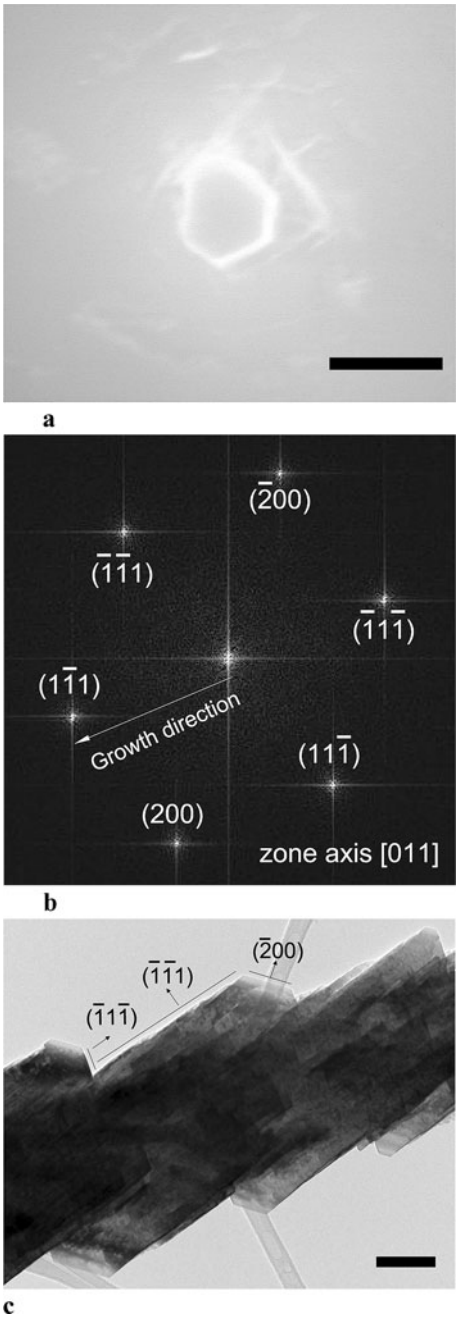

Fig. 3 **a** Typical SEM top-view image of rough surfaced Si NWs grown on Si (100) substrates. The side facets consist of <112> planes and an irregular hexagonal shape. **b** A FFT (fast Fourier transform) pattern of the rough surfaced Si NWs side facets grown in the <111> direction. **c** Rough surfaced Si NWs side facets consist of {111} and {100} planes to minimize the surface energy of the side facets; scale bar = 100 nm

[111] and [100] facets which show the lowest surface energy among the Si facets (1.23 and 1.36 J/m^2, respectively). These facets may have lower surface energy than the [112] facets and, thus, can minimize the surface energy. Therefore, surface energy minimization would drive roughening during the course of radial VS growth.

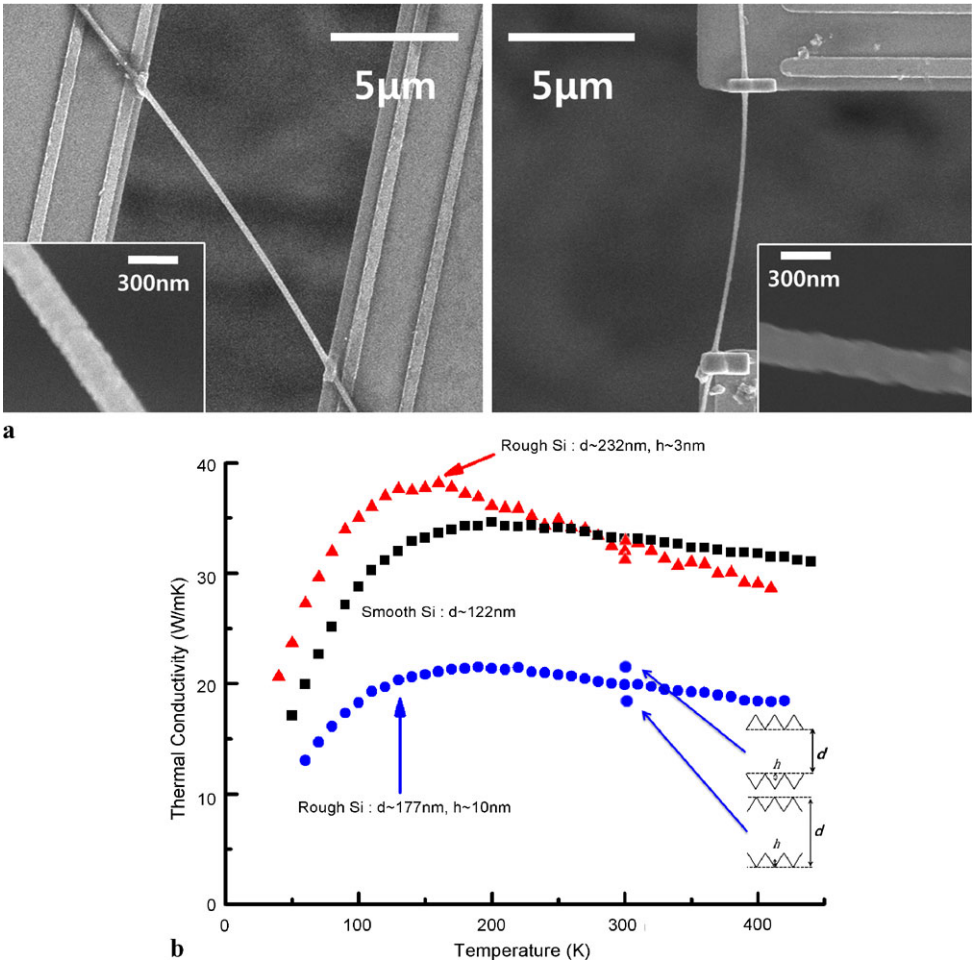

Fig. 4 **a** SEM images of VLS-grown rough Si nanowires on the membrane for thermal conductivity measurement. **b** Temperature dependent thermal conductivity of rough Si NWs with different roughnesses and diameters. Thermal conductivity of smooth surfaced NWs is shown for reference

Figure 4a shows SEM images of VLS-grown rough Si nanowires on the membrane for thermal conductivity measurement. The distance between membranes is 10 μm. This is five times larger than that in previous devices [2, 3, 14]. Therefore, effects of thermal contact resistance should be smaller compared with those of previous studies. Pt/C had been thoroughly deposited on the contact area of the nanowire to improve thermal contact. Also, thermal contact resistance of Si NWs has been estimated based on the study by Yu et al. [27] and was found to be negligible. Figure 4b shows thermal conductivities of rough Si NWs with various roughnesses and diameters in the temperature range of 40 to 420 K. The rough NWs have roughness, h, and diameter, d, where $h = 3$ nm & $d = 232$ nm and $h = 10$ nm & $d = 177$ nm. Thermal conductivities of smooth NWs with a diameter of 122 nm are shown for reference. In the measurement, we are measuring thermal conductance. Thermal conductivity of NWs is extracted based on this measured thermal conductance. Therefore, thermal conductivity of rough Si NWs should be different based on how the surface roughness and diameter are defined. The way we defined these parameters are shown as an inset in Fig. 2e. Also, we indicated as dots in the thermal conductivity at 300 K when two extreme cases of defining the surface roughness and the diameter. Since thermal conductivity is extracted based on measured thermal conductance, depending on how to defining diameter of NWs, different thermal conductivity can be deduced from the same NWs. As shown in the figure, both the surface roughness and diameter of NWs affect thermal conductivity. The fact that thermal conductivity decreases with reduced diameter is well known [5]. What is surprising in Fig. 4b is that (1) increasing surface roughness significantly reduces the thermal conductivity of NWs and (2), although thermal conductivities of NWs depend both on the surface roughness and diameter, the surface roughness affects thermal conductivities of NWs more strongly. This can be readily observed by comparing thermal conductivities of smooth 122 nm NWs with those of rough 232 nm NWs. Even though the diameter of rough 232 nm NWs are almost twice that of smooth 122 nm NWs, the thermal conductivity of rough 200 nm NWs is comparable with that of smooth 122 nm NWs. Also, in this case the surface roughness, h, is only 3 nm, yet thermal conductivities of two NWs are comparable. Also, the same principle can be applied based on the comparison between smooth 122 nm NW

and rough 177 nm NW. The diameter of rough 177 nm NW is larger than that of smooth NW but thermal conductivity is way lower than that of smooth nanowire. In fact, our recent paper on thermal conductivity of rough $Si_{0.96}Ge_{0.04}$ nanowire [28] suggested that surface roughness scattering scatters mid-wavelength phonons, whereas phonon boundary scattering affects long-wavelength phonons. Therefore, the surface roughness reduces thermal conductivity of rough 177 nm NW significantly. Also, temperature dependency of thermal conductivity is different due to the magnitude of surface roughness. Although for all NWs the thermal conductivity decreases at high temperature, indicating that the Umklapp scattering begins to dominate over other scattering processes, this behavior is more significant in the thermal conductivity of NWs with 3 nm in roughness. This is suspected because of rather large diameter, i.e., long phonon mean free path due to the boundary scattering, and small surface roughness, i.e., long phonon mean free path due to the surface roughness.

Both smooth and rough nanowires were grown the same VLS process but with different catalyst, i.e., Au for the smooth nanowire and Mn for the rough nanowire. Although previous studies [2, 13] also showed that thermal conductivity of rough Si nanowires is significantly lower than that of smooth Si nanowires, those nanowires were synthesized by a different method, VLS for smooth Si nanowires and electroless etching for rough Si nanowires. Thermal conductivity usually depends on the growth parameters, such as growth temperature [29]. Therefore, this study confirmed that, indeed, surface roughness is an important parameter for thermal conductivity reduction.

4 Conclusion

Si nanowires were grown using Mn catalyst under high carrier gas flow rate. These conditions enable the growth of Si nanowires by a combination of VLS and VS mechanisms for the longitudinal and radial growth dimensions, respectively. In the course of radial growth, a rough surface was developed by exposing (111) and (100) facets to minimize the surface energy of the nanowires. Thermal conductivity of rough Si nanowires is significantly lower than that of smooth Si nanowires, even when the diameter of the smooth nanowire is smaller than that of the rough nanowire. Both smooth and rough nanowires were grown with the same VLS process; therefore, thermal conductivity dependency over the growth temperature is not an issue in such cases. These outcomes demonstrate that the surface roughness affects thermal conductivity of NWs more significantly than the diameter of the NWs. Growing rough Si nanowires by combinatorial VLS and VS mechanisms holds promise for both the development of Si-based thermoelectric devices with high figures of merit, as well as furthering a fundamental understanding of thermal conductivity.

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