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Inherent diode isolation in programmable metallization cell resistive memory elements

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Abstract The feasibility of a storage element with inherent rectifying or isolation properties for use in passive memory arrays has been demonstrated using a programmable metallization cell structure with a doped (*n*-type) silicon electrode. The Cu/Cu–SiO_2/*n*-Si cell used in this study switches via the formation of a nanoscale Cu filament in the Cu–SiO_2 film which results in the creation of a Cu/*n*-Si Schottky contact with soft reverse breakdown characteristics. The reverse bias leakage current in the on-state diode is dependent on the programming current employed as this influences the area of the electrodeposit and hence the area of the Cu/*n*-Si junction. The programming current also controls the on-state resistance of the device, allowing multi-level cell (MLC) operation, in which discrete resistance levels are used to represent multiple logical bits in each physical cell. The Cu/Cu–SiO_2/*n*-Si elements with heavily doped silicon electrodes were readily erasable at voltage less than −5 V which allows them to be re-programmed. Lightly doped silicon electrode devices were not able to be erased due to their very high reverse breakdown voltage but exhibited extremely low leakage current levels potentially allowing them to be used in low energy one-time programmable arrays.

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1 Introduction

The semiconductor industry has generally accepted that arrays based on a crossbar architecture will be a cost effective approach to ultra-high density memory and solid state storage in the sub-20 nm regime [1]. Such systems have an extremely simple structure, with a compact two-terminal storage cell being located at each crossing point of multiple perpendicular (row and column) conducting lines. Not only is it possible to reduce cell area to its minimum possible value ($4F^2$, where F is the minimum feature size), it might also be feasible to construct multiple layers of cross-point devices, thereby attaining extremely high storage densities. Resistance-change devices show great promise as storage cells in these architectures as they can possess many of the attributes required of next generation memory and are generally compatible with the crossbar approach. Resistance switching has been reported in a variety of materials and structures, and the switching mechanisms range from thermal and electronic effects to ionic effects. The many systems which show resistance switching and their switching mechanisms have been well reviewed elsewhere [2].

The main challenge in integrating a resistance-change memory cell in a crossbar architecture is minimizing crosstalk via leakage paths, which is an inherent disadvantage of this architecture. An example of such a leakage path is when two adjacent cells in the same row are programmed to be in a low-resistance state. Although the cells are in different columns by virtue of the crossbar architecture, their low resistance effectively links the columns together via the common row connection. Taking this to the worst case, low-resistance cells could connect every row and every column in the array, making it difficult or impossible to access individual devices or, at the very least, severely limiting the size of the array. The obvious solution to this problem is to

put an isolation device in series with the memory element at each cross-point. In current memory arrays, this device is typically a transistor which is fabricated in the silicon substrate, however, this reduces the ability for the array to be fabricated in multiple layers in the upper levels of metal in the integrated circuit. Research in this area has therefore concentrated on simple thin-film diode elements in series with each cell, which in the example above will not allow column-to-column connection as one of the diodes will be reverse biased, cutting-off the current path. Such transistorless (at least at the memory cell level) diode-isolated architectures are typically called "passive" arrays.

The desired characteristics of the diode isolation element are good process compatibility, large rectification ratio, and current capacity high enough to write and erase the memory cell. Amorphous Si-based diodes may be fabricated during back-end-of-line (BEOL) processing at low temperature but are generally not favored due to their low current capacity [3]. Heterojunction diodes based on oxides appear to be preferred over Si-based diodes as they have more ideal characteristics but typically involve the deposition of multiple additional layers. Another approach is to use a memory element with inherent rectifying characteristics to simplify the fabrication process which in turn leads to lower fabrication cost, a critical factor in ultra-high density storage applications where the solid state system may be competing with the extremely low cost-per-bit of hard disk drives. Previously reported work concentrated on memory cells for write-once-read-many (WORM) applications, usually with a semiconductor–insulator–semiconductor or metal–insulator–semiconductor structure [3, 4]. Electric fields in the range of a few MV/cm are applied to break down the insulator to form a rectifying junction. Since the programming process is irreversible, application has been limited to one-time programmable (OTP) memories but the approach has nevertheless demonstrated the feasibility of multi-layer crossbar memories. This paper presents the initial results and analysis of a resistance-change memory cell with inherent rectification properties. Our memory element falls under a class of resistance switching devices called Programmable Metallization Cells (PMC) [5] also known as Conductive Bridging RAM (CBRAM) [6]. In these devices, the switching to the low-resistance state occurs by migration of metal cations in a solid electrolyte under the influence of an applied electric field and the reduction of these cations to form an electrodeposited metallic link between two electrodes. The process is reversible by applying a bias opposite to that used for the write operation, thus oxidizing the electrodeposit back into an ionic state and returning the device to its high-resistance condition. This "bipolar" operation (different polarity for write and erase) allows the devices to be written and erased at low energy, an attribute that is not seen in "unipolar" devices which typically require a high current for erase (also called "reset" in these devices). PMC devices based on germanium-chalcogenides or tungsten oxide combined with Ag or Cu have yielded promising results as next generation memory elements [7, 8]. Devices based on Cu and SiO_2 have also been studied due to the ease of integration of these materials in CMOS technology [9] and their potential as a non-volatile memory alternative in terms of low-power switching, speed, retention, and endurance, has been discussed elsewhere [10, 11]. The main disadvantage of all PMC memory devices in re-programmable crossbar applications is their bipolar operation, as a series diode with a high reverse resistance would not allow a sufficient bias across the device element to permit the erase operation. It is therefore necessary to use a Zener or a soft breakdown diode that will allow both cell isolation and sufficient reverse bias current for erase at an appropriate voltage. Such an approach has been defined by others using discrete Zener diode elements with PMC-like devices [12] but a memory element with an inherent reverse breakdown diode has not been reported to date. We describe such a device in this paper.

2 Device fabrication

The memory cells presented in this paper are based on a thin film (15 nm) of high-resistivity Cu-doped SiO_2, sandwiched between a copper top electrode which supplies Cu ions during the write operation, and a bottom inert electrode which supplies electrons during programming. It is believed that it is the reduction of the Cu ions in the SiO_2 by the electrons that results in the formation of the Cu filament which defines the on-state of the device. Our choice of Cu–SiO_2 for the switching layer was to ultimately allow temperatures up to the mid-600°C range to be used in BEOL processing [13]. In our previous work, the inert electrode was tungsten [13]. Figure 1 shows a typical current–voltage (I–V) plot of such a Cu/Cu–SiO_2/W device. In this plot, the voltage is swept from 0 V to 1.5 V and the device switches from its off-state resistance, R_E, of 1 GΩ to its on-state resistance, R_F, at approximately 0.45 V (arrows 1, 2 and 3 in the figure). Note that R_F is inversely proportional to the current limit in PMC devices [10]. This dependence of on-state resistance to the magnitude of programming current can allow multi-level cell (MLC) operation, in which discrete resistance levels are used to represent multiple logical bits in each physical cell [14]. The constant of proportionality in this case is 0.18, leading to an on state resistance of 7.2 kΩ for the 25 μA current limit used. The voltage is then swept from 1.5 V to −1.0 V (arrows 4, 5, 6, 7, 8) and the device switches to a high-resistance state around −0.1 V.

To assess the viability of using a bipolar device with a series diode, a discrete Zener diode with a −3.3 V reverse

breakdown voltage was connected in series with a well-characterized Ag/Ag–Ge–S/W cell [5] and the I–V plot for this combination is given in Fig. 2. As is evident from the plot, the device switches to its compliance current-limited written state at nearly 1 V, which is considerably higher than the 450 mV write threshold without the diode. The

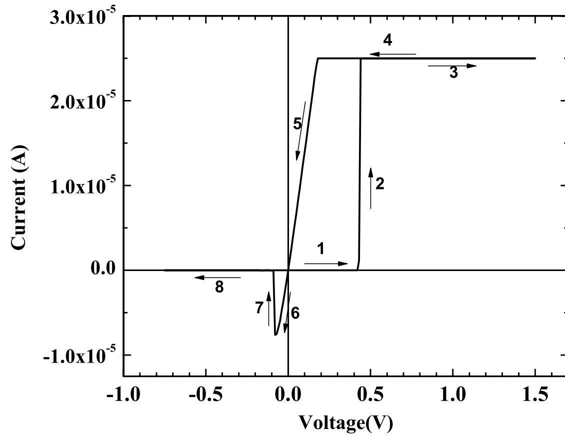


Fig. 1 Current–voltage plot for a $Cu/Cu–SiO_2/W$ device showing off-state resistance to on-state resistance switching at 0.45 V and switching back to the off-state resistance at −100 mV

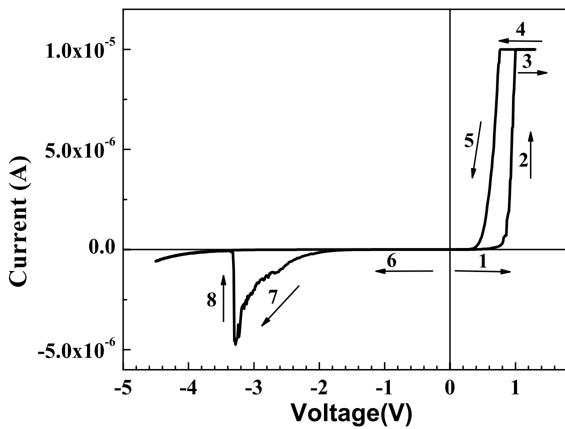
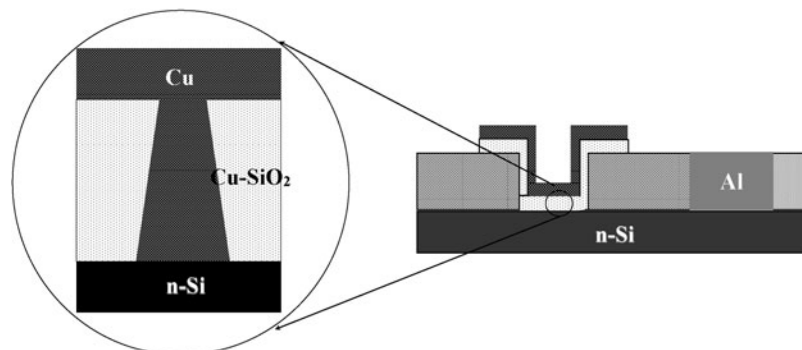


Fig. 2 Current–voltage plot for a series combination of a Ag/Ge–S/W memory cell and a discrete Zener diode

forward biased diode characteristic is clear when the device is in its low-resistance state and it is evident that the turn-on voltage of the diode leads to the increase in write voltage. As expected, even though the device is in its low-resistance state, the current flow under negative bias is small (<10 nA at -1.5 V) due to the influence of the diode but rises rapidly when the bias approaches its breakdown voltage at -3.3 V, at which point the diode conducts and the memory cell switches to its high-resistance state. Note that this series combination would be written at 1 V and read between the knee voltage of the diode and the programming voltage (e.g., at 0.7 V) so that the off- and on-states may be readily distinguished without disturbing the off-state. The above result indicates that a separate Zener diode can be used to provide current blocking at low voltage, i.e., at the voltages used for writing or reading devices, but will still allow the erase operation to occur at higher bias. However, the goal of this work was to create a built-in diode as part of the cell and this involved a modification to the inert electrode material. Specifically, we elected to use n-type silicon (n-Si) rather than tungsten as the bottom electrode (cathode) in a $Cu/Cu–SiO_2/n$-Si device to produce a rectifying effect. The proposed principle was simple; the interface between the Cu filament in the on-state of the PMC device and the n-Si electrode would constitute a Schottky diode with soft reverse breakdown without the need for additional device layers. Note that our intent was not to create a crossbar array at this time but to assess the feasibility of this approach and characterize the diode element formed. For this work, two batches of samples were fabricated, the first with a high substrate doping density of 10^{18} cm^{-3} (Sb-doped) and the second with an epitaxial layer of low doping density 5×10^{14} cm^{-3} (P-doped) in order to provide device data over a wide dopant concentration range. The sample schematic is shown in Fig. 3. The Cu filament that forms in the WRITE step (discussed in more detail later) is shown in the inset. In the device fabrication process, we started by growing 200 nm of SiO_2 on the Si substrate by a wet oxidation process. The lithography process involved two masks, the first one defined the vias ranging from 2 μm to 8 μm in diameter through the oxide, and the second mask patterned the

Fig. 3 The schematic of a $Cu/Cu–SiO_2/n$-Si programmable metallization cell. *The inset* shows the schematic view of the Cu filament formed after WRITE step



top electrode. Just before loading into the deposition tool, the samples were dipped in a 20:1 buffered oxide etchant solution for 30 seconds to remove any native oxide formed in the vias on n-Si electrode surface. Then, 15 nm of SiO_2 and 35 nm of Cu were deposited using physical vapor deposition in a Torrvac e-beam evaporator. The samples were annealed at 660°C for 15 min in a flowing N_2 ambient to drive the Cu into the SiO_2 to form the solid electrolyte [13]. Al was then deposited and patterned to form contact pads to the bottom of the n-Si substrate after a wet-etch of the SiO_2 dielectric. Two control samples were also fabricated using similar processing conditions. The control samples did not contain the 15 nm oxide film so that the Cu made direct contact with the n-Si material for each doping density mentioned above. These are effectively Cu/n-Si metal semiconductor interfaces with interface diameter defined by the vias and were used for extraction of diode leakage parameters (see later). The Cu/n-Si metal semiconductor interface sample with the highly doped silicon electrode was called control sample A and that with the low doped electrode control sample B.

3 Characterization

The devices were connected to the electrical characterization equipment via tungsten probes held by micro manipulators in a probe station. A semiconductor parameter analyzer (Agilent 4155C) was used to apply slow voltage sweeps to create the current–voltage (I–V) and resistance–voltage (R–V) plots. Separate WRITE (0 V to 6.5 V and back to 0 V), READ (500 mV) and ERASE (0 V to −6.5 V) sweeps were used to record the switching characteristics. During the WRITE sweep and READ operation, the Cu top electrode was positively biased compared to the n-Si bottom electrode and vice versa during the ERASE sweep. The compliance current (programming current) setting in the 4155C was used to limit the current passing through the device after the device was written. Measurements were made at 5°C, 15°C, 25°C and 35°C.

4 Results and discussion

Figures 4a and 4b show typical WRITE and ERASE switching characteristics, respectively, of two Cu/Cu–SiO_2/n-Si-based cells with the two different n-Si electrode doping densities. The voltage sweep direction and sequence of events are shown by numbered arrows. In Fig. 4a, both devices are initially in their high-resistance state (R_E) in region 1 of the WRITE sweep. As shown in the inset, R_E for the highly doped Si case is in excess of 10^8 Ω and the lightly doped Si device has R_E above 10^{10} Ω (which is above the limit of the measurement apparatus). The higher R_E for the substrate devices with the low doped cathode is due to a combination of factors such as a higher series resistance due to the lightly doped electrode and also a larger barrier for electron tunneling at the SiO_2/Si interface. The band bending at the interface is expected to be higher for the highly doped n-Si substrate, resulting in a narrow barrier for electrons to tunnel and leading to a lower resistance. The switching to the low-resistance state is seen at region 2. The initial switching threshold (V_t) is in the order of 3.25 V and 3.75 V for the light and heavy doped Si cases, respectively. The V_t values did not show any significant trend between the two sets of samples and the recorded values from multiple devices typically lay within a ±10% range from a mean value. Similar variation, albeit at a lower threshold voltage, was observed in Cu/Cu–SiO_2/W based cells and is believed to be due to variations in free Cu concentration in the SiO_2 matrix [13]. The programming (compliance) current limit (I_{prog}) in both cases was 50 μA and the current through the devices remains at this value in regions 3 and 4, indicating that the memory cells are in their low-resistance state (R_F). The actual value of R_F is masked by the current limit circuitry in the

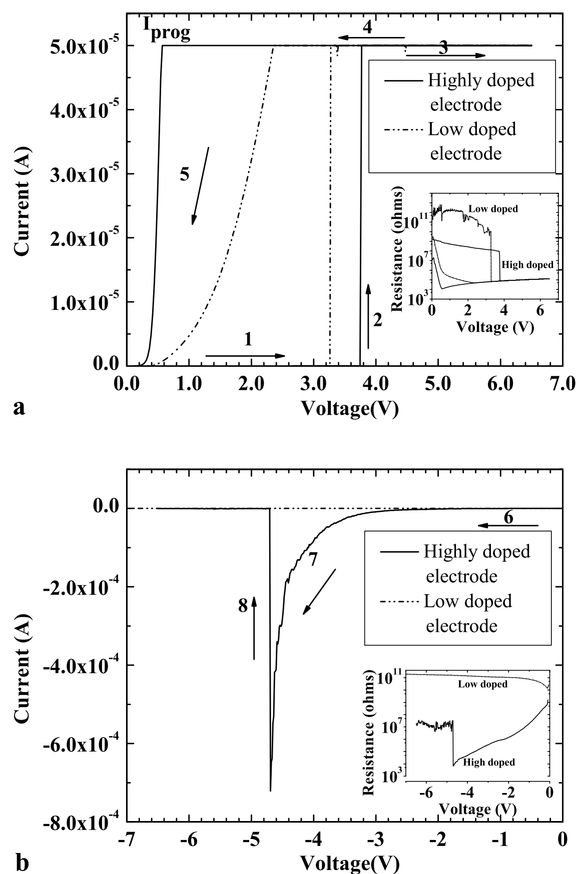


Fig. 4 Switching characteristics of Cu/Cu–SiO_2/n-Si devices with two different doping densities for the bottom electrode. (**a**) 0 V–6.5 V WRITE sweep; (**b**) 0 V–(−6.5 V) ERASE sweep. The corresponding resistance–voltage plot is shown *in the inset*

semiconductor parameter analyzer, which manifests itself as the rising R–V curves at higher voltage in the inset. However, the lowest R_F values observed were around 10 kΩ and 50 kΩ for the heavy and light doped Si cases, respectively, more than four orders of magnitude lower than R_E. Region 5 is where the voltage drop across the devices is low enough to cause the current to decrease below the compliance limit. Both devices show distinctly non-ohmic characteristics in this region, which is quite different than the Cu/Cu–SiO_2/W device of Fig. 1, which shows ohmic characteristics for the on-state with the metal bottom electrode. These non-ohmic I–V characteristics are expected in a rectifying contact and also add an additional series resistance component, which doubtless leads to the higher R_F in the lightly doped Si case. During the ERASE sweep, the devices behave like a rectifier in reverse bias, a further indication that we have indeed created an inherent diode structure in the on-state. The rectification action can be seen in region 6 in Fig 4b. The Cu/Cu–SiO_2/W device in Fig. 1 shows no such current blocking in the equivalent region. The rectifying nature can be quantified by a reverse bias to forward bias resistance ratio for a constant voltage magnitude. From Fig. 4, this ratio is on the order of 10^4 for $|V| = 500$ mV for the Cu/Cu–SiO_2/n-Si-based device with a highly doped n-Si bottom electrode. The highly doped Si device begins to conduct in region 7 and then switches back to the high-resistance state at region 8 in a similar fashion to the discrete Zener diode case shown in Fig. 2, but in this case the ERASE voltage is closer to -4.75 V. Note that R_E for a negative bias beyond the ERASE voltage is in the order of 10^7 Ω. This value is lower than the forward bias R_E due to the leaky nature of the off-state device at these relatively high voltages. Interestingly, the lower doped n-Si electrode device does not conduct under negative bias and a transition to its high-resistance state is not observed over the voltage range used (this will be discussed in more detail later).

The rectification observed in these devices can be understood by considering the switching mechanism in a Cu-based PMC device. In a Cu/Cu–SiO_2/W device, the low-resistance state formed by the electrodeposition of a Cu filament results in a Cu–W contact at the lower electrode which leads to the observed ohmic characteristics (Fig. 1). However, in the case of the n-type Si device, a metal–semiconductor junction is formed at the bottom electrode. The forward bias characteristic of the heavily doped Si device after the Cu electrodeposit is formed, as shown in Fig. 5, reasonably fits the Schottky diode equation with a non-ideality factor n of 1.65. The decrease in the current from ideal can be observed at voltages of around 300 mV and higher, and is most likely due to the series resistance in the circuit. The series resistance extracted from this difference in current is approximately 4 kΩ, which is in the range of the expected on-state resistance of the device for the programming current used [10].

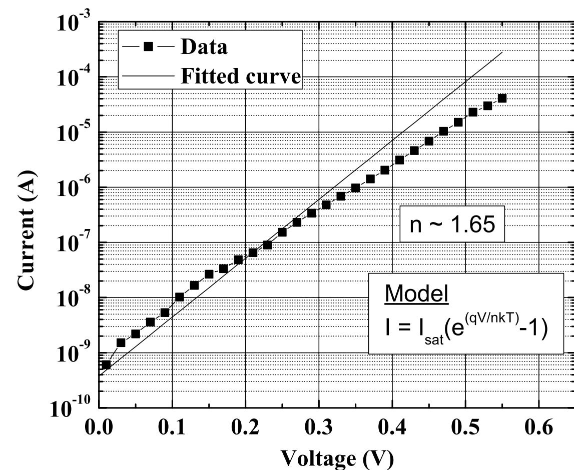


Fig. 5 Forward bias curve obtained from a Cu/Cu–SiO_2/n-Si device after forming the filament with a WRITE sweep. The curve is fitted to an ideal-diode equation with a non-ideality factor, $n \approx 1.65$

During the ERASE sweep, the heavily doped Si device behaves like a reverse biased Schottky diode. The increase in current for higher negative bias voltage resembles the soft breakdown characteristics shown by Schottky devices on highly doped semiconductors. The substrate doping density is in the range of 10^{18} cm^{-3} for which the onset of soft breakdown is expected at around 3 V [15] which is consistent with the results shown in Fig. 4b. Based on this, we propose that the current in this regime is mainly due to tunneling of electrons across the metal–semiconductor barrier leading to the soft Zener breakdown.

When the current and resultant voltage drop across the cell is sufficiently high, the dissolution process of the electrodeposit is initiated. This erase process is believed to be similar to that of a metal bottom electrode device but occurs at a much larger voltage due to the influence of the reverse biased Schottky junction which limits the current flow until it breaks down. However, once the electrodeposit is dissolved, the diode is "disassembled" and the device behaves as a normal PMC element in its off-state. The reverse breakdown voltage for the n-Si electrode that was doped to 10^{15} cm^{-3} is expected to be in excess of 100 V [15]. Consistent with this, these devices showed very low conduction in reverse bias and no breakdown characteristics were observed up to -40 V (the maximum that could be applied due to equipment limitations). This high breakdown voltage is the reason these devices could not be erased in the same voltage range as their more heavily doped counterparts. The rectification ratio was not measured in this case as the conduction at -500 mV was below the resolution limit of the equipment but it was clear that the rectification ratio was much higher than in the highly doped Si electrode case.

Figure 6 shows a simple circuit model of the erased and written states of a Cu/Cu–SiO_2/n-Si memory cell. In the

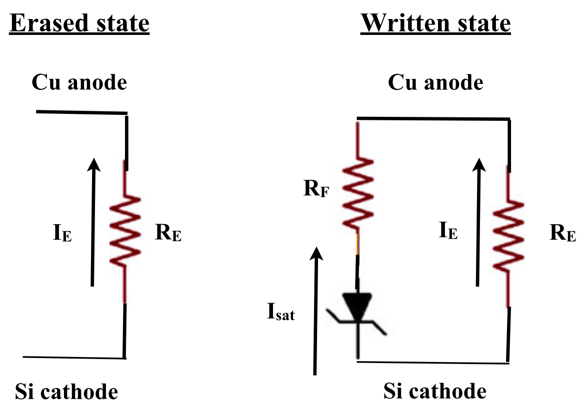


Fig. 6 A simple circuit model showing the erased and written state of the Cu/Cu–SiO_2/n-Si with the erase state leakage current (I_E) through the electrolyte and the leakage current (I_{SAT}) through the diode element being formed after the WRITE sweep

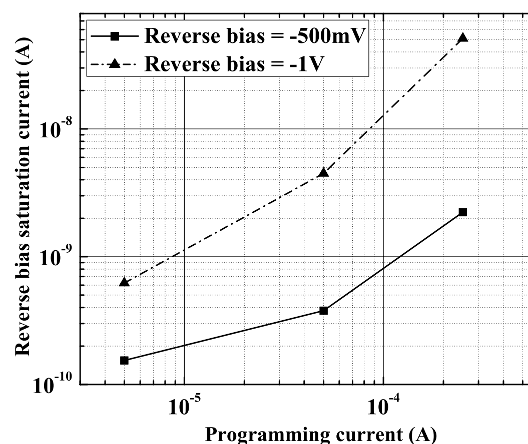


Fig. 7 Data showing the trend in the reverse bias saturation current (I_{SAT}) with different programming currents (I_{prog}), for reverse bias voltages −0.5 V and −1 V in a Cu/SiO_2/n-Si cell with a bottom electrode doping density of 10^{18} cm^{-3}

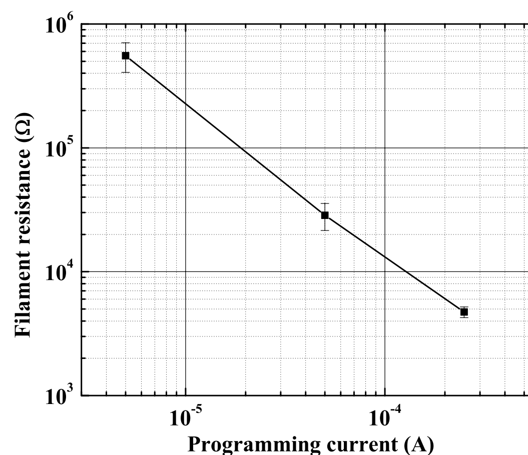


Fig. 8 The filament resistance (R_F) measured for three different programming currents (I_{prog}). R_F was measured at 90% of the I_{prog} value in each case and error bars show the median of the deviation across devices

erased state, the off-state resistance R_E is determined by the Cu-doped SiO_2 electrolyte and its interfaces with the electrodes. R_E will generally scale as the inverse of the device area which is determined by the size of the via in the dielectric. In the written state, R_E is still present but it is now in parallel with the Cu filament resistance, R_F, in series with the Schottky diode created at the filament—Si interface. The leakage current through an unwritten device, I_E, is determined by R_E and the applied bias; in our experiments, an average I_E of 5 nA was obtained for a 6 μm diameter device for a 500 mV READ voltage and was about a factor of 10 higher for −1 V reverse bias. Since I_E depends on device area, this will reduce to around 50/500 fA in a 20 nm device at ±1 V, assuming all other device parameters, such as film thickness and composition, stay the same. Reduction of the off-state current is important as not only will it increase the R_E/R_F ratio, thereby simplifying the sensing of the state, but also because this leakage path could affect the current through another cell in the same row or column which is being addressed if R_E was too low.

In a written device, there is an additional leakage path during reverse bias through the Cu filament/n-Si interface. This component is the reverse bias saturation current (I_{SAT}) of the diode element. Hence, in a written device I_{SAT} and I_E together constitute the total leakage current. To determine I_{SAT} from the total leakage current of a written device, it was assumed that I_E remains constant between a written and an erased device. This is a reasonable assumption as the formation of the nanoscale electrodeposit should not significantly affect the conductivity of the rest of the film in a via with a diameter in the order of a few microns. The total leakage current was measured in devices with a highly doped n-Si bottom electrode written using compliance currents of 5 μA, 50 μA, and 250 μA. The measurements were performed at room temperature at reverse bias voltages of −500 mV and −1 V. I_E was measured at the same voltages in unwritten devices and the average value was subtracted from the average total reverse bias leakage current in the written device to obtain I_{SAT}.

The data of Fig. 7. reveal a rising trend in I_{SAT} with increasing I_{prog} at the two measurement voltages. As mentioned previously, in Cu/Cu–SiO_2/W devices and, for that matter, all other PMC variants with metal bottom electrodes, it has been shown that higher programming current results in an electrodeposit with lower resistance and the relationship between R_F and the current limit is inverse linear [10]. The mechanism behind this relationship has been discussed elsewhere [16] but the assumption is that a larger I_{prog} results in an electrodeposit with a larger effective cross-sectional area. The Cu/Cu–SiO_2/n-Si device data shown in Fig. 8 show the same relationship. The data were obtained from five differ-

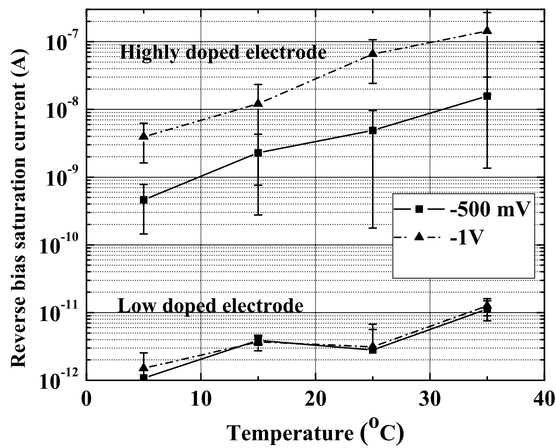


Fig. 9 Reverse bias saturation current (I_{SAT}) measured at four different temperature values on the Cu/Cu–SiO_2/n-Si samples with high and low doped bottom electrode. The error bar shows the median of the deviation across different devices

ent devices for each programming current. Resistance was measured at a current value equal to 90% of the I_{prog} to ensure that the diode formed at the interface is completely conducting in forward bias and that the measured resistance is close to the true resistance of the filament (R_F). Each device was subjected to at least 10 consecutive WRITE and ERASE voltage sweeps and an R_F measured for each such cycle. The variation in R_F across cycles was found to be less than 20% for each device. The almost two orders of magnitude range in the on-state resistance with reasonable controllability indicates that the Cu/Cu–SiO_2/n-Si devices are indeed capable of MLC operation.

If we are to assume that the same increase in the effective area of the electrodeposited filament occurs with increasing I_{prog} in the Cu/Cu–SiO_2/n-Si devices, the increase in I_{SAT} with programming current is not surprising. A larger area Cu filament will result in a larger junction area between the Cu filament and the n-Si electrode and this in turn will increase I_{SAT}. The exact relationship between I_{SAT} and I_{prog} is a subject for further research as, taking the simplest analysis, the effective cross-sectional area of the electrodeposit and the resultant saturation current should be proportional to the programming current. However, the data of Fig. 7 show that for a 50× increase in programming current (5 μA to 250 μA), there is only a little over 10× increase in I_{SAT} at 500 mV but almost 100× increase at 1 V. This suggests that other factors, such as edge effects and perhaps even the morphology and composition of the Cu filament formed at different currents, could also contribute to the reverse bias leakage.

I_{SAT} was measured for two reverse bias voltages at four temperatures for both high- and low-doped n-Si bottom electrode samples. The programming current limit in this case was fixed at 50 μA. At least five different devices were tested at each temperature for both levels of Si doping. Figure 9 shows the median I_{SAT} value obtained across the multiple devices and the error bar illustrates the median of the absolute deviation in data between devices. From the figure, I_{SAT} shows a clear dependence on the doping density of the bottom Si electrode. As expected, lower doping density gives lower leakage currents, but as mentioned before, the ERASE voltage is much higher and so this is obviously a point of compromise in device applications. In the highly doped n-Si-based devices, the leakage current increases significantly with the reverse bias voltage whereas there is little difference with voltage in the case of the lower doped Si. In the higher doped material, tunneling of electrons through the Cu/n-Si barrier from the metal side can be a significant component in the reverse bias saturation current in addition to thermionic emission. The tunneling component is proportional to the electric field and hence will rise with applied voltage, whereas, in lower doped substrates the leakage current is mainly due to thermionic emission which is little influenced by the electric field but is a strong function of temperature, as can be seen in the data of Fig. 9.

The saturation currents obtained at different temperatures were used to extract the barrier height for the Cu/n-Si interface as follows.

1. The R_F of the device after writing was determined from the forward bias characteristics of the cell at a current of 90% of the I_{prog} (50 μA). Resistance measurement at relatively high current was necessary due to the non-ohmic device characteristic in forward bias. The resistance had to be measured in the region where the series resistance due to the electrodeposit dominates rather than that of the diode element (measurement in the diode-dominated region gives an abnormally high series resistance).
2. R_F was used to extract an effective area for the Cu/n-Si interface using a truncated cone model approximation for the shape of the electrodeposit [17], as shown in the inset of Fig. 3. Based on this geometrical model,

$$R_F = \rho \frac{H}{\pi r(r+H)} \tag{1}$$

where ρ is the resistivity of Cu in the electrodeposit, H is the height of the cone and r the radius of the smallest cross-section of the cone which, in PMC devices is assumed to be near the top (Cu) electrode end as the electrodeposit nucleates and grows out from the bottom electrode [18]. The filament resistivity will be higher than the resistivity of bulk crystalline Cu due to additional scattering parameters, primarily grain boundaries and surface morphology. The resistivity is assumed to be approximately eight times higher than the bulk resistivity of 1.67 μΩ-cm by the model proposed in [19]. Based on the above approach, the effective area at the Schottky interface is calculated to be in the order of 180 nm^2 for

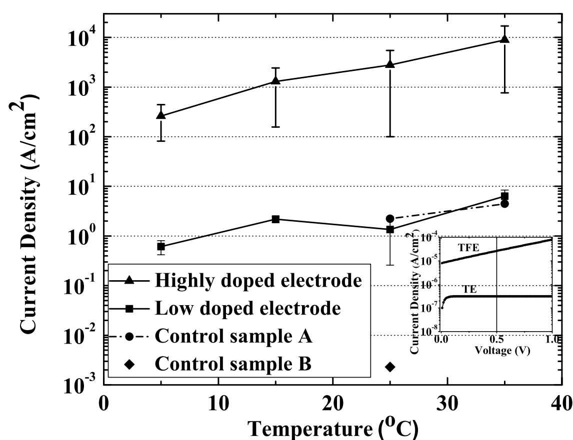


Fig. 10 Reverse bias saturation current density calculated for four different temperatures based on the reverse bias saturation current measured at −500 mV and the effective area values. *The inset* shows the simulated current density values for a Cu/n-Si interface based on the diode equations for thermionic field and thermionic emission

50 μA programming current (i.e., an effective radius of approximately 7.6 nm).

3. The effective area was used to convert the saturation current to current density. Figure 10 shows the current densities obtained for a reverse bias voltage of −500 mV. The tunneling current component at the Cu/n-Si interface in the highly doped Si device is via thermionic-field emission (TFE) and results in a reverse bias current which is at least two orders of magnitude higher than that of the low-doped Si device where thermionic emission (TE) alone is the major contributor to leakage. To verify whether the TFE mechanism can be responsible for such a large increase in current over the TE mechanism, standard reverse bias Schottky diode equations for each of these mechanisms were plotted for the relevant voltage range. The plots are shown in the inset of Fig. 10, and it may be seen that at a reverse bias voltage of −500 mV, the current due to TFE is indeed at least two orders of magnitude higher than that in the TE case. However, it has been shown that to experimentally obtain the actual current density values predicted by the ideal-diode equations, device structures using diffused guard rings are necessary [20]. Hence, a comparison of the actual current density values obtained from the Schottky interfaces formed in these devices to that predicted by ideal-diode equations is not justified. Thus, a comparison has been made to current density values obtained from the control samples. The current density values, which are in the range of 1 kA/cm^{-2} (highly doped cathode) to 1 A/cm^{-2} (low doped cathode), are approximately three orders of magnitude higher than the corresponding control samples (control sample A & B on high and low doped electrodes, respectively). As mentioned before, the control samples are Cu/n-Si Schottky interfaces fabricated under similar processing conditions and with the same n-Si electrodes as the device structures, with interface size in the range of 2 μm to 8 μm. Similar enhanced conduction across metal–semiconductor interfaces has been reported in the case of silicides of Co when the interface diameter is scaled to 100 nm or less [21] and also in Au/n-Si nanocontacts [22]. The model proposed for such nanoscale Schottky diodes shows enhanced tunneling across a barrier, the size of which is interface-size dependent. Since, the estimated interface radius for the Cu/Cu–SiO$_2$/n-Si in the on-state is typically <10 nm, the devices easily fall in the regime of a nanoscale Schottky diode with possible enhanced tunneling at the interface. This effect could be absent in the case of the control samples where the interface diameters are in the order of a few microns. This effect has to be investigated further.
4. The barrier height was extracted for the samples of the highly doped n-Si devices by solving the saturation current density equations based on the TFE model for different temperatures, using the data given in Fig. 10. The barrier potential obtained via this approach was approximately 0.75 eV. Using a TE model for the same data gave a barrier height of 0.65 eV. This is to be expected as the TE model does not take the tunneling current component into account and therefore gives a lower value for the barrier. The barrier potential obtained using the TFE model on these devices is comparable to the highest measured Schottky-barrier height for a standard Cu/n-Si interface, which is 0.8 eV [15].

An Arrhenius plot of the forward bias current measured at 300 mV on the highly doped n-Si-based devices was also used to extract a barrier potential. To simplify the analysis, the TE based forward bias current equation was used in this case. The relevant equation is

$$\ln\left(\frac{I_f}{T^2}\right) = \ln\left(AA^*\right) - \frac{q(\phi_b - V_f)}{kT} \tag{2}$$

The data and the fitted model are shown in Fig. 11. Based, on the slope b of the fitted model, the calculated barrier potential was 0.68 eV which is reasonably close to the barrier potential extracted using the reverse bias saturation current density values with the TE model. The extracted barrier potential for the low doped n-Si devices was in the same range, however, the barrier potential data in that case were more prone to error as we had fewer data points due to our inability to cycle the low doped n-Si-based devices.

The above analyses show that it is extremely likely that a metal–semiconductor interface is indeed formed when the device is in its on-state. It is highly possible that the interface has a thin layer of native oxide on top of the n-Si electrode, however, based on the electrical

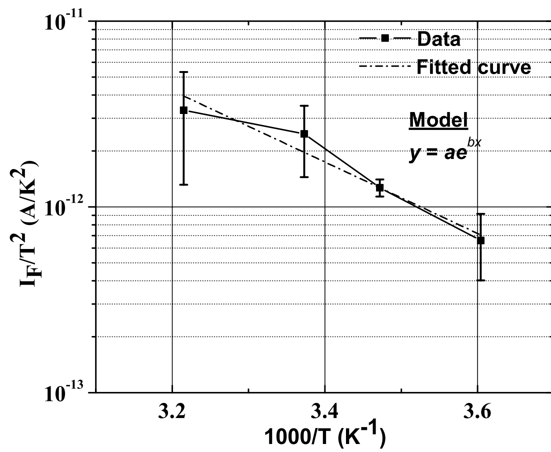


Fig. 11 Arrhenius plot of the forward bias current measured at 300 mV on the Cu/Cu–SiO_2/n-Si devices with the highly doped bottom electrode. The data are fitted to an exponential to extract the barrier potential

characterization results presented here, the interface can be well approximated by a Cu/n-Si Schottky junction.

5 Conclusions

The feasibility of a memory element with inherent rectifying properties has been demonstrated using a Programmable Metallization Cell structure with an n-type silicon electrode. The results were obtained from Cu/Cu–SiO_2/n-Si devices with silicon electrode doping densities of 10^{18} cm^{-3} and 5×10^{14} cm^{-3}. The low-resistance state of the resistive switching element produced by Cu ion migration and electrodeposition results in the formation of a Cu/n-Si Schottky interface, the behavior of which has been shown to be comparable to a Cu–Si Schottky diode in forward and reverse bias. A barrier potential for this interface was extracted and the values obtained, 0.65 eV–0.75 eV, were similar to the previously measured values for a Cu–Si interface, although current densities were relatively high possibly due to the nanoscale nature of the contact.

The leakage current in the off-state was in the order of $5/50$ nA at ± 1 V for a 6 μm diameter device but since this current is carried by the Cu–SiO_2 material, it is expected to scale with device area, e.g., $50/500$ fA at 20 nm, resulting in acceptable levels for cell-to-cell isolation even without a diode element. The reverse bias leakage current in the on-state diode was dependent on the WRITE current employed to program the device as I_{prog} influences the area of the electrodeposit and hence the area of the Cu/n-Si junction. Our analysis revealed that I_{SAT} is <1 nA at 1 V for $I_{prog} < 10$ μA, providing GΩ-level cell-to-cell isolation in a passive array. As in the case of all PMC-like memory elements, the on-state resistance of the Cu/Cu–SiO_2/n-Si device could be controlled via the magnitude of I_{prog} and this allows multi-level cell (MLC) operation, in which discrete resistance levels are used to represent multiple logical bits in each physical cell.

Our Cu/Cu–SiO_2/n-Si elements with heavily doped silicon electrodes were readily erasable at reasonable voltage (less than -5 V) which allows them to be cycled. For this study, we only attempted a small number of write-erase cycles (approximately 20) to establish basic functionality and more work is required to assess what the ultimate endurance of such structures is. The lightly doped silicon electrode devices were not able to be erased due to their very high reverse breakdown voltage but since their leakage current levels were around three orders of magnitude lower than in the case of the highly doped silicon electrode devices, they are actually ideal one-time programmable (OTP) devices as they can be programmed at low voltage and current and are extremely well isolated by their extremely high R_E in the off-state and ultra-low I_{SAT} in the on-state.

Although this work used crystalline silicon as a bottom electrode since it was relatively simple to fabricate the devices and make electrical contact to them, the results still point toward the feasibility of Cu/Cu–SiO_2/*poly*-Si-based devices with inherent rectification properties, which could then be integrated into multi-layer cells, with MLC capability, in a dense crossbar memory array. Clearly, more work is needed in this area to ascertain the characteristics of polycrystalline silicon-based devices but it is likely that since the PMC storage elements can be programmed at low currents, the use of polycrystalline silicon will not be a limiting factor for current delivery. Note also that the excellent thermal stability of Cu–SiO_2 promotes ease of integration with multiple layers of doped polycrystalline silicon electrodes deposited by chemical vapor deposition at up to 650°C.

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