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Colossal resistive switching behavior and its physical mechanism of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt thin films

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Abstract A heterojunction structure of p-NiO/n-$Mg_{0.6}Zn_{0.4}O$ with an aim to tuning or improving the resistive switching properties was fabricated on Pt/$TiO_2/SiO_2/Si$ substrates by the sol-gel spin-coating technique. The Pt/NiO/$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction thin-film device shows excellent resistive switching properties, such as a reduced threshold current of 1 µA for device initiation, a small dispersion of reset voltage ranging from 0.54 to 0.62 V, long retention time and a high resistance ratio of high-resistance state to low-resistance state about six orders of magnitude. These results indicate that the resistive switching properties can be greatly improved by constructing the p-NiO/n-$Mg_{0.6}Zn_{0.4}O$ heterojunction for nonvolatile memory applications. The physical mechanism responsible for colossal resistive switching properties of the heterojunction was analyzed based on interfacial defect effect and formation and rapture of conductive filaments.

1 Introduction

Recently, reproducible resistive switching behaviors between high-resistance states (HRS) and low-resistance states (LRS) have attracted great attention for potential applications in next generation nonvolatile memory devices such as resistive random access memories (RRAM) [1, 2]. However, the origin of the resistive switching effect is still not well understood now. This leads to numerous investigations on various material systems. On the other hand, constructing oxide heterostructures such as $SrTiO_{3-\delta}$/Nb–$SrTiO_3$ or multilayer structures such as NiO/IrO_2, NiO_y/TiO_x has been thought to be an effective way to tune or improve resistive switching performances through the interfacial effects [3–6].

It is known that both NiO and $Mg_xZn_{1-x}O$ thin films sandwiched by Pt electrodes exhibit the resistive switching effect [7–10], especially, $Mg_xZn_{1-x}O$ thin films with high Mg contents have ultrahigh resistance ratio of HRS to LRS ($R_{H/L}$) which is beneficial for improving the signal-to-noise ratio of devices [11]. Note that intrinsic NiO film is p-type conduction and ZnO-based film is n-type [12, 13], therefore, they can constitute a p–n junction. Meanwhile, considering that the p–n junction is the key structure of electronic devices and can be utilized as a switching element to access the memory by forming the so-called "$1D/1R$" structure [14], it should be of much interest to investigate if p–n heterojunction structures composed of p-NiO and n-$Mg_xZn_{1-x}O$ exhibit good resistive switching properties.

In this study, p-NiO/n-$Mg_xZn_{1-x}O$ heterojunctions were fabricated on Pt/$TiO_2/SiO_2/Si$ substrates. The Pt/NiO/$Mg_xZn_{1-x}O$/Pt heterojunction devices show good reproducible resistive switching properties, such as reduced threshold current for device initiation, small dispersion of reset voltage, and high resistance ratio $R_{H/L}$.

2 Experimental

The NiO/$Mg_{0.6}Zn_{0.4}O$ heterojunctions were prepared by sol-gel spin-coating technique. The details of solution synthesis and heterojunction fabrication have been reported

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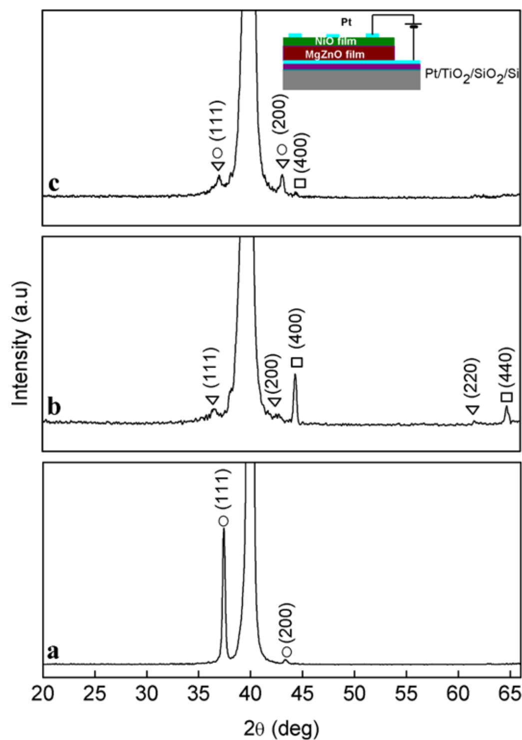

Fig. 1 XRD patterns of films deposited on $Pt/TiO_2/SiO_2/Si$ substrates, (**a**) NiO films, (**b**) $Mg_{0.6}Zn_{0.4}O$ films, and (**c**) $NiO/Mg_{0.6}Zn_{0.4}O$ heterojunction films. *The open circle* and *open reversed triangle* denote cubic phase of NiO and $Mg_{0.6}Zn_{0.4}O$ films, respectively. *The open squares* denote the spinel phase. *The inset* shows a schematic diagram of the Pt/*p*-NiO/*n*-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device

elsewhere [11, 13]. The heterojunctions were annealed at 650°C for 1 h at air ambient. The thickness of NiO and $Mg_{0.6}Zn_{0.4}O$ layers is about 100 nm and 300 nm, respectively. For comparison, NiO film and $Mg_{0.6}Zn_{0.4}O$ film were, respectively, prepared on $Pt/TiO_2/SiO_2/Si$ substrates under same experimental conditions. The crystalline phases of the heterojunctions and the individual thin films were characterized in θ–2θ mode by a Rigaku (D-MAX 2200 VPC) X-ray diffractometer (XRD) with Cu K_α radiation ($\lambda = 0.154$ nm). The I–V curves were measured at room temperature by a Keithley 236 sourcemeter after deposition of circular Pt top electrodes (thickness about 100 nm) with diameter of 0.3 mm through a shadow mask. The bias voltage was swept from $0\ V \rightarrow +V_{max} \rightarrow 0\ V \rightarrow -V_{max} \rightarrow 0\ V$. Before the measurement of I–V loops, a threshold current pulse (I_D) with delay time of 50 ms was applied for initiation. The schematic structure of the heterojunction device is illustrated in the inset of Fig. 1.

3 Results and discussions

Figure 1 shows XRD patterns of NiO films, $Mg_{0.6}Zn_{0.4}O$ films, and $NiO/Mg_{0.6}Zn_{0.4}O$ heterojunction films deposited on $Pt/TiO_2/SiO_2/Si$ substrates by sol–gel method. The open circle and open reversed triangle denote cubic phase of NiO and $Mg_{0.6}Zn_{0.4}O$ films, respectively. The open square denotes the spinel phase [15]. It can be seen that the NiO films show the pure cubic phase, while the $Mg_{0.6}Zn_{0.4}O$ films and the $NiO/Mg_{0.6}Zn_{0.4}O$ heterojunction films consist of cubic phase and spinel phase. It is believed that the cubic phases in heterojunction resulted from the overlapped cubic phases of NiO and $Mg_{0.6}Zn_{0.4}O$ films. No impurity phase can be detected from interfacial reaction between $Mg_{0.6}Zn_{0.4}O$ layer and NiO layer.

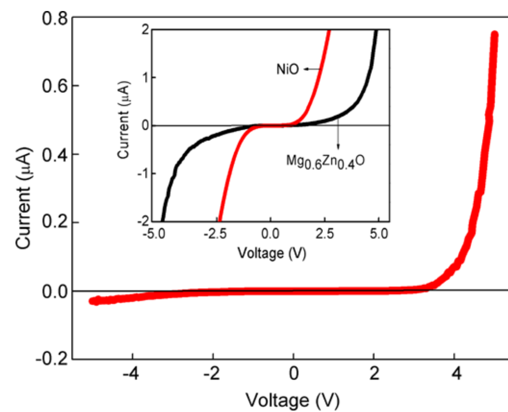

Fig. 2 Typical original rectifying I–V characteristic of the $NiO/Mg_{0.6}Zn_{0.4}O$ heterojunction. *The inset* shows the I–V curves of Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt structures

Figure 2 shows original I–V curve of Pt/*p*-NiO/*n*-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device. A good rectifying characteristic can be observed from the asymmetric I–V curves between reverse and forward bias. For comparison, rather a symmetrical I–V dependence of Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt devices is shown in the inset of Fig. 2, suggesting that the rectifying behavior of heterojunction can be attributed to the formation of a typical *p*–*n* junction at the oxide interface, which agrees with previous reports [13, 16]. It is the *p*–*n* junction and interface that modify the transport of the carriers, and affect the resistance switching behaviors of the heterojunction device.

After initiated by threshold current pulse (I_D) of 1 μA (i.e. so-called electroforming and set process), Pt/*p*-NiO/*n*-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device exhibits the reproducible and stable resistive switching effects in the positive bias region, shown as Fig. 3. Inset of Fig. 3 shows one typical resistive switching process of Pt/*p*-NiO/*n*-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device plotted in double-log scale. It can be seen that a high resistance ratio of HRS to LRS ($R_{H/L}$) of about six orders of magnitude for the Pt/*p*-NiO/*n*-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device is achieved, which is favorable for high signal-to-noise ratio of the resistive switching devices.

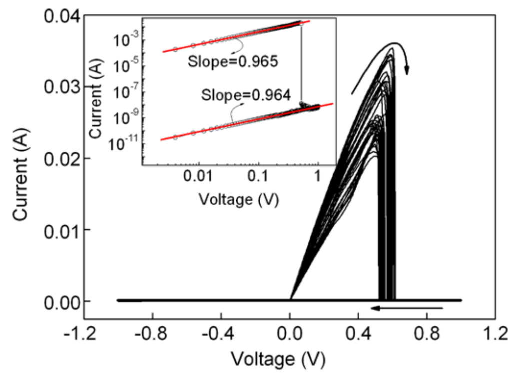

Fig. 3 I–V behaviors of memory cell based on Pt/NiO/$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction devices, initiated by current pulse of 1 μA. *The inset* shows typical resistive switching process of Pt/NiO/$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction in log–log scale

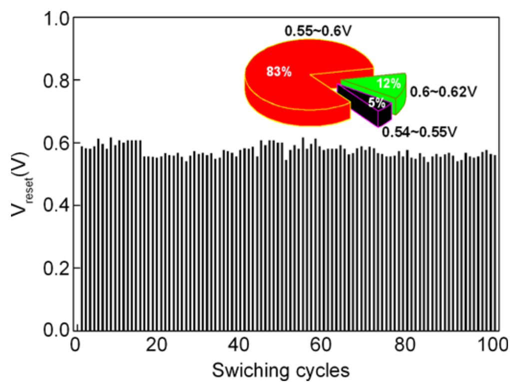

Fig. 4 Dispersion of V_{reset} of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device in 100 *switching cycles* and *the inset* shows its configuration

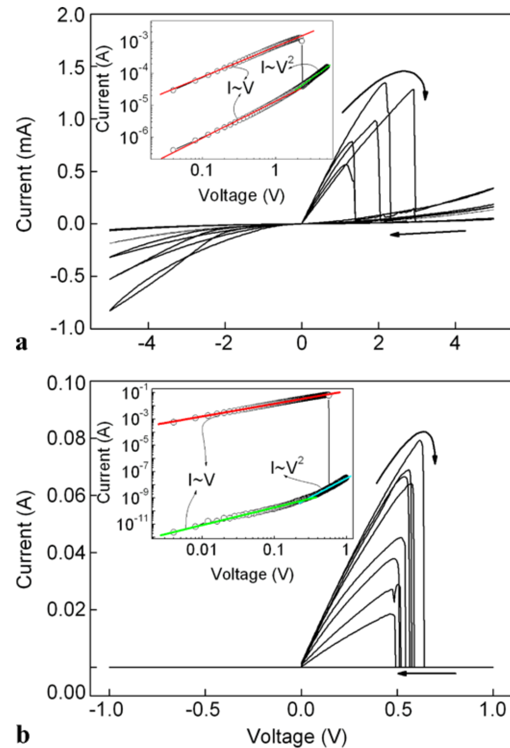

Fig. 5 I–V behaviors of memory cells based on (**a**) Pt/NiO/Pt initiated by current pulse of 1 mA and (**b**) Pt/$Mg_{0.6}Zn_{0.4}O$/Pt initiated by current pulse of 5 mA. *The inset* in (**a**) shows typical resistive switching process of Pt/NiO/Pt in log–log scale, and *the inset* in (**b**) shows typical resistive switching process of Pt/$Mg_{0.6}Zn_{0.4}O$/Pt in log–log scale, respectively

Figure 4 shows the dispersion of the reset voltage (V_{reset}) of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device in 100 switching cycles. Considerable stability of V_{reset} was observed, values of which scattered within 0.54–0.62 V. The inset of Fig. 4 shows the configuration of V_{reset}. It can be seen that V_{reset} distributes mostly in 0.55–0.6 V region. The V_{reset} below 0.55 V and above 0.6 V account for 5% and 12%, respectively. These results show that the small dispersive distribution of V_{reset}, which is favorable for reading the signal of device, can be achieve by fabrication of p–n heterojunction device.

For comparison, I–V curves of Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt devices prepared under the same conditions are shown in Fig. 5. For the Pt/NiO/Pt device, a threshold current pulse I_D of 1 mA with delay time of 50 ms was applied for initiation before the I–V measurements. The resistance ratio $R_{H/L}$ of the Pt/NiO/Pt device is ∼100. However, it can be observed that there is a serious dispersion for the reset voltage between 1–3 V. As for the Pt/$Mg_{0.6}Zn_{0.4}O$/Pt device, a threshold current pulse I_D of 5 mA with delay time of 50 ms was applied for initiation, after which the Pt/$Mg_{0.6}Zn_{0.4}O$/Pt device shows an ultra-high $R_{H/L}$ of 10^7 [11].

Table 1 lists the resistive switching parameters of the Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction devices together with those of Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt devices. It can be seen that $R_{H/L}$ of the heterojunction device is comparable to that of the Pt/$Mg_{0.6}Zn_{0.4}O$/Pt device. However, V_{reset} of the heterojunction device is within 0.54–0.62 V, showing smaller dispersion than that of Pt/NiO/Pt device. In addition, I_D of the heterojunction device is reduced as low as 1 μA, much smaller than those of Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt devices (1 mA and 5 mA, respectively). These results indicate that the resistive switching properties have been greatly improved by constructing the p–n heterojunctions.

Additionally, for Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt device, similar linear I–V behavior of HRS and LRS can be seen from inset of Fig. 3, both corresponding to the Ohmic conduction mechanism. While the space charge limited current conduction mechanisms in HRS were observed in Pt/NiO/Pt and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt devices, shown as inset of Figs. 5(a) and 5(b), respectively. For the p–n heterojunction device, the built-in potential should be mainly applied to $Mg_{0.6}Zn_{0.4}O$ layer due to its much lower carrier concentra-

Table 1 Resistive switching parameters of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device, Pt/NiO/Pt device, and Pt/$Mg_{0.6}Zn_{0.4}O$/Pt device

Device	I_D	V_{reset} (V)	I_{max} (mA)	$R_{H/L}$
Pt/NiO/Pt	1 mA	1–3	0.5–1.5	$\sim 10^2$
Pt/$Mg_{0.6}Zn_{0.4}O$/Pt*	5 mA	0.5–0.75	60–90	$\sim 10^7$
Pt/NiO/$Mg_{0.6}Zn_{0.4}O$/Pt	1 μA	0.54–0.62	20–35	$\sim 10^6$

*See [11]

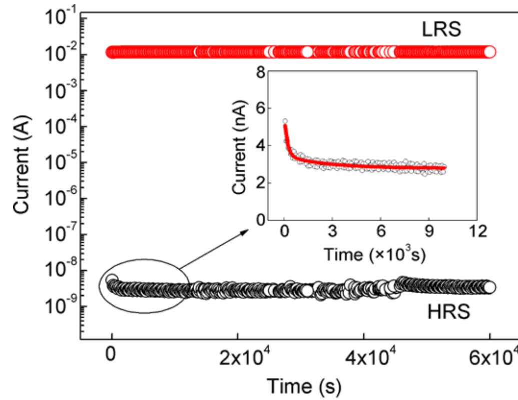

Fig. 6 Retention time characteristic of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt device in the LRS and HRS; the current was readout at 0.2 V. *The inset* shows the current relaxation behavior of HRS within 10^4 s, and *the red solid line* means the result of fitting with a double exponential decay law

tion than NiO layer. Therefore, the depleting layer is mainly in $Mg_{0.6}Zn_{0.4}O$ layer, which also dominates the electrical properties of p–n heterojunction device when it is switched to the HRS. Therefore, a high $R_{H/L}$ of heterojunction device can be achieved due to the ultrahigh $R_{H/L}$ of $Mg_{0.6}Zn_{0.4}O$ layer. However, the forward voltage is within 1 V, most of which is utilized to overcome the built-in potential of p–n heterojunction. As a consequence, the current injected and the bias voltage on $Mg_{0.6}Zn_{0.4}O$ layer is low when the devices switch to HRS, resulting in the linear I–V dependence of HRS.

To further demonstrate the stability of the resistive switching properties of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt devices, data retention time behavior was investigated by examining the current evolution of the device in the LRS and HRS over a long period of time (6×10^4 s), respectively. The current was readout at a constant bias of 0.2 V after set and reset switching. As shown in Fig. 6, the appreciable stability of current can be observed in the each state of fabricated devices. Within the measure time, the $R_{H/L}$ keeps about six orders of magnitude with no distinct degradation, indicating that the Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt devices have a non-destructive readout property and can store the information for a long time, which is favorable for non-volatile memory cells. The inset in Fig. 6 shows the current relaxation behavior of HRS within 10^4 s, which can be well fitted by the second order exponential decay law: $I = I_0 + A_1 \exp(-t/\tau_1) + A_2 \exp(-t/\tau_2)$ with time constant $\tau_1 = 0.75$ h and $\tau_2 = 0.05$ h.

Recently, some investigations showed that the resistive switching properties of oxide, including NiO and ZnO, sandwiched between two metal electrodes are originated from formation and rupture of local conductive filamentary paths, corresponding to "set" and "reset" process, respectively [2, 17, 18]. For our Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction device, the defect interface layer is believed to be formed between NiO and MgZnO, whose effects must be taken into consideration on forming the conductive filaments. It has been reported that a variety of defects assembled at the interface, leading to formation of space charge region, will modify or dominate the switching properties [3, 4]. As mentioned before, the current pulse I_D of 1 μA can switch Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction to LRS due to formation of conductive filaments. However, for NiO and $Mg_{0.6}Zn_{0.4}O$ thin films same as the individual layers in the heterojunction device, a mA-level current pulse is needed. This means that the interfacial defects of Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction might facilitate the formation and rupture of the filaments during the switching process. In addition, note that V_{reset} of the heterojunction device is 0.55–0.60 V, much lower than that of Pt/NiO/Pt device, it is reasonable to believe that the resistive switching properties of the Pt/p-NiO/n-$Mg_{0.6}Zn_{0.4}O$/Pt device are mainly originating from the interface while the NiO layer is in the low-resistance state. On the other hand, the dispersion of V_{reset} can also be minimized by avoiding the random formation and rupture of filaments at the interface. Kinoshita and coworkers also reported that the conductive filaments formed in sequence for heterojunction devices due to the differences of concentration and configuration of defects [6]. Further study to investigate the correlation among the interfacial defects, transport of carriers and resistance switching characteristics is ongoing.

4 Conclusions

In conclusion, NiO/$Mg_{0.6}Zn_{0.4}O$ p–n heterojunctions were prepared on $Pt/TiO_2/SiO_2/Si$ substrates by sol-gel spin-coating technique. The resultant Pt/NiO/$Mg_{0.6}Zn_{0.4}O$/Pt heterojunction devices exhibit typical rectifying I–V characteristics. After initiation, the resistive switching effects

with a high resistance ratio about six orders of magnitude are demonstrated. Furthermore, the heterojunction devices have a small reset voltage dispersion and a low threshold current for device initiation. These results indicate that the resistive switching properties can be greatly improved by constructing the p–n heterojunctions.

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