# Performance improvement of $Cu_x O$ resistive switching memory by surface modification

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Received: 18 October 2010 / Accepted: 22 December 2010 / Published online: 22 January 2011 © Springer-Verlag 2011

Abstract The  $Cu_xO$  films grown by plasma oxidation are composed of an insulating CuO layer and a conductive gradient  $Cu_xO$  layer. We found that the surface CuO layer influenced the switching behaviors greatly. Giant improvement of reliable endurance was achieved after annealing the device in the N<sub>2</sub> atmosphere, resulting from the transition of CuO to Cu<sub>2</sub>O. The possible mechanism for this improvement is attributed to the alleviation of over-programming during forming process. The result shows that for resistance switching Cu<sub>2</sub>O is much more preferred than CuO. After further reducing the thickness of Cu<sub>2</sub>O layer, the forming voltage can be totally eliminated.

## **1** Introduction

Non-volatile memories (NVM) are becoming more and more important in semiconductor market. As a most promising candidate for next generation NVM, resistive random access memory (RRAM) has attracted a great deal of attention for its low power, low cost, and fast speed. Many materials have been investigated for RRAM applications, such as binary transition metal oxides (BTMO) [1–3], doped perovskites [4], chalcogenides [5], and organic semi-

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T. Tang Department of Microelectronics, Fudan University, Shanghai 200433, P.R. China conductors [6]. However, more and more scientists and industry developers pay attention to BTMO RRAM for their simple composition and good compatibility with silicon processes.

 $Cu_xO$  is an excellent solution for RRAM application in BTMO materials because  $Cu_xO$  memory is fully compatible with standard Cu interconnect processes. However, the poor endurance of this  $Cu_xO$ -based memory prevents it from practical application [7, 8].

In this work, we reported an effective way to enhance the endurance properties of  $Cu_xO$ -based RRAM fabricated by plasma oxidation. By means of modifying the surface layer, the superior endurance performance could be achieved.

# 2 Experiments

1 µm electrochemical-plant (ECP) Cu was deposited on Cu [seed layer (120 nm)]/Ta (10 nm)/TaN (15 nm)/SiO<sub>2</sub> (400 nm)/Si substrate with standard Novellus ECP system at room temperature. Different thickness Cu<sub>x</sub>O films of CuO surface layer were grown on inductively-coupled plasma (ICP) system at low temperature. The Cu films were also treated as bottom electrodes to compose a metal-oxide-metal (MOM) structure, while Al top electrodes (300 nm) were fabricated by electron beam evaporation and lift-off process with a square area of  $180 \times 180 \,\mu\text{m}^2$ . The depth distribution profile of Cu and O elements in Cu<sub>x</sub>O films was analyzed by sputtering—Auger electron spectroscopy (AES). The current-voltage (I-V) characterizations of the Al/Cu<sub>x</sub>O/Cu structure were performed on a Keithley 4200-SCS semiconductor parameter analyzer accompanied with a Keithley 3402 pulse generator.

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#### 3 Results and discussion

The RIE oxidation tool in our experiment has no cooling apparatus to keep the substrate at constant temperature. During the oxygen plasma treating, the temperature of the plasmabombed substrate will be raised as the oxidation time increases. Therefore, the products of Cu<sub>x</sub>O oxide are quite different when being treated at various times. Figure 1 shows the depth profiles of O and Cu concentration ratio of 30 and 10 min oxidized samples, denoted as sample A and C, respectively. The sample B was prepared by annealing the sample A at 350 °C for 30 min under N<sub>2</sub> atmosphere. It can be clearly seen that all the samples can be divided into two layers, a surface  $Cu_x O$  layer and a gradient  $Cu_x O$  layer. By selectively removing the surface  $Cu_xO$ , we found the devices with left gradient Cu<sub>x</sub>O configured by Pt/gradient- $Cu_xO/Cu$  structure were shortened, indicating that the gradient CuxO was actually conductive. From the AES measurements, the surface [Cu]/[O] ratio of sample A is about 0.9, while for sample B and C the ratio is about 0.7. From this result we can get two conclusions. First, the product of 10-min oxidation is mainly composed of Cu<sub>2</sub>O, while for 30-min oxidation it is mainly composed of CuO. Second, the CuO layer can be transited to Cu<sub>2</sub>O by thermal annealing in O-deficient ambience. The average etching rate of Ar ion sputtering on  $Cu_x O$  was about 13 nm per minute; therefore, the thicknesses of surface Cu<sub>x</sub>O layer and inner gradient  $Cu_x O$  layer can be approximately calculated since the etching rates for the two layers are nearly the same.

Figure 2 shows the XPS spectra Cu 2p3/2 of samples A, B and C. It is obvious that the 10-min oxidized sample is mainly composed of cuprous oxide with Cu 2p3/2 peak locating at 932.23 eV and little cupric oxide having Cu 2p3/2 peak at 933.83 eV. Sample B has nearly the same composition as sample C; while for sample A only two peaks of cupric oxide are found on the surface, respectively locating at 933.1 eV and 934.2 eV [9]. The results agree well with the conclusion deduced from the above AES measurement.

Figure 3 shows the I-V curves of forming process of samples A, B and C with 180-µm sized Al/Cu<sub>x</sub>O/Cu structure under d.c. voltage sweep at room temperature. During the test, the Cu substrate was grounded and the Al top electrode was positively biased. As can be seen from the figure, the first set voltage and current for 30-min oxidized sample are about 13 V and 25 mA, respectively. The *R*-on after forming process is always at about 10  $\Omega$ , which is so low that more than 80% of the device cannot switch back to HRS. In other words, the yield of this device with 30-min oxidized Cu<sub>x</sub>O is as low as 20%. Moreover, the HRS of this 20% device is much lower than the initial resistance. As for sample B, the forming voltage and current are reduced to a great degree, to 7.5 V and 2 mA, respectively. Samples



Fig. 1 The depth profile of O and Cu concentration ratio of samples A, B and C. The average etching rate of Ar ion sputtering on  $Cu_xO$  was about 13 nm per minute. S–A, S–B and S–C represent samples A, B and C, respectively.  $t_0$  is the plasma oxidation time



Fig. 2 XPS spectra Cu 2p3/2 of samples A, B and C



Fig. 3 I-V curves of forming process for samples A, B and C with 180-µm sized Al/Cu<sub>x</sub>O/Cu structure under d.c. voltage sweep at room temperature. The voltages were swept at a speed of 0.01 V per step. S–A, S–B and S–C represent samples A, B and C, respectively



A and B are nearly of the same thickness. The only difference between them is the composition of the surface layer. The result indicates that the Cu<sub>2</sub>O layer can be broken down more easily than CuO layer. This is reasonable. The Cu<sub>2</sub>O film has relatively more defects due to the enrichment of copper vacancy [10]. By comparing the samples B and C it can be further found that by reducing the thickness of the surface Cu<sub>2</sub>O layer, the forming voltage can be totally eliminated, with the same value of the lateral successive SET voltage. It seems that the thickness of surface Cu<sub>2</sub>O layer controls whether the forming process occurs or not. If the Cu<sub>2</sub>O layer is thin enough, no extra forming voltage is necessary. It is worthy to mention here that there exists a lower limit for the Cu<sub>2</sub>O thickness, e.g. the 3-min oxidized sample has almost no switching characteristics. The possible reason may be ascribed to the inter-diffusion of the electrode and the Cu<sub>2</sub>O layer. When the Cu<sub>2</sub>O layer is too thin, the whole device would be punched through.

Next, let us further evaluate the endurance performance of these three kinds of devices. Due to the severe overprogramming in the forming process of the sample A, the switching characteristics were seriously degraded. Only tens to hundreds of switching cycles were found in this device. The typical values of *R*-on after forming process for samples A, B and C are 100, 50, and 10  $\Omega$ , respectively. Although sample B also needs forming process, 90% of this device can still switch back to HRS and exhibit reliable switching behavior. The endurance of sample C can achieve thousands of operation cycles. As for sample A, an excellent endurance of more than 10<sup>4</sup> cycles and high yield of 99% can be achieved.

According to our previous study, local conductive filaments' formation and rupture model was well demonstrated as the switching mechanism for Cu<sub>x</sub>O-film-based RRAM device [3, 11]. A possible explanation of the improvement of this model's switching performance after surface modification will be discussed in the following. Figure 4 shows the schematic diagrams of the forming process for the samples A, B and C. The pristine stages of samples A, B and C are depicted in Fig. 4(a) to (c), which are comprised of thick CuO, thick Cu<sub>2</sub>O and thin Cu<sub>2</sub>O, respectively. Compared with Cu<sub>2</sub>O, the CuO film is more insulating and dense, resulting in higher voltage and current needed to break it down. As can be seen from Fig. 3, the forming voltage and current for sample A are about 13 V and 25 mA, respectively, which would cause severe over-programming to the memory device. The consequent R-on value after forming process is as low as 10  $\Omega$ , which corresponds to a strong conductive filament formed in CuO film (as shown in Fig. 4(d)). Assuming the RESET process is caused by Joule heating [11], a critical temperature should be reached to dissolve the filament. When *R*-on is too low, an extremely high RESET current is needed to generate enough Joule heat. On the other hand, the heat is also dissolved through the electrode. The stronger the filament, the more dissolution there will be. So, when the generated Joule heating is less than that which dissolved, the RESET process will never happen. This may be the cause for the low device yield of sample A. As for Cu<sub>2</sub>O film, which has more defects such as grain boundaries and copper vacancies, it can be broken down more easily. The forming voltage and current for sample B are about 7.5 V and 2 mA, much lower than those for sample A. Relatively thin conductive filament could be formed after forming process (as shown in Fig. 4(e)). Although sample B still needs the forming voltage, the yield and performance are much better than for sample A. By further reducing the thickness of Cu<sub>2</sub>O film, the forming voltage can be fully eliminated, which is nearly the same as the subsequent SET voltage. The conductive filament formed is also the smallest (as seen from Fig. 4(f)).

# 4 Conclusions

The performance of  $Cu_xO$ -based resistive switching memory with different surface modifications was investigated. The surface CuO layer influenced the switching behaviors greatly. After annealing the device in the N<sub>2</sub> atmosphere, the forming voltage and current were greatly reduced. The device performances such as endurance and yield were improved dramatically. The possible cause is the transition of CuO to Cu<sub>2</sub>O during annealing in oxygen deficient ambience. By further reducing the thickness of Cu<sub>2</sub>O layer, the forming voltage can be totally eliminated. This work provides a promising clue for further improving the RRAM device performance.

### References

- C. Rohde, B.J. Choi, D.S. Jeong, S. Choi, J.S. Zhao, C.S. Hwang, Appl. Phys. Lett. 86, 262907 (2005)
- A. Beck, J.G. Bednorz, Ch. Gerber, C. Rossel, D. Widmer, Appl. Phys. Lett. 77, 139 (2000)
- H.B. Lv, X.F. Fu, P. Zhou, Y.Y. Lin, T.A. Tang, IEEE Electron Device Lett. 29, 309 (2008)
- S. Srivastava, N.K. Pandey, P. Padhan, R.C. Budhani, Phys. Rev. B 62, 21 (2000)
- D. Adler, M.S. Shur, M. Silver, S.R. Ovshinsky, J. Appl. Phys. 51, 3289 (1980)
- T. Oyamada, H. Tanaka, K. Matsushige, H. Sasabe, C. Adachi, Appl. Phys. Lett. 83, 1252 (2003)
- A. Chen, S. Haddad, Y.C. Wu, T.N. Fang, Z. Lan, S. Avanzino, S. Pangrle, M. Buynoski, M. Rathor, W. Cai, N. Tripsas, C. Bill, M. VanBuskirk, M. Taguchi, in *Electron Devices Meeting*, 2005. *IEDM Tech. Digest. IEEE International* (2005), p. 746
- R. Dong, D.S. Lee, W.F. Xiang, S.J. Oh, D.J. Seong, S.H. Heo, H.J. Choi, M.J. Kwon, S.N. Seo, M.B. Pyun, M. Hasan, H. Hwang, Appl. Phys. Lett. **90**, 042107 (2007)
- 9. http://srdata.nist.gov/xps/Bind\_e\_spec\_query.asp
- 10. A.F. Wright, J.S. Nelson, J. Appl. Phys. 92, 5849 (2002)
- H.B. Lv, M. Wang, H.J. Wan, Y.L. Song, W.J. Luo, P. Zhou, T.A. Tang, Y.Y. Lin, R. Huang, S. Song, J.G. Wu, H.M. Wu, M.H. Chi, Appl. Phys. Lett. 94, 213502 (2009)