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Resistance switching effect in $LaAlO_3$/Nb-doped $SrTiO_3$ heterostructure

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Abstract The authors report on the fabrication and electronic transport property of $LaAlO_3$/Nb-doped $SrTiO_3$ heterostructure. The current–voltage curves of this heterostructure show hysteresis and a remarkable resistance switching behavior, which increase dramatically with decreasing temperature. Multiresistance states were realized by voltage pulses with different amplitudes and polarities and the ratio of the electrical pulse induced resistance change is larger than 10^4. More interestingly, the relaxation of junction current after switching follows the Curie–von Schweidler law $J \propto t^{-n}$ with an exponential increase of n with temperature. The results were discussed in terms of the trap-controlled space charge limited conduction process via defects near the interface of the heterostructure.

1 Introduction

Recently, electric field and/or current induced resistance switching (RS) effect observed in the metal-insulator-metal (MIM) structures has attracted much attention due to its potential applications in the nonvolatile random access memory, as well as its importance for understanding the electronic transport in these structures [1–8]. The so-called colossal electro-resistance (CER), related to the RS effect, has been found in the MIM structures with various insulating oxides [1, 9–12]. Besides the RS effect in the MIM structures involving metal-oxide heterostructures, there are a few reports on the RS effect in the heterostructures composed of two oxides [13–15]. The study of RS effect in the all oxide heterostructures is significant because combinations of different oxides can show various properties, and the controlled interface and epitaxy can be easily realized, which is helpful for shedding light on the mechanisms of RS effect. Moreover, for both the MIM structures and all oxide heterostructures, the study of temperature dependence for the RS effect and the relaxation behavior of junction current after switching, which are important for understanding the mechanisms of RS effect, is still limited [15, 16].

$LaAlO_3$(LAO) is an interesting high-k material with a dielectric constant of about ∼25, wide energy band gap of ∼6 eV, and thermal stability up to 2100°C. It is widely used as the substrate for thin film growth. Actually, it is also a suitable material for the nonvolatile memory devices. Up to now, however, there has been no report on the RS effect or CER in LAO and LAO related heterostructure. In this paper, we report on the giant RS effect in the heterostructure of LAO/Nb-doped $SrTiO_3$. The temperature dependence of the RS effect and the relaxation behavior of the junction current after switching were investigated in detail. Based on the analysis of these results, a mechanism was proposed to account for the RS effect in LAO/Nb-doped $SrTiO_3$.

2 Experimental

LAO thin films were deposited on the (100) oriented, 0.7 wt% Nb-doped $SrTiO_3$(NSTO) substrates to obtain the LAO/NSTO heterostructures using the pulsed laser deposition. LAO single crystal was used as the target. The laser

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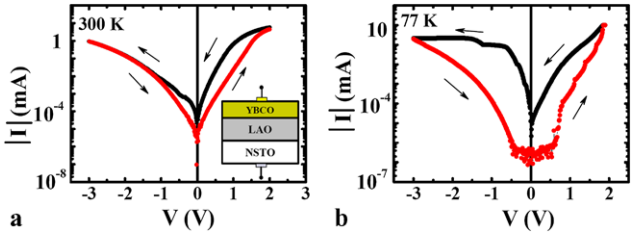

Fig. 1 *I–V* curves of YBCO/LAO/NSTO heterostructure at (**a**) 300 K and (**b**) 77 K, respectively. The *arrows* indicate the direction for changing voltage. The *inset* of (**a**) is the schematic of the sample and electrodes setting

pulse frequency was 3 Hz, and the pulse energy density was about 1.5 J/cm^2. During the deposition process, a substrate temperature of 700°C and an oxygen pressure of 13 Pa were maintained. $YBa_2Cu_3O_{7-\delta}$ (YBCO) was then deposited in-situ on LAO. After deposition, the film was cooled down to room temperature with a 0.8 atm of oxygen. The thickness of LAO film is about 150 nm. YBCO was deposited as the top electrode, which is in ohmic contact with LAO film and Au pad was deposited on YBCO as the top electrode by magnetron sputtering using a shadow mask. Indium was pressed on the back of NSTO as the bottom electrode which is in ohmic contact with NSTO. The X-ray diffraction patterns of the heterostructure, obtained by using a Rigaku diffractometer with a Cu K_α radiation, do not show impurity peaks. The current-voltage (*I–V*) curves of the heterostructure were measured by the two-probe method using a Keithley 2400 source meter. DC voltage pulses with width of 0.2 s and interval of 0.1 s were applied to measure the *I–V* curves with a step of 0.05 V. In order to protect the samples, a compliance current of 10 mA was used. The schematic of the sandwich structure is shown in the inset of Fig. 1(a). The positive bias is defined by the current flowing from the top electrode to the bottom electrode. For the measurements from low to high temperature, the samples with the probe were dipped into liquid nitrogen.

3 Results and discussion

The junction resistance per unit area (1 cm^2) for the as-deposited YBCO/LAO/NSTO was larger than 10^{10} Ω in the voltage region from −3 to 2 V and no RS effect is present. Therefore, an electroforming process was performed on the heterostructure with a forming voltage of 15 V. After the forming process, *I–V* curves of YBCO/LAO/NSTO were measured at different temperatures. Figure 1 shows the *I–V* curves for the YBCO/LAO/NSTO heterostructure measured at 300 and 77 K with the sequence of $0 \rightarrow 2 \rightarrow 0 \rightarrow -3 \rightarrow 0$ V. The heterostructure exhibits a rectifying behavior and a remarkable hysteresis. The hysteresis becomes more remarkable at low temperatures, manifesting the resultant RS

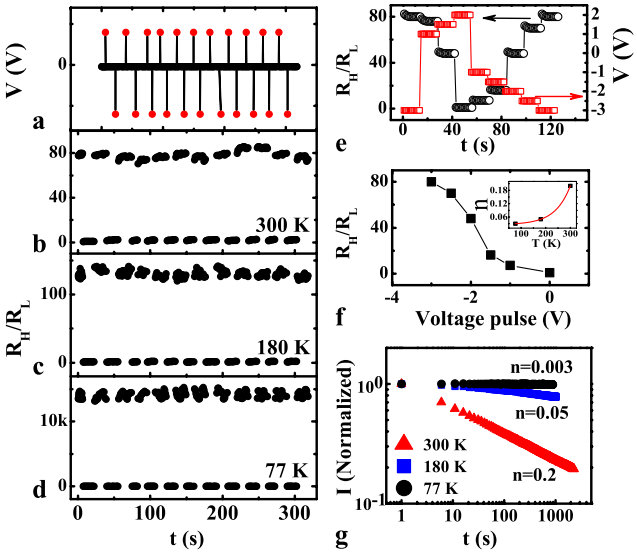

Fig. 2 Tuneability of YBCO/LAO/NSTO junction resistance with a train of voltage pulses of given polarities. (**a**) The train of voltage pulses with amplitudes of +2 V and −3 V. Responses of the junction resistance to the train of voltage pulses at different temperatures with (**b**) 300 K, (**c**) 180 K, and (**d**) 77 K, respectively. (**e**) Variation of the junction resistance at 300 K with different polarities and amplitudes of triggered voltage pulses. (**f**) Variations of the junction resistance with different triggered voltage pulses at 300 K. The *inset* is the variation of n with temperature. (**g**) Relaxation of the junction current at different temperatures after switching to the LRS

effect. Here, we define the upper and lower branches of the *I–V* curves as the low-resistance state (LRS) and high resistance state (HRS), respectively. The resistance of the heterostructure is switched from the HRS to LRS by applying a positive bias voltage and from LRS to HRS by applying a negative bias voltage. In order to estimate the contributions from the Au/YBCO and YBCO/LAO interfaces, YBCO films grown on $SrTiO_3$(STO) substrates were used with two Au pads on the surface of YBCO and the *I–V* curve of Au/YBCO shows linear behavior without hysteresis. We also grew YBCO/LAO/YBCO trilayer structure on STO substrate and the *I–V* curve of YBCO/LAO/YBCO also shows a linear behavior without hysteresis. Thus, *I–V* behavior of the YBCO/LAO/NSTO heterostructures is dominated by the LAO/NSTO interface.

In order to study the temporal variation of the response of YBCO/LAO/NSTO heterojunction to the voltage pulses, the variation of the junction resistance with a train of voltage pulses of given polarities and amplitudes was measured at different temperatures and the result is shown in Fig. 2. Figure 2(a) shows the train of voltage pulses with +2 V and −3 V, respectively. Figures 2(b), 3(c), and 3(d) are the responses of the junction resistance for YBCO/LAO/NSTO to the train of voltage pulses at different temperatures. To measure the junction resistance, a voltage pulse of −0.1 V was applied and this measuring process was repeated more than 50 times successively before the polarity of the electric pulse

was reversed and the same process was repeated. The junction resistance was normalized to the LRS. It can be seen that the train of voltage pulses can switch the heterojunction between different resistive states with the positive voltage pulses decreasing the resistance (increasing current) and the negative voltage pulses increasing the resistance (decreasing current), resulting in the LRS and HRS, respectively. The ratio of the electrical pulse induced resistance change (EPIR), defined by R_H/R_L, is about 80 at RT and increases with decreasing temperature, reaching about 14500 at 77 K, which is among the largest EPIR reported so far. Figure 2(e) is the variation of the junction resistance at 300 K with different polarities and amplitudes of triggered voltage pulses. The data were obtained by the method similar to that of Fig. 2(b) to Fig. 2(d). The change of the junction resistance with time was measured under different voltage pulses to obtain the ratio of R_H/R_L. First, the junction was triggered to the HRS with a voltage pulse of -3 V, followed by quasi-LRS with voltage pulse of $+1$, $+1.5$ V, respectively and finally LRS with a voltage pulse of $+2$ V. We got R_H/R_L by dividing the resistances of HRS (-3 V) by those of LRS. After these, the junction was triggered to quasi-HRS with voltage pulses of -1, -1.5, -2, -2.5 V, respectively and HRS with a voltage pulse of -3 V. We normalized the resistances of HRS with that of the LRS ($+2$ V) to obtain R_H/R_L. It shows that the junction resistance changes with the amplitude of voltage pulse, resulting in multi-resistance states and the R_H/R_L stays steadily after the pulse application regardless of the resistive status of the junction right before the pulse application. Figure 2(f) is the dependence of EPIR on the amplitude of triggered voltage pulses with negative polarity which was derived from Fig. 2(e). EPIR increases with the amplitude of triggered voltage and finally gets saturated.

In our previous work [15], it has been shown for $SrTiO_{3-x}$/NSTO heterojunction that the junction current relaxes with time after switching to the LRS and the relaxation follows the Curie–von Schweidler law at room temperature, indicating the role of defects in the interfacial depletion region. In order to explore the mechanism for the RS effect and the types of defects in LAO/NSTO heterojunction, we measured the relaxation of the junction current after switching to the LRS at different temperatures and the results are shown in Fig. 2(g). The junction current has been normalized to the initial current and the measuring voltage pulse is 0.01 V. It can be seen that the junction current roughly follows the Curie-von Schweidler law with $J \propto t^{-n}$ [17], where n is a constant and less than 1. As indicated in the inset of Fig. 2(f), the value of n increases exponentially with increasing temperature, which is consistent with the slower component of isothermal discharge current density observed in aromatic polyimide [18]. Among the relaxation mechanisms reported for the Curie–von Schweidler law, the space charge trapping has been used for very large band gap dielectrics, e.g., SiO_2, Al_2O_3, and thin film devices [19, 20]. Peng et al. [21] also indicated that the Curie–von Schweidler behavior is a relatively slow relaxation process and is intimately related to the inevitable presence of a finite amount of disorder, thus the junction current relaxation in LAO/NSTO can be understood by the defects near the interface.

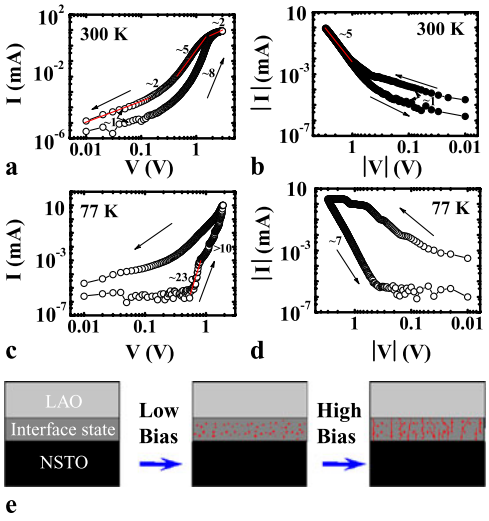

Fig. 3 *I–V* curves of YBCO/LAO/NSTO heterojunction in a double-logarithmic plot at 300 and 77 K with positive bias voltages ((**a**) and (**c**)) and negative bias voltages ((**b**) and (**d**). *Arrows* indicate the directions of voltage change. The values of different slopes are indicated in the plots. (**e**) Schematic picture for carrier transport in YBCO/LAO/NSTO heterojunction

Analyses of the *I–V* curves for LAO/NSTO also suggest the role of traps in the RS effect. Figure 3 shows the double logarithmic plots of the *I–V* curves at different temperatures for the positive (Figs. 3(a) and 3(c)) and negative (Figs. 3(b) and 3(d)) voltage regions. For the positive bias voltages (Figs. 3(a)), the *I–V* curve shows a linear behavior for $V < 0.3$ V, a slope of $2 \sim 3$ for $0.3\ \text{V} < V < 0.7$ V, then a sharp current rise with a slope of 8 for $V > 0.7$ V (V_T) followed by a slope of 2. This behavior can be described by the trap-controlled space charge limited (SCL) conduction mechanism [22] with V_T as the transition voltage from the trap-unfilled to trap-filled SCL regimes. Upon decreasing the voltage, the current retains the higher value indicating that the trapped carriers are not released from the trap centers, which result in the hysteresis of *I–V* curves. The reverse bias voltage (Fig. 3(b)) releases the trapped carriers from the traps, leading to switch to the HRS. This analysis also applies to the low temperature *I–V* curves (Figs. 3(c) and 3(d)). The mean time t spent by a carrier in a trap with depth E_t is proportional to $\exp(E_t/kT)$ [23], where k is Boltzmann's constant. So the mean time that a carrier spends in a trap increases with decreasing temperature. Only deep traps can keep the carriers trapped after the removal of the positive bias voltage and more carriers are trapped at low temper-

atures due to the smaller thermal energy (k_BT). This can account for the experimental observation that the resistive switching effect becomes more remarkable at low temperatures and the resultant dramatic increase of EPIR ratio, and also the slower relaxation at low temperatures with smaller n value.

Based on the above results and analyses, we proposed a model as schematically shown in Fig. 3(e) to account for the RS effect and CER in LAO-NSTO heterostructures. As shown in the previous discussion that the electronic transport of LAO-NSTO is dominated by the interface. Electroforming is expected to introduce some structural disorders or defects at the interface which result in the interface states acting as the trapping centers as shown in the left panel of Fig. 3(e). For the low bias voltages, the electronic transport of LAO-NSTO is dominated by the trap-controlled SCL conduction mechanism (middle panel of Fig. 3(e), traps filled by carries are denoted by red dots and unfilled traps are not shown). The existing trapping centers are gradually occupied by the injected carriers with increasing bias voltage, leading to a remarkable current rise. Further increase of bias voltage results in the formation of paths with low resistance at the interface since all the trapping centers in the paths are occupied (right panel of Fig. 3 (e), red lines express the paths in which all the traps are filled). In contrast, large negative bias voltages release the carriers from the trapping centers and close the low resistance paths, which lead to the current decrease (increase of the resistance). It should be mentioned that band bending should occur at the interface of LAO/NSTO leading to the asymmetry in the interfacial band structure, and the trap-controlled SCL conduction in the interface region dominates the electronic transport process of LAO/NSTO.

In summary, the electronic transport property of LAO-NSTO heterostructures has been investigated. *I–V* curves of these heterostructures show a remarkable resistance switching effect with a remarkable temperature dependence. The relaxation of junction current after switching follows the Curie-von Schweidler law $J \propto t^{-n}$ with an exponential increase of n with temperature. The results can be explained by the trap-controlled space charge limited conduction process via defects near the interface of the heterostructure.

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