Appl Phys A (2011) 102: 901–907
DOI 10.1007/s00339-011-6271-x

Applied Physics A
Materials Science & Processing

A study of the switching mechanism and electrode material of fully CMOS compatible tungsten oxide ReRAM

W.C. Chien · Y.C. Chen · E.K. Lai · F.M. Lee · Y.Y. Lin · Alfred T.H. Chuang · K.P. Chang · Y.D. Yao · T.H. Chou · H.M. Lin · M.H. Lee · Y.H. Shih · K.Y. Hsieh · Chih-Yuan Lu

Received: 30 September 2010 / Accepted: 22 December 2010 / Published online: 26 January 2011
© Springer-Verlag 2011

Abstract Tungsten oxide (WO_X) resistive memory (ReRAM), a two-terminal CMOS compatible nonvolatile memory, has shown promise to surpass the existing flash memory in terms of scalability, switching speed, and potential for 3D stacking. The memory layer, WO_X, can be easily fabricated by down-stream plasma oxidation (DSPO) or rapid thermal oxidation (RTO) of W plugs universally used in CMOS circuits. Results of conductive AFM (C-AFM) experiment suggest the switching mechanism is dominated by the REDOX (Reduction-oxidation) reaction—the creation of conducting filaments leads to a low resistance state and the rupturing of the filaments results in a high resistance state. Our experimental results show that the reactions happen at the TE/WO_X interface. With this understanding in mind, we proposed two approaches to boost the memory performance: (i) using DSPO to treat the RTO WO_X surface and (ii) using Pt TE, which forms a Schottky barrier with WO_X. Both approaches, especially the latter, significantly reduce the forming current and enlarge the memory window.

W.C. Chien (✉) · Y.C. Chen · E.K. Lai · F.M. Lee · Y.Y. Lin · A.T.H. Chuang · K.P. Chang · M.H. Lee · Y.H. Shih · K.Y. Hsieh · C.-Y. Lu
Emerging Central Lab., Macronix International Co., Ltd., Hsinchu, Taiwan, ROC
e-mail: wcchien@mxic.com.tw
Fax: +886-3-5789087

E.K. Lai
Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan, ROC

Y.D. Yao
Department of Physics and Institute of Applied Science and Engineering, Fu Jen University, Taipei, Taiwan, ROC

T.H. Chou · H.M. Lin
National Nano Device Laboratories, Hsinchu, Taiwan, ROC

1 Introduction

Although progressing at astonishing speed, the mainstream floating gate Flash memory is facing fundamental limits that threaten its continued scaling. Thus, non-charge-based memories such as phase change memory (PCM), spin torque transfer MRAM (STT-MRAM), and resistive RAM (ReRAM) have attracted much attention because of their promise for scaling below 10 nm, and for their potential for 3D stacking. ReRAM is particularly attractive due to its simple structure and process. A popular ReRAM material is transition metal oxide, including TiO_X [1, 2], NiO_X [3, 4], MoO_X [5], CuO_X, TaO_X, and CoO_X [6].

WO_X-based ReRAM is especially interesting because (i) it does not introduce any new material, and (ii) the device is built on the existing W plug that is universally used in CMOS circuits. It is also the simplest process, requiring only one extra mask [7]. In 2007, we reported a down-stream plasma oxidation (DSPO) WO_X ReRAM. The DSPO device exhibited remarkable electrical performance, such as high endurance, high speed, and good high temperature data retention [7]. However, the device required large programming current and had a limited resistance window. Thus in 2009 we proposed a RTO (rapid thermal oxidation) process to replace DSPO. Devices made with RTO WO_X showed a larger resistance window, smaller programming current, and tighter operation voltage distributions [8]. In this paper, we examine the memory mechanism of WO_X ReRAM, explain why RTO is superior to DSPO, and propose two approaches to optimize the WO_X ReRAM performance.

2 Process

Figure 1(a) shows the schematic process flow of the self aligned WO_X ReRAM. The flow starts from the conventional W-plug process. After W CMP, the top surface of the W plug is oxidized by DSPO [7] or RTO [8] to create the WO_X memory layer with the remaining W plug serving as the bottom electrode (BE). The top electrode (TE) is then deposited by sputtering tool, often as a part of the metal layer contacting the W plug. Only one additional mask is required to remove the WO_X outside of the memory array. Note that the top portion of the TiN adhesion layer in the plug is converted into highly resistive $TiNO_X$ thus there is no danger of shorting through the liner TiN. TEM images of the DSPO and RTO WO_X cells with 0.18 µm contact size are shown in Fig. 1(b) and (c), respectively. Thickness of the DSPO and RTO WO_X layers is 660 Å and 140 Å, respectively.

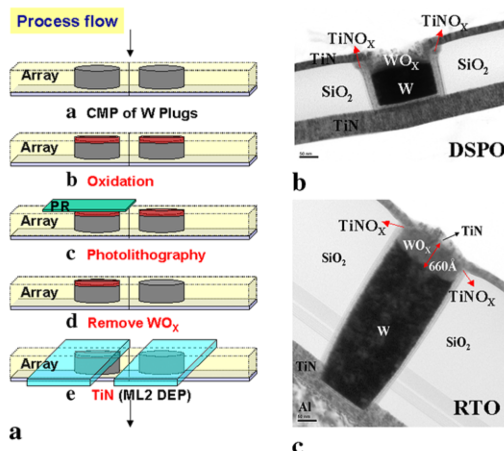


Fig. 1 (**a**) The WO_X ReRAM process that is completely CMOS compatible. TEM images of (**b**) a down-stream plasma oxidation (DSPO) WO_X cell and (**c**) a rapid thermal oxidation (RTO) WO_X cell

3 Switching mechanisms

Figures 2(a) and (b) show the intrinsic resistance vs. pulse voltage (R–V) characteristics after positive and negative pulses. The output resistance value is defined by 0.25 V read voltage. Positive pulses (RESET pulses) on the TiN TE switch the device to the high resistance state (HRS); negative pulses (SET pulses) cannot increase the resistance no matter how large the pulse amplitude is. This indicates that the switching mechanism of the WO_X ReRAM is very polarity dependent, and may be related to oxygen ion movement under high electric field.The asymmetrical response to biasing polarity also indicates that the switching is unlikely to occur in the bulk of WO_X but rather either at the bottom WO_X/W interface or at the top TiN/WO_X interface.

In order to identify the switching location, a symmetric structure TiN/WO_X/TiN with two TiN/WO_X interfaces is specially designed, as shown in Fig. 3. When negative pulses are applied to the cell, oxygen ions are pushed away from the top interface, changing the resistance to low (Step 1, SET). When enough oxygen ions are accumulated at the bottom interface, a high resistance state is created (Step 2, RESET). After the negative pulses, the pulse polarity is switched to positive, and the amplitude is gradually increased from 0 to 4 V. The resistance first decreases (Step 3, SET) and then increases (Step 4, RESET) behaving symmetrically as in Steps 1–2. Thus a symmetric structure such as TiN/WO_X/TiN switches symmetrically while an asymmetric structure (such as TiN/WO_X/W) switches asymmetrically. From these results we can conclude that the switching occurs at the TiN/WO_X interface.

Figure 4 shows WO_X cells with different TEs: TiN, Ti, W, and Al, and their resistance windows. Although all the cells have the same WO_X/W plug structure, the electrical properties depend heavily on the TE. The resistance windows for cells using TiN, Ti, and W TEs are 5 K/50 KΩ, 0.3 K/3 KΩ, and 0.2 K/1 KΩ, respectively. TiN is clearly a better TE than Ti, and W. More interesting is that there is no resistive switching for cells with Al TE. This strongly suggests that TE plays an important role for ReRAM memory

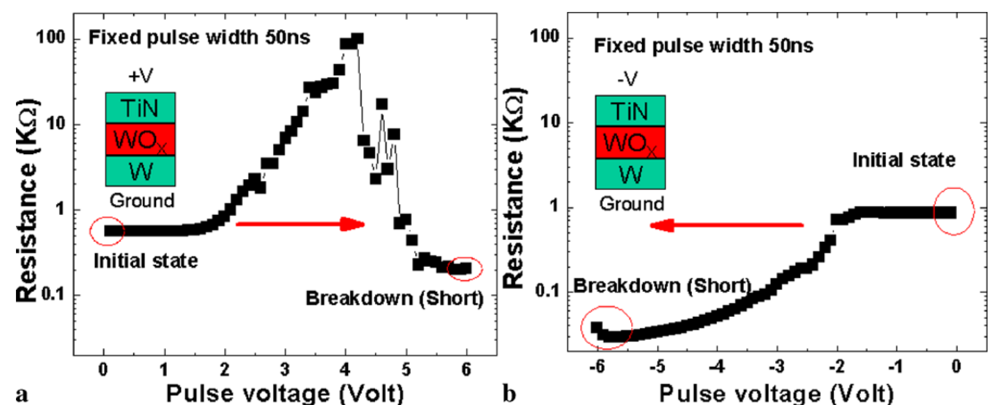


Fig. 2 (**a**) Resistance of a WO_X cell increases after applying a positive pulse. However, the resistance may drop to very low if the pulse amplitude is too high (>4 V). (**b**) Negative pulses do not increase the device resistance

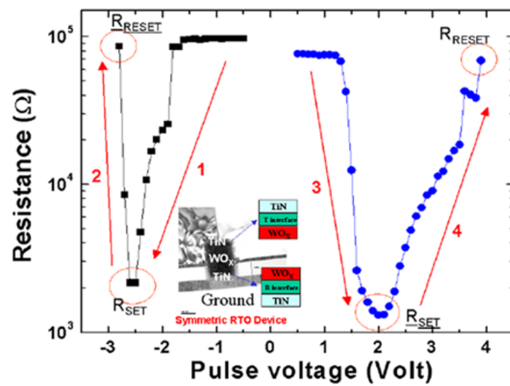


Fig. 3 A symmetric TiN/WO_X/TiN structure (*the insert*) shows symmetric resistive switching behavior. The structure is equivalent to two WO_X cells that are back-to-back connected. Step 1 is SET at the top interface. Step 2 is RESET at the bottom interface. Step 3 is SET at the bottom interface. Step 4 is RESET at the top interface

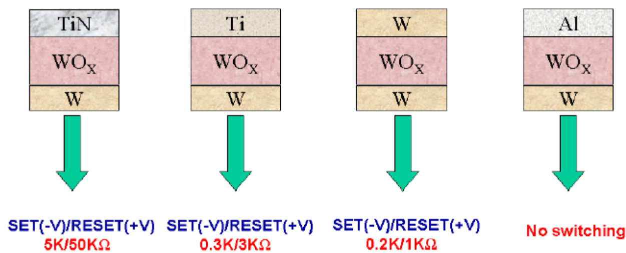


Fig. 4 Comparison with WO_X ReRAM with different top electrodes TiN, Ti, W, and Al

property and performance. TiN has better oxygen-blocking ability than Al. Therefore, TE material has to be oxygen-inert and oxygen-blocking when designing WO_X ReRAM.

Besides the switching location, we also investigated the switching mechanism of WO_X ReRAM by atomic force microscopy (AFM) and conductive AFM (C-AFM). A WO_X cell with a 0.5 μm contact hole was examined by AFM (Fig. 5(a)) and the WO_X surface was clearly distinguished. The same cell was then mapped by a conductive AFM, as illustrated in Fig. 5(b). The AFM tip was grounded with a 0.1 V external bias connected to the W bottom electrode. The C-AFM scan of the initial low resistance state is shown in Fig. 5(c). The dark areas represent local conducting paths that are responsible for the low initial resistance. Even after the oxidation process, the WO_X is not a good insulator because of these conducting paths. Interestingly, by applying a current through the AFM tip these conducting paths are eliminated (Fig. 5(d)) probably through oxidation caused by Joule heating.

Based on the TE dependence and the C-AFM observations, we propose that the switching mechanism for WO_X ReRAM is an electrochemical REDOX reaction as formulated in (1)—the low resistance state (LRS) is caused by the creation of conductive WO_{3-n} filaments while the high re-

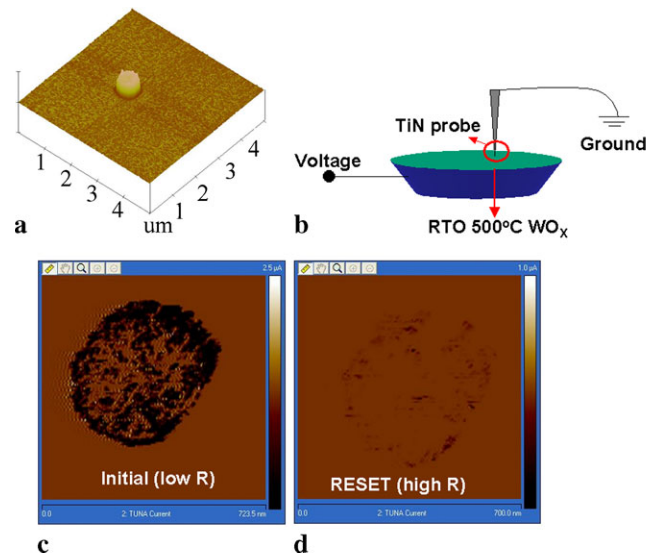
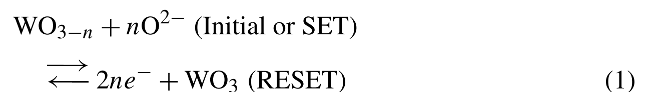


Fig. 5 (**a**) An AFM image of a WO_X cell built on a 0.5 μm contact hole. (**b**) Apparatus of conductive AFM (C-AFM), which is used to test the WO_X cell. (**c**) The C-AFM images of the initial state. A *dark area* represents a leaking path. (**d**) RESET state created by applying voltage through C-AFM to the WO_X cell

sistance state is by the rupturing of the filaments that restores the insulating WO_3. This REDOX mechanism has previously been proposed for other transition metal oxide ReRAM's [9, 10] although the behavior of WO_X is quite different from others



$$WO_{3-n} + nO^{2-} \text{ (Initial or SET)} \rightleftarrows 2ne^- + WO_3 \text{ (RESET)} \quad (1)$$

The unique forming process [7, 8, 11–13] for WO_X ReRAM, which starts from a LRS and requires high RESET voltage to form (other TMO devices start at HRS and requires a breakdown operation to form), can be well explained by our mechanism, as shown in Fig. 6. After DSPO or RTO, conductive leakage paths exist on the WO_X surface due to incomplete oxidation to form WO_3. Beneath the surface, the oxygen concentration is lower, so the major compositions are W_2O_5 and WO_2 (both are conductive), which serves as oxygen reservoir for oxygen ions to the active layer above. During forming, a positive voltage draws O^{2-} ions from the underneath oxygen reservoir to the TE/WO_X interface and converts the leaky WO_{3-n} into insulating WO_3. After forming, the resistance becomes high. Thus the forming process is a repair action that creates a perfect insulating WO_3 surface layer that the oxidation process fails to accomplish. After the forming process, the SET and RESET operations are just the building and rupturing of conducting filaments in the reactive layer (mostly composed of WO_3), similar to other TMO devices.

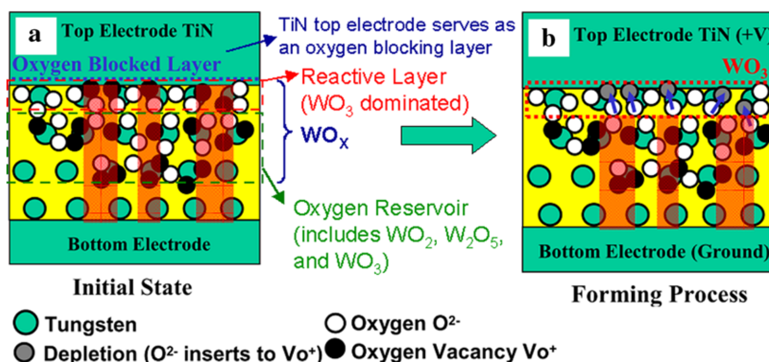


Fig. 6 Proposed WO_X ReRAM forming mechanism. (**a**) Many oxygen vacancies are present in the WO_X film coagulating into conducting paths. (**b**) During the forming process, the positive voltage drives oxygen atoms into vacancies to form WO_3 near the top electrode

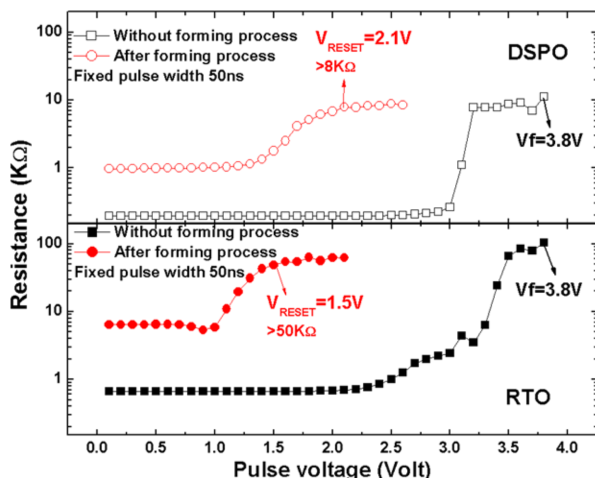


Fig. 7 Pulse R–V curves prior and after the forming process for DSPO and RTO devices, respectively

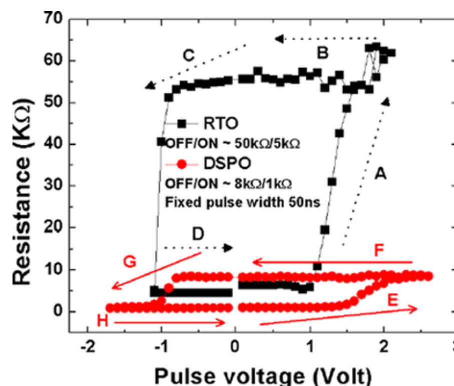


Fig. 8 Hysteresis loop of pulse R–V curves for DSPO and RTO devices

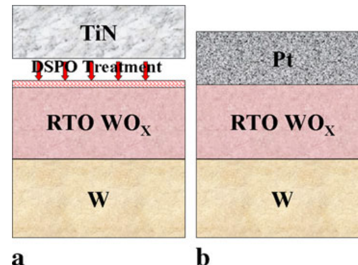


Fig. 9 Two proposed new TE/WO_X interfaces to increase WO_X ReRAM memory performance—(**a**) using DSPO to treat a RTO WO_X layer, (**b**) a using Pt TE

4 Comparison of DSPO and RTO

Figure 7 shows the pulse R–V characteristics before and after the forming process for DSPO and RTO devices. For virgin cells by either DSPO or RTO, a large forming pulse around 4 V/50 ns is required to bring the cells to the high resistance state. After that, the cells can be operated by smaller pulses. Nevertheless, there is a 10× difference in resistance between RTO and DSPO cells for both the RESET and the SET states. It is clear the oxidation process does affect the electrical property of the WO_X ReRAM. The detailed switching characteristics of DSPO and RTO cells are compared in Fig. 8. The larger resistance window and lower operation current make RTO cells more preferred for memory applications.

That the RTO cells are superior to the DSPO cells can be explained by X-ray photoelectron spectroscopy (XPS) analysis [14]. The DSPO cells have a reactive layer (major composition is WO_3) about 2 nm and oxygen reservoir (major composition includes W_2O_5 and WO_2) underneath is about 6 nm. On the other hand, RTO cells have thicker reactive layer and thicker oxygen reservoir due to higher process temperature [15]. A thicker reactive layer results in a larger resistance window. Besides, the RTO cell shows higher endurance than the DSPO cell. This may come from the thicker oxygen reservoir that can more efficiently replenish oxygen ions to the reactive layer for the loss from the TiN/WO_X interface to TiN TE during cycling. A detailed understanding however, is still needed, and will be a subject for future study.

5 TE/WO_X interface engineering

With an understanding of the switching mechanism we have designed two new TE/WO_X structures, as illustrated in Fig. 9, to improve the performance. The first uses a two-step

oxidation process (Fig. 9(a))—adding a DSPO treatment to the RTO WO_X. The pulse R–V curve of the RTO + DSPO device is compared with those from pure DSPO and pure RTO cells (Fig. 10). The RTO + DSPO cell shows an even better resistance window than the other two. Moreover, the forming voltage is reduced from 4 V to 3.3 V. These improvements are believed to come from the increased oxygen content in the WO_X reactive layer by the DSPO.

The second new structure is to use Pt TE in the RTO WO_X cell (Fig. 9(b)). Figure 11(a) shows that the J–V curves of the new Pt/WO_X/W device are very sensitive to temperature. The curves can be well modeled by thermionic emission (2), where A* is the effective Richardson constant ($= 120\ \mathrm{A\,cm^{-2}\,K^{-2}}$), T the absolute temperature, Φ_B the barrier height, and ε_i the insulator permittivity. The effective barrier height, extracted from the Pt devices, is 0.44 eV. Figure 11(b) shows the $\ln(J/T^2)$ versus $1/k_BT$ curve for Pt/WO_X/W at various bias voltages. This barrier lowering by electric fields, further confirms there is a Schottky barrier formed at the Pt/WO_X interface and that thermionic emission dominates the conduction mechanism of the Pt TE cell [16]

$$J = (A*) * T^2 \exp\left(\frac{q\sqrt{qE/4\pi\varepsilon_i}}{k_BT} - \frac{q\Phi_B}{k_BT}\right) \quad (2)$$

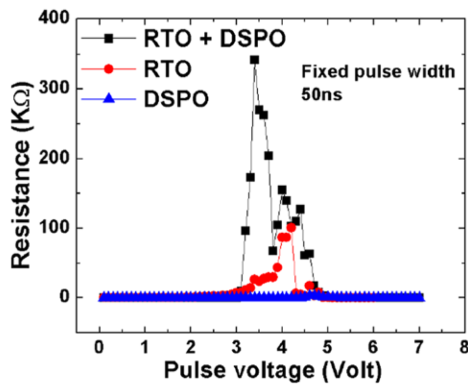


Fig. 10 Pulse R–V curve for DSPO, RTO, and RTO with DSPO treatment cells, respectively

Contrary to the TiN TE cells, the initial resistance of the Pt cells is high so the forming of this Pt device is to bring the resistance from high to low, rather from low to high. The forming process of the Pt device seems a soft breakdown process that creates conduction path(s) through the Pt/WO_X barrier and gives the cell a low resistance state. After the forming, the Pt cell can be operated by conditions very similar to the TiN cell—typically, a positive pulse of 1.5 V/50 ns is enough to RESET the WO_X device while a negative pulse of −1.5 V/50 ns can SET the cell. The corresponding R–V curves of the Pt cell are plotted in Fig. 12(a). Cycling endurance of the Pt cell is shown in Fig. 12(b); the resistance

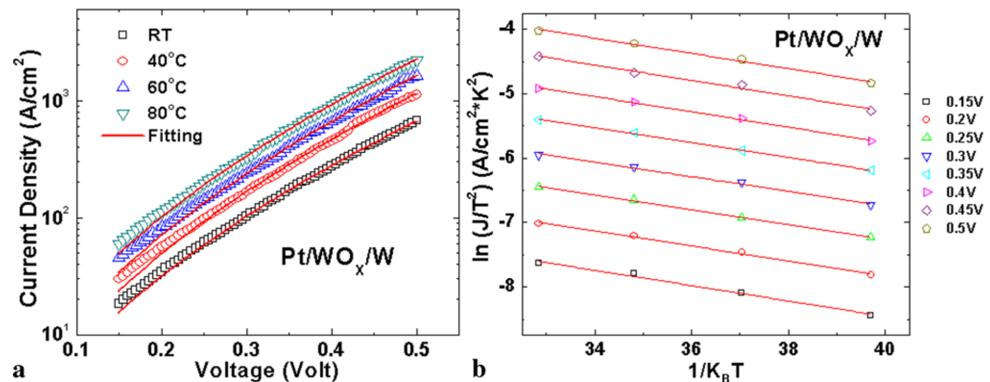


Fig. 11 (**a**) J–V curves and thermionic emission fitting results for the initial state of Pt/WO_X/W at 25, 40, 60 and 80°C. (**b**) $\ln(J/T^2)$ versus $1/k_BT$ curves for Pt/WO_X/W at various bias voltages. The behaviors are well predicted by thermionic emission

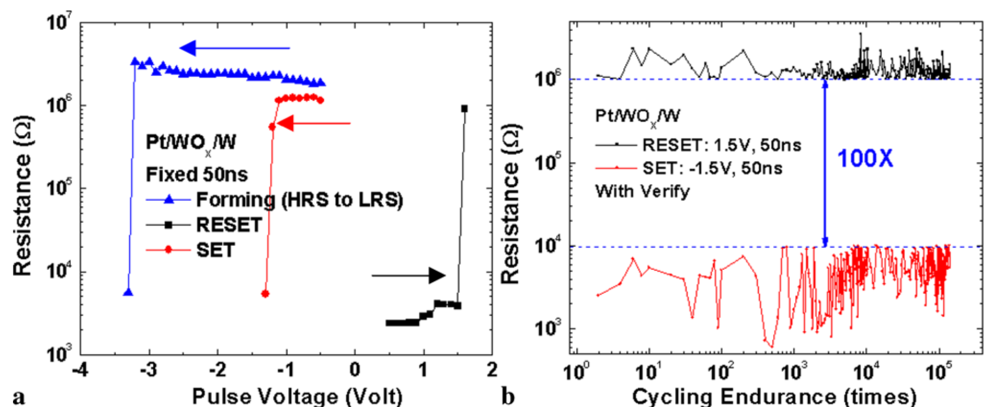


Fig. 12 (**a**) Forming, RESET, and SET pulse R–V curves of a Pt/WO_X/W cell. (**b**) Cycling characteristics of the Pt/WO_X/W cell. A RESET/SET resistance window is well separated at 1 MΩ/10 KΩ for >100 K cycles

Table 1 Performance table for DSPO, RTO, RTO + DSPO, and Pt/RTO WO_X/W cells

	Forming voltage	Forming current (A/cm^2)	SET current (A/cm^2)	RESET current (A/cm^2)	HRS (ohm)	LRS (ohm)	Endurance (times#)
DSPO	4V, 50ns (LRS to HRS)	$1*10^8$	$1*10^7$ (-1V, 50ns)	$1.3*10^7$ (2V, 50ns)	8K	1K	>10K
RTO	4V, 50ns (LRS to HRS)	$8*10^7$	$3.3*10^6$ (-1.5V, 2ns)	$3.4*10^6$ (1.8V, 2ns)	100K	10K	>100K
RTO add DSPO	3.3V, 50ns (LRS to HRS)	$4.7*10^7$	$4.9*10^6$ (-1.2V, 50ns)	$4.9*10^6$ (1.2V, 50ns)	200K	10K	>100K
Pt/RTO WO_X/W	-3.5V, 50ns (HRS to LRS)	$1.2*10^6$	$1.6*10^6$ (-1.5V, 50ns)	$3.5*10^6$ (1.5V, 50ns)	1M	10K	>100K

window with two orders of resistance change is well maintained by a program-verify algorithm [8] even after 100 K cycles.

Table 1 summaries the performance of different WO_X devices, including DSPO, RTO, RTO + DSPO, and the RTO cell with a Pt TE. Generally, RTO cells have superior performance than DSPO cells in all performance indices. Using RTO + DSPO can slightly reduce the forming voltage and current while the resistance window is increased by 100%.

Devices using RTO WO_X and Pt TE show the best performance. The Schottky barrier at the Pt/WO_X interface not only changes the forming property but also improves the memory performance. The forming current density is reduced to 1.2×10^6 A/cm^2, which is 50× smaller than that of the RTO device using TiN TE. The resistance window is also larger than the RTO devices. The operation voltages for RESET and SET are below ±2V, suitable for low voltage operation.

6 Conclusion

The switching mechanism of WO_X ReRAM was studied by using C-AFM, various structures including asymmetric TiN/WO_X/W and symmetric TiN/WO_X/TiN devices, and cells with different TEs. Our experimental results suggest that the switching occurs at the TE/WO_X interface through a REDOX reaction. Thus the TE material plays a very important role and we propose using either a two-step oxidation process (RTO + DSPO) or a Pt TE to further improve the performance of WO_X ReRAM. The RTO + DSPO device shows a smaller forming voltage and a larger resistance window, and a Pt TE not only significantly improves the resistance window but also reduces the forming current density by 50X. This simple one-mask WO_X ReRAM device is very promising for both high-density storage and embedded memory applications.

References

1. K.M. Kim, B.J. Choi, C.S. Hwang, Localized switching mechanism in resistive switching of atomic-layer-deposited TiO_2 thin films. Appl. Phys. Lett. **90**, 242906 (2007)
2. R.G. Sharpe, P.W. Palmer, Concerted regeneration of electroformed metal-insulator-metal devices. J. Appl. Phys. **79**, 8565 (1996)
3. Y. Ogimoto, Y. Tamai, M. Kawasaki, Y. Tokura, Resistance switching memory device with a nanoscale confined current path. Appl. Phys. Lett. **90**, 143515 (2007)
4. C.B. Lee, B.S. Kang, M.J. Lee, S.E. Ahn, G. Stefanovich, W.X. Xianyu, K.H. Kim, J.H. Hur, H.X. Yin, Y. Park, I.K. Yoo, J.-B. Park, B.H. Park, Electromigration effect of Ni electrodes on the resistive switching characteristics of NiO thin films. Appl. Phys. Lett. **91**, 082104 (2007)
5. D. Lee, D.J. Seong, I. Jo, F. Xiang, R. Dong, S. Oh, H. Hwang, Resistance switching of copper doped MoO_x films for nonvolatile memory applications. Appl. Phys. Lett. **90**, 122104 (2007)
6. H. Shima, F. Takano, H. Akinaga, Y. Tamai, I.H. Inoue, H. Takagi, Resistance switching in the metal deficient-type oxides: NiO and CoO. Appl. Phys. Lett. **91**, 012901 (2007)
7. C.H. Ho, E.K. Lai, M.D. Lee, C.L. Pan, Y.D. Yao, K.Y. Hsieh, R. Liu, C.-Y. Lu, A highly reliable self-aligned graded oxide WO_x resistance memory: conduction mechanisms and reliability, in *Symp. VLSI Tech.* (2007), pp. 228–229
8. W.C. Chien, Y.C. Chen, E.K. Lai, Y.D. Yao, P. Lin, S.F. Horng, J. Gong, T.H. Chou, H.M. Lin, M.N. Chang, Y.H. Shih, K.Y. Hsieh, R. Liu, C.-Y. Lu, Unipolar switching behaviors of RTO WO_X RRAM. IEEE Electron Device Lett. **31**, 126–128 (2010)
9. R. Waser, Electrochemical and thermochemical memories, in *IEDM., Tech. Dig.* (2008), pp. 289–292
10. Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, T. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, M. Oshima, Highly reliable TaO_x ReRAM and direct evidence of redox reaction mechanism, in *IEDM., Tech. Dig.* (2008), pp. 293–296
11. W.C. Chien, Y.C. Chen, E.K. Lai, Y.Y. Lin, K.P. Chang, Y.D. Yao, P. Lin, J. Gong, S.C. Tsai, C.H. Lee, S.H. Hsieh, C.F. Chen, Y.H. Shih, K.Y. Hsieh, R. Liu, C.-Y. Lu, High-speed multilevel resistive RAM using RTO WO_X, in *SSDM* (2009), pp. 1206–1207, G-7-3
12. W.C. Chien, K.P. Chang, Y.C. Chen, E.K. Lai, H. Mähne, Y.D. Yao, P. Lin, J. Gong, S.H. Hsieh, K.Y. Hsieh, R. Liu, C.-Y. Lu, Multi-level switching characteristics for WO_X resistive RAM (RRAM), in *SSDM* (2008), pp. 1170–1171, J-9-5

13. K.P. Chang, W.C. Chien, Y.C. Chen, E.K. Lai, S.H. Hsieh, Y.D. Yao, J. Go, K.Y. Hsieh, R. Liu, C.-Y. Lu, Low-voltage and fast-speed forming process of tungsten oxide resistive memory, in *SSDM* (2008), pp. 1168–1169, J-9-4
14. W.C. Chien, E.K. Lai, K.P. Chang, C.H. Yeh, M.H. Hsueh, Y.D. Yao, T. Luoh, S.H. Hsieh, T.H. Yang, K.C. Chen, Y.C. Chen, K.Y. Hsieh, R. Liu, C.-Y. Lu, Unipolar switching characteristics for self-aligned WO_X resistance RAM R-RAM, in *VLSI-TSA Technical Program Committee, VLSI-TSA, Session 9, T97* (2008), pp. 144–145
15. W.C. Chien, Y.R. Chen, Y.C. Chen, A.T.H. Chuang, F.M. Lee, Y.Y. Lin, E.K. Lai, Y.H. Shih, K.Y. Hsieh, C.-Y. Lu, A forming-free WO_X resistive memory using a novel self-aligned field enhancement feature with excellent reliability and scalability, in *IEDM., Tech. Dig.* (2010), pp. 440–443
16. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley/Central Book Company, New York, 1985), p. 403