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Stress-induced large-area lift-off of crystalline Si films

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ABSTRACT A new implantation-free lift-off process is presented. We deposit a layer with mismatched thermal expansion coefficient with respect to the substrate. Upon cooling, the differential contraction induces a large stress field which is released by the initiation and the propagation of a crack parallel to the surface. The principle is demonstrated on both single and multi-crystalline silicon. Films with an area of $25\,cm^2$ and a thickness of 30–$50\,\mu m$ have been obtained. Some Si layers were further processed into solar cells. An energy conversion efficiency of 9.9% was reached on a $1\,cm^2$ sample.

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1   Context and introduction

The separation of thin layers of crystalline silicon and subsequent transfer to a carrier substrate is of great interest for high-performance integrated circuits based on silicon-on-insulator wafers and potentially also for photovoltaics. The most well-known technique is the SmartCut technology [1], which relies on the weakening by ion implantation of a layer deep in the substrate, enabling to detach the upper part of the substrate. Other technologies also rely on the formation of a weak layer (e.g., porous-silicon), followed by an epitaxial growth of silicon with the desired quality and thickness [2–5]. The costs of these methods are, however, high, especially when the thickness of the silicon film to be produced exceeds a few microns, which limits their application. The method presented here does not require the costly formation of a weak layer. It relies on the stress induced by layers deposited with cost effective techniques, and enables the fabrication of layers of a few tens of microns with a very limited material loss.

2   Experimental proof of principle

The method is schematically described in Fig. 1. A $5 \times 5\,cm^2$ multi-crystalline silicon substrate (thickness $\sim 300\,\mu m$) is used as starting material. We screen-print on top of it a double layer of commercially available metal paste (Fig. 1a). First a layer of $\sim 20\,\mu m$ of Ag paste (DuPont PV146) is printed. The solvents are dried below $200\,°C$ for a few minutes in a belt drier, and the wafer is annealed at high temperature (approximately $900\,°C$) for a few seconds in a belt furnace. On top of the first metal layer, a layer of $\sim 50\,\mu m$ of Al paste (DuPont PV333) is printed, dried and annealed the same way. The metal pastes are printed up to 1 mm from the edge of the substrate. The bonding between the metal layer and the silicon occurs at high temperature, in the belt furnace. Upon cooling down, the metal layers as well as the silicon substrate undergo a thermal contraction, but the mismatch in coefficient of thermal expansion (TCE) between the metal and the silicon induces a high stress field in the substrate (Fig. 1b). To release the stress in the system, the silicon substrate first bends, and then the metal layer suddenly snaps off the parent substrate, peeling off at the same time a silicon layer of approximately $40\,\mu m$ (Fig. 1c). Figure 2 shows a photograph of the resulting substrate Fig. 1a and of the silicon layer lifted-off, still attached to the metal layer Fig. 1b. The substrate is cut along the whole surface but remains otherwise intact. It can in principle be re-used for further additional layer lift-off. The metal layers inducing a permanent stress in the peeled-off wafer are then removed in a metal-etching solution, resulting in a clean and stress-free silicon layer (Fig. 1d). Total reflection X-ray fluorescence measurements were carried out, which revealed no detectable trace of metals.

Figure 3 displays a scanning electron microscopy (SEM) cross section of the flat and clean wafer obtained. The thickness is approximately $40\,\mu m$ and is relatively constant over the whole sample. No crack is visible, despite the high stress undergone by the Si layer during the lift-off process. The two surfaces exhibit different topologies: the surface that was in contact with the metal is very rough. Potentially, this roughness can be advantageously used for light trapping in photovoltaic applications.

The resulting thin silicon film was processed into a solar cell with an amorphous-Si/crystalline-Si heterojunction emitter, as described elsewhere [6]. The heterojunction emitter was deposited on the surface that exhibits the wavy fracture patterns. This same surface was exposed to standard AM1.5 light. The cell had an area of $1 \times 1\,cm^2$ and reached an energy conversion efficiency of 9.9% (see Table 1). The fill

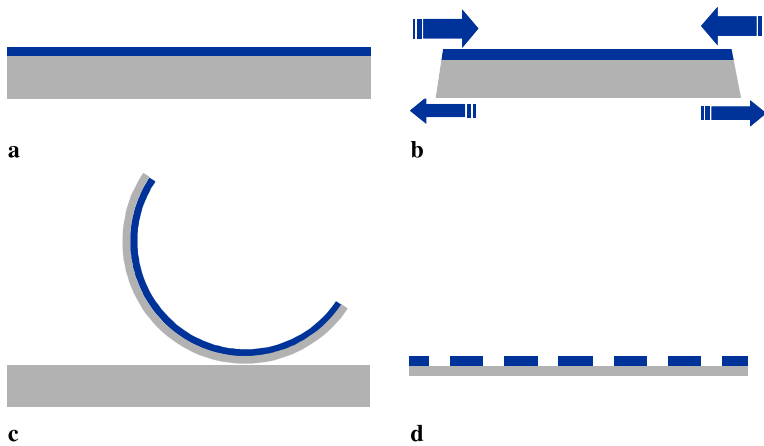✉ Fax: +32 16 28 15 01, E-mail: frederic.dross@imec.be

FIGURE 1 Schematic description of the method proposed to produce thin silicon films. (**a**) Metal deposition, (**b**) Decrease in temperature to induce stress (**c**) Peeling of the top layer, (**d**) Cleaning and stress removal by chemical etching
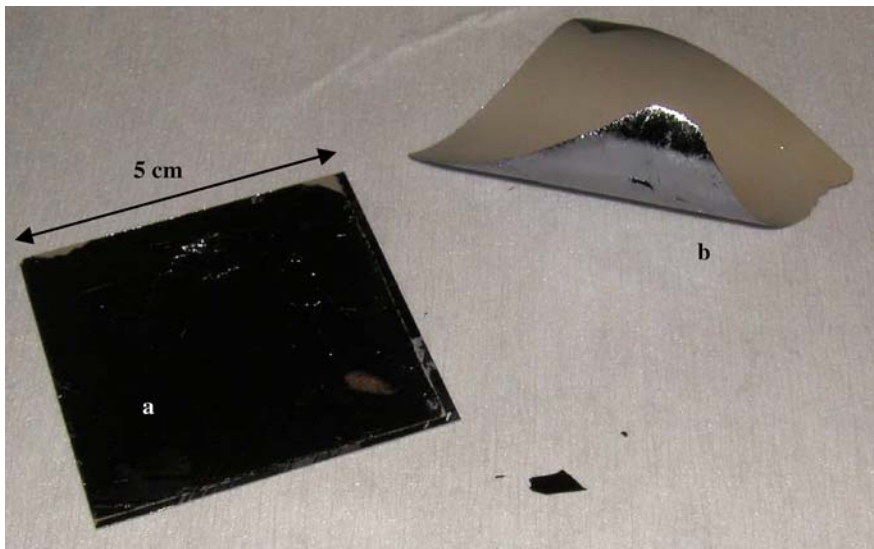

FIGURE 2 Photograph of the structure after the top layer has been peeled off the parent substrate (25 cm^2). The parent substrate (**a**) can be re-used for additional layer lift-off, and the top silicon layer (**b**) is still attached to the stress-inducing layer

factor was low due to some series resistance issues related to processing. The open-circuit voltage and short-circuit current values are poor in comparison with standard Si solar cells, because of the very thin base, the absence of back-surface passivation, and the lack of intentional surface texturing. Nevertheless these still good results indicate that the electronic quality of the material, as well as most probably its crystalline structure, are largely preserved during the lift-off process in spite of the high stress values involved.

3 Modeling and discussion

The misfit stress in the film, induced by the TCE mismatch during cooling from the temperature of bonding T_0 to the lift-off temperature $T_1 < T_0$, is given, under the assumptions of homogeneous, isotropic and linearly elastic materials, by the relation [7]:

$$\sigma = (\alpha_f - \alpha_s)(T_0 - T_1) E_f / (1 - \nu_f) ,$$

with $\alpha_{f,s}$ the TCE of the film and of the substrate, E_f the Young's modulus of the film, and ν_f the Poisson's constant of the film. The film is under tensile stress, whereas the substrate undergoes compressive stress. If the stress exceeds the fracture strength of the substrate, a crack will initiate and propagate in the bulk of the substrate. Assuming a homogeneous defect density, the crack will start from the first location submitted to a stress intensity factor exceeding the fracture toughness of the substrate. The precise trajectory of the crack depends on the thermo-mechanical parameters of the system. The crack can either cut through the whole substrate, propagate along the film-substrate interface, or select a path parallel to the surface at a certain depth inside the substrate, and propagate longitudinally along this path. The latter is known as substrate spalling and requires, to be activated, a minimum thickness of the film given by [7]:

$$h = \Gamma_s E_f / Z \sigma^2 ,$$

with Γ_s, the fracture resistance of the substrate (energy density threshold expressed in J/m^2 assumed isotropic), and Z a dimensionless driving force [8] depending on the cracking pattern and elastic mismatch between the film and the substrate. Assuming elastical homogeneity and a semi-infinite substrate, $Z = 0.343$ [7] for substrate spalling.

In order for the crack to propagate parallel to the surface through the whole substrate, pure mode I (opening mode, introduced by a tensile stress normal to the plane of the crack) stress load is required during the crack propagation [9]. The phenomenon was modeled using a simple 2D finite element analysis tool (AutoFEA), with assumption of linear and isotropic thermo-mechanical behavior of the investigated materials (the TCE for the film and for the substrate were taken equal to respectively 2.2×10^{-4} K^{-1}, and 2.6×10^{-6} K^{-1}). The structure is modeled as a substrate of finite thickness d_s, and a film of thickness $d_f = d_s/5$. The film does not extend up to the edge of the substrate. After cooling down ($T_0 - T_1 = 950$ K), the

J_{sc}	V_{oc}	FF	Efficiency
26.7 mA cm^{-2}	550 mV	67.8%	9.9%

TABLE 1 Electrical characteristics under standard AM1.5 illumination of the 1 cm^2 solar cell processed on a sample obtained with the new lift-off technique. J_{sc} is the short-circuit current, V_{oc} is the open-circuit voltage, and FF is the fill-factor of the illuminated cell
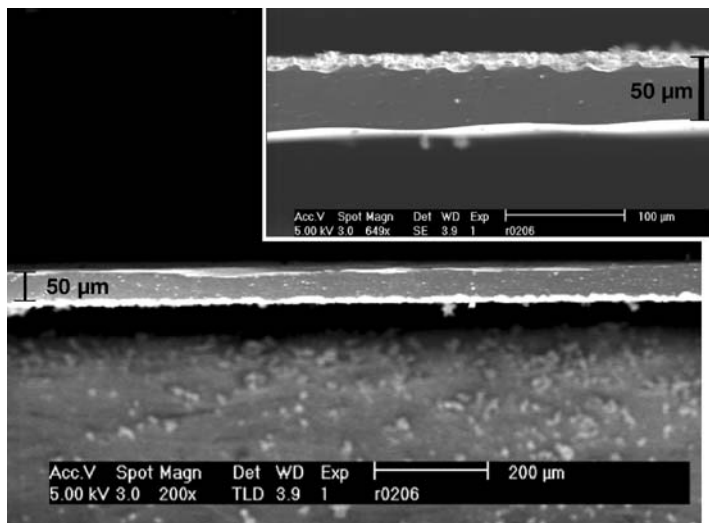
FIGURE 3   SEM pictures of the film after flattening and metal-cleaning of the bi-material
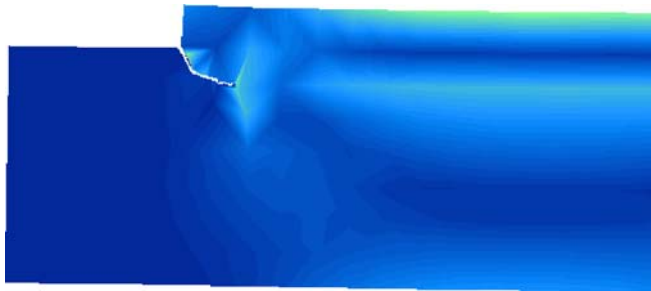

FIGURE 4   Von Mises stress map of the structure after propagation of the crack perpendicular to the principal stress at the maximum stress point. The crack was propagated 20 times. In *light color* are the areas with higher stress. The structure was modeled with the finite element software AutoFEA

maximum stress is found at the edge of the interface between the film and the substrate. From the calculated shear and normal stress values, we can estimate the principal direction of stress on this point. Assuming perfectly brittle behavior, the crack will spring open in a direction normal to the principal stress. By changing the topology of the structure (additional node and re-calculated mesh), we propagate the crack along the calculated direction of propagation by a propagation length $l = d_f/10$. This process is repeated 20 times to observe how the direction of propagation evolves while the structure is opening. The resulting (opened) structure is presented on Fig. 4. Due to symmetry reasons, only half of the structure was modeled. The crack starts in an oblique direction (49° from normal to the surface) and converges towards an overall direction parallel to the substrate surface. Figure 4 also presents the Von Mises stress map of the opened structure. The Von Mises stress is an arithmetic function of the components of the stress tensor that gives an appreciation of the overall magnitude of the tensor. It is used here as a qualitative estimation of the stress distribution. After propagating the crack 20 times in the structure, the crack tip is still the point of highest stress. At a certain depth depending on the materials mechanical parameters, the mode II (sliding mode, introduced by a shear stress acting parallel to the plane of the crack and perpendicular to the crack front) stress load vanishes, and the crack trajectory remains parallel to the surface.

The simple simulation presented here proves that the process is purely mechanical and that there is no need to include any inhomogeneity (weak plane) or anisotropy (cleavage plane) to explain the phenomenon. More accurate calculations are nonetheless needed to obtain quantitative information. The concept was demonstrated on multi-crystalline material, proving that the method does not require a specified crystal orientation. The process was also applied successfully to ⟨100⟩ and ⟨111⟩-oriented single Si crystals.

We anticipate that the thickness of the lifted-off film can be tuned to custom needs within a certain range by changing the mechanical parameters and/or the thickness of the stress-inducing paste. For photovoltaic applications the thickness of 30–50 µm experimentally obtained is actually close to the theoretical optimum value needed to obtain the highest efficiency under 1-sun illumination when the performances are limited by Auger recombination [10].

4   Conclusion

A new method to peel off thin crystalline Si layers from a Si wafer has been described. A layer with a mismatched TCE is bonded to a Si wafer at high temperature. The whole system is cooled down and the stress induced by the differential thermal contraction induces a crack in the substrate. Under certain conditions the crack propagates in the direction parallel to the surface at a depth of a few tens of microns, and peels off the top layer of the substrate. This method is purely based on the thermo-mechanical behavior of silicon and of screen-printed pastes and does not require the formation of a weak layer in the silicon substrate. Although the method is demonstrated on Si wafers, it might be applicable to other materials. Films with an area of 25 cm^2 and a thickness of 30–50 µm have been obtained. A simple solar cell process was performed on a 1 cm^2 sample and an efficiency of 9.9% was reached. This lift-off process has the potential to drastically reduce the Si consumption for Si solar cells, thereby lowering costs and energy payback time.

REFERENCES

1 M. Bruel, Electron. Lett. **31**, 1201 (1995)
2 R. Brendel, Japan. J. Appl. Phys. **40**, 4431 (2001)
3 C.S. Solanki, R.R. Bilyalov, H. Bender, J. Poortmans, Phys. Stat. Solidi A **182**, 97 (2000)
4 K.J. Weber, A.W. Blakers, K.R. Catchpole, Appl. Phys. A **69**, 195 (1999)

5 K. Sakaguchi, K. Yanagita, H. Kurisu, H. Suzuki, K. Ohmi, T. Yonehara, Electrochem. Soc. Proc. **99**, 117 (1999)

6 L. Carnel, I. Gordon, D. Van Gestel, G. Beaucarne, J. Poortmans, A. Stesmans, J. Appl. Phys. **100**, 063 702 (2006)

7 J.W. Hutchinson, Z. Suo, Adv. Appl. Mechan. **29**, 63 (1992)

8 A.G. Evans, M.D. Drory, M.S. Hu, J. Mater. Res. **3**, 1043 (1988)

9 Z. Suo, J.W. Hutchinson, Int. J. Solids Struct. **25**, 1337 (1989)

10 M.A. Green, J. Zhao, A. Wang, S.R. Wenham, IEEE Trans. Electr. Dev. **46**, 1940 (1999)