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Influence of the substrate temperature during deposition on film characteristics of copper phthalocyanine and field-effect transistor properties

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ABSTRACT In this paper, we employ different substrate temperatures during the deposition process and observe a highly ordered structure and strong orientation of copper phthalocyanine (CuPc) molecules on Si/SiO_2 by using X-ray-diffraction and transmission electron microscopy analysis. The results show the effect of CuPc morphology at different substrate temperatures on the organic field-effect-transistor performance. When the substrate temperature for deposition of CuPc is 120 °C, a mobility of 3.75×10^{-3} cm^2/V s can be obtained.

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1 Introduction

Organic semiconductor thin films have attracted much attention due to their successful applications in optical and electronic devices [1, 2], such as organic light-emitting diodes and field-effect transistors (FETs). Recently, it has been shown that the ordering and orientation of the molecules is crucial for the performance of organic field-effect transistors (OFETs) [3, 4]. The preferred orientation of the crystallites is usually determined by sample-preparation conditions of the thin films, for example substrate temperature (T_{sub}), type of substrate (amorphous or single crystalline), deposition rate, and quality of the substrate surface [5]. In addition, the morphology of the thin-film surface depends decisively on the sample-preparation conditions.

Phthalocyanines (Pcs) represent one of the most promising candidates for modern opto-electronic devices, such as optical recording, gas sensors, field-effect transistors, and solar cells [6–9], as these systems offer outstanding optical and electrical properties, excellent film-growth properties, and chemical stability [10–12]. They can easily be sublimed, resulting in high-purity thin films without decomposition. The effects of substrate temperature on the properties of CuPc thin films have been reported in the literature [13–15]. In these studies, the Pc materials were always deposited on glass, Al, or Au substrates. However, because the FET experiment is often carried out on a SiO_2/Si substrate, it is also necessary to study the growth behavior of CuPc on a SiO_2 surface, which can reflect directly the relationship between the film structure and the FET properties. Therefore, the knowledge of the surface morphology and the preferred orientation of the crystallites on a SiO_2/Si substrate is essential for their successful applications [16–18]. Moreover, the transistor properties of these compounds are still poor. Mobilities of an OFET based on NiPc and CuPc at room substrate temperature of around 10^{-4} cm^2/V s were reported [19, 20].

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In this letter, the influences of different deposition conditions on the preferred orientation of CuPc crystallites within the films and on the surface morphology are investigated by X-ray diffraction (XRD) and transmission electron microscopy (TEM) analysis. We observed variable ordering and orientation of CuPc molecules on Si/SiO_2 at different substrate temperatures during the deposition process, which affects directly the morphology of the thin films. The results show the effect of CuPc morphology at different substrate temperatures on the transistor performance. When the substrate temperature for deposition of CuPc is 120 °C, a mobility of 3.57×10^{-3} cm^2/V s can be obtained.

2 Experimental

The chemical structure of CuPc is shown in Fig. 1a. CuPc was synthesized in our laboratory and purified three times using vacuum sublimation at 10^{-5} Torr or lower. For morphological studies, CuPc was vacuum evaporated onto Si/SiO_2 and carbon-coated electron microscope grids simultaneously with the OFET at different substrate temperatures of 20, 120, 170 and 200 °C. The deposited films were of about 50-nm thickness; those used for electron microscopy were examined in a JEOL transmission electron microscope at 100 kV. CuPc films on Si/SiO_2 were used for X-ray-diffraction studies in the reflection mode at 45 kV and 300 mA and with Cu K_α radiation from a 2-kW Rigaku X-ray diffractometer.

The organic FETs of CuPc were constructed as shown in Fig. 1b. OFETs

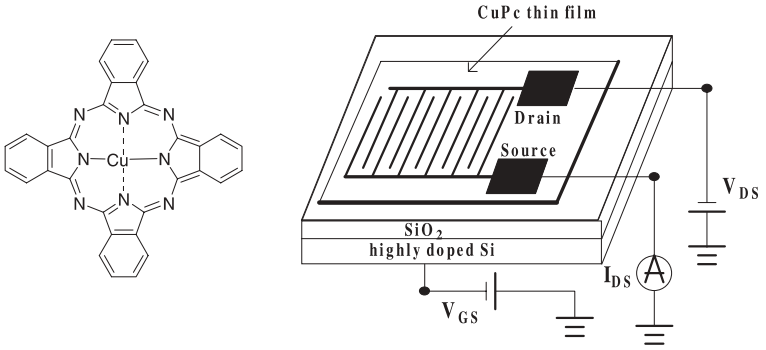

FIGURE 1 Molecular structure of CuPc (**a**) and schematic structure of a CuPc field-effect transistor (**b**)

with a channel length $L = 0.4$ mm and a channel width $W = 66$ mm were fabricated on thermally oxidized Si substrates. The n-doped Si substrate functions as the gate and an oxide layer of 600 nm is the gate dielectric. CuPc thin films were prepared by vacuum deposition at a rate of 2 nm/min under a pressure of 10^{-7} Torr, and the thickness of the resulting films was between 50 and 60 nm. On top of this surface, gold was deposited through a shadow mask to give the source (S) and drain (D) electrodes. OFET characteristics were obtained at room temperature in air using a Hewlett-Packard (HP) 4140B semiconductor parameter analyzer at various gate voltages. Temperature-dependent measurements were done by placing the device on the cold finger of a closed-cycle helium cryostat in a CTO-Cryodyne model M22.

3 Results and discussion

To characterize the preferred orientation of CuPc crystallites within the thin films, XRD experiments were performed. Figure 2a shows the X-ray-diffraction pattern of CuPc films deposited at various substrate temperatures on Si/SiO_2 and the same process conditions as for device fabrication. A single sharp reflection at 2θ of 6.9° ($d = 12.9$ Å) was observed. This distance between the plane of the copper atoms in one layer and that in the next layer is in fair agreement with the reference value (12.6 Å) [21, 22]. The single peak is the result of diffraction from the (200) lattice planes separated by approximately the inter-stacking distances and, therefore, implies that the trace of the herringbone pattern is parallel to the substrate. Figure 2b shows that the configuration on the CuPc planes is oriented edge-on with respect to the substrate. All our thin films prepared at different substrate temperatures usually show this type of preferred orientation. This type of orientation has been found particularly useful in achieving high mobilities since the π–π stacking direction is in the plane of the current-flowing direction. When CuPc was sublimed onto a Si/SiO_2 substrate with increased substrate temperature, the reflection intensity at 6.9° showed a corresponding increase and sharpening with T_{sub}, which suggested better ordering and enhanced crystallinity within the thin film.

The morphology of CuPc films plays a critical role in determining their macroscopic semiconducting performance. Figure 3 shows TEM pictures of CuPc films deposited on carbon-coated electromicroscopic grids at different temperatures. The film deposited at room temperature is made of homogeneous small crystal grains with an average diameter of about 20–30 nm (Fig. 3a). With increase of the deposition temperature, the size of the crystal increases dramatically from 20 nm to 3 μm and the morphology of the films gradually changes from grains to rod-like and large flat crystal. Clearly, a larger, more perfect flat crystal is far more preferable for carrier flow (Fig. 3b). However, nucleation at high substrate temperature is very sparse so that the resulting large and regular crystals end up being separated far from each other and severe film discontinuities and large gaps occur (Fig. 3c and d), which have a negative effect on mobility of OFET devices. These results confirm that the control of substrate temperature allows us to monitor the grain size and shape together with homogeneity of structural organization.

The transistor behavior of CuPc was studied using the device structure shown in Fig. 1b. CuPc performs as a p-channel transistor and operates as an

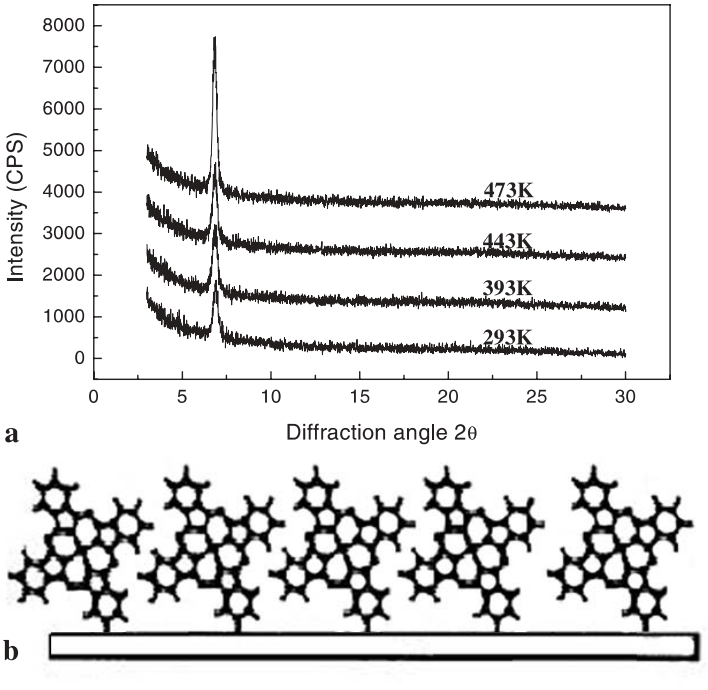

FIGURE 2 The X-ray diffraction of CuPc deposited on Si/SiO_2 at different substrate temperatures (**a**) and schematic descriptions of the preferred orientations observed in CuPc thin films (**b**), molecular planes oriented approximately perpendicular to the substrate surface

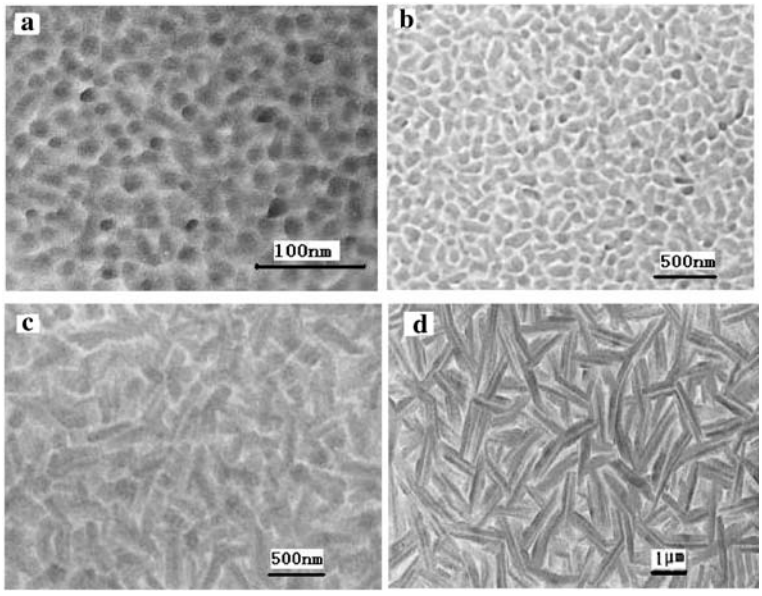

FIGURE 3 Transmission electron micrographs from CuPc films at different substrate temperatures. **a** $T_{sub} = 20\,^{\circ}C$, crystals are granular $\sim$ 20–30 nm in diameter, **b** $T_{sub} = 120\,^{\circ}C$, rod-like crystals with average dimensions $\sim 50 \times 200\,nm^2$, **c** $T_{sub} = 170\,^{\circ}C$, rod-like crystals with average dimensions $\sim 60 \times 460\,nm^2$ (with some small gaps), **d** $T_{sub} = 200\,^{\circ}C$, large flat crystals with dimensions of up to $\sim 400 \times 3000\,nm^2$ (with severe discontinuities and large gaps)

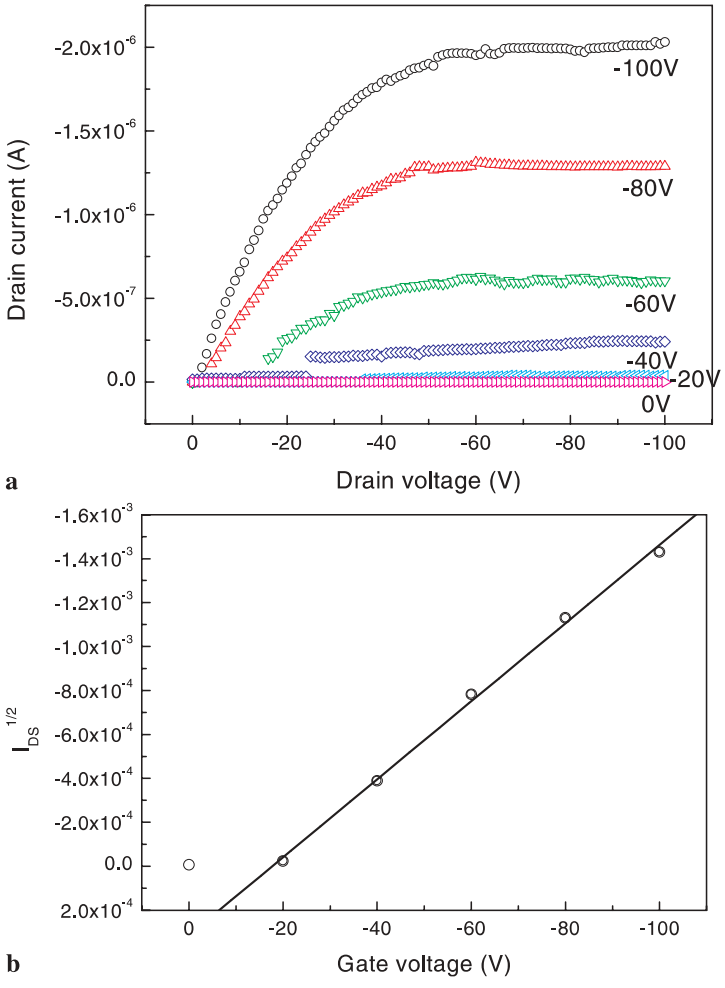

FIGURE 4 The current–voltage characteristics of an OFET for different source–gate voltages (**a**) and plot of the square root of drain current in the saturation regime as a function of the gate voltage for the same transistor (**b**)

accumulation-mode device. Figure 4a shows the typical drain–source current characteristics of a FET with a 50-nm thin film of CuPc as the semiconducting layer deposited at room temperature at different gate voltages. The mobility was measured in the saturation regime ($V_{DS} > V_{GS}$), which is modeled by the equation [23]:

$$I_{DS} = \frac{WC_i}{2L}\mu(V_G - V_0)^2\,, \qquad (1)$$

where μ is the field-effect mobility, L and W are channel length and width, respectively, C_i is the insulator capacitance per unit area, and V_0 is the extrapolated threshold voltage. Due to the low Ohmic current at zero gate voltage, a plot of $I_{DS}^{1/2}$ versus V_G can be used to obtain V_0, the extrapolated threshold voltage (Fig. 4b). The field-effect mobility calculated using this method is $1.01 \times 10^{-3}\,cm^2/V\,s$; the on/off ratio of the transistor is 2.3×10^4, which is better than recent reports in the literature [11, 24]. The field-effect mobilities obtained on films of CuPc at different substrate temperatures are listed in Table 1. Device mobility reaches its highest value when T_{sub} is 120 °C. We note that the mobility is strongly dependent on the deposition temperature. From the above XRD and TEM analysis, the control of substrate temperature allows us to monitor the orientation and morphology of thin films, affecting the field-effect mobility of FET devices. Therefore, the morphology of the films can greatly affect charge-carrier mobilities due to the grain-boundary effect [25, 26].

The channel conductivity is examined in the cold finger of a closed-cycle helium cryostat as a function of gate bias. A typical result is shown in Fig. 5. The gate bias can modulate the conductance of a CuPc film surface. The resulting charge-transport data of

Substrate temperature (°C)	Mobility ($cm^2/V\,s$)
20	1.01×10^{-3}
120	3.75×10^{-3}
170	2.9×10^{-3}
200	4.9×10^{-5}

TABLE 1 Field-effect mobilities of CuPc at different substrate deposition temperatures

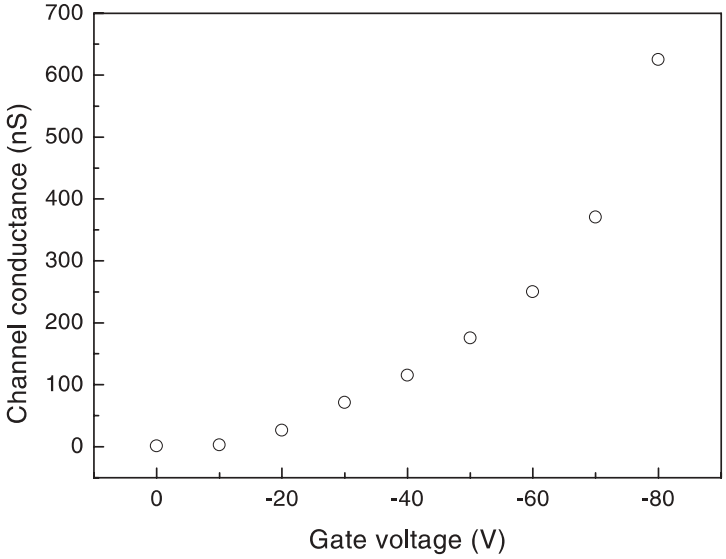

FIGURE 5 The channel conductance as a function of gate bias

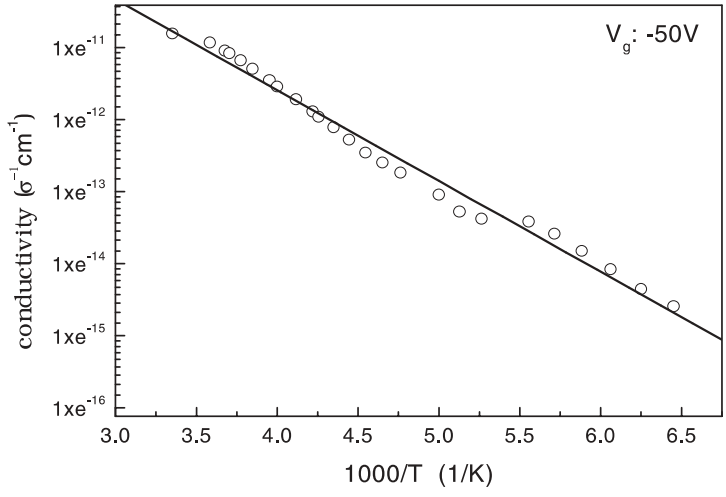

FIGURE 6 Channel conductance of a CuPc TFT as a function of the different temperatures for a gate voltage $V_G = -50$ V. Its slope is used for determining the thermal activation energy ($E_a = 0.109$ eV). It shows thermally activated behavior

the CuPc FET at different temperatures for a gate voltage $V_G = -50$ V are shown in Fig. 6. The channel conductivity is clearly thermally activated with a thermal activation energy in the order of 0.109 eV. This behavior is attributed to defects, disorder, and domain boundaries in the polycrystalline film, since the transport has been described by a variable-range hopping process between localized trap states [27, 28].

4 Conclusion

We observed high order and strong orientation of CuPc molecules on Si/SiO_2 by using XRD and TEM analysis at different substrate temperatures during the deposition process, which affect directly the morphology of thin films. The results show the effect of CuPc morphology at different substrate temperatures on the transistor performance. When the substrate temperature for deposition of CuPc is 120 °C, a mobility of 3.75×10^{-3} cm^2/V s can be obtained.

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