Electrical Engineering
https://doi.org/10.1007/s00202-024-02595-2

ORIGINAL PAPER

Study of SVPWM control algorithm with voltage balancing based on simplified vector for cascaded H-bridge energy storage converters

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Received: 6 February 2024 / Accepted: 3 July 2024

Abstract
DC-side voltage balancing is a critical problem to be solved for cascaded H-bridge energy storage converters. Aiming at inner-phase voltage balancing problem, a space vector pulse width modulation (SVPWM) algorithm with voltage balancing based on simplified vector is proposed. Firstly, the number of voltage vector is simplified by the proposed algorithm. Secondly, the action time of each level is calculated based on the volt-second balance, and the output vector is determined by comparing the DC-side voltage magnitude. Furthermore, the change of module level is minimal at the time of level change, and leapfrog hopping of the module level is prevented. Then, the inner-phase voltage balance can be achieved using vector selection. Due to the simplified SVPWM with voltage balancing, the algorithm is simpler, the switching losses is smaller, and it is easy to extend to cascaded H-bridge converters with more modules. Regarding the mutual-phase voltage balancing problem, the additional power generated by the zero-sequence voltage injection changes the power distribution among the three phases, so that the mutual-phase voltages is balanced. Finally, the effectiveness of the proposed control algorithm is verified by simulation and experimental results.

Keywords Cascaded H-bridge energy storage converters · SVPWM · Voltage balance · Simplified vector · Low switching losses

1 Introduction

In recent years, the energy storage technology has gradually become an indispensable component in the stable operation of smart grid with the development of renewable energy [1, 2]. Currently, with the development of energy storage technology in the direction of high voltage and high power, it is of great significance to study high-capacity multilevel energy storage power converters. There are more advantages of CHB topology compared to CHB and other multilevel topologies [3, 4]. The CHB topology is more suitable to be used as a high-power energy storage converters structure due to its modularity, expandability, ease of meeting higher voltage and capacity design requirements, and grid-connectivity without the need for an additional transformer.

The CHB energy storage converters consist of multiple identical modules in cascade, each module consists of an energy storage unit and a full-bridge structure, and the energy storage unit is generally a lithium iron phosphate battery, a lead-acid battery, a supercapacitor, etc. In this paper, supercapacitor is used as an energy storage unit, due to the faster response, higher power density and longer service life compared to battery energy storage [5, 6]. However, considering the differences in capacity and internal resistance as well as losses in the production process of supercapacitors [7]. This can cause an imbalance in the DC-side voltage between modules, as well as over-charging and over-discharging phenomena, which can seriously endanger the service life of supercapacitors. Therefore, the balancing of DC-side voltage is especially critical for the energy storage system, which is a prerequisite for the safe and stable operation of the system.

Inner-phase balancing and mutual-phase balancing controls are commonly employed for DC-side voltage balancing problems in three-phase CHB energy storage systems. For the inner-phase balancing, there are mainly two kinds of hardware balancing and software balancing. In [8], a hardware balancing control by adding a DC–DC link on the DC-side is proposed, which has good control effect, but it is complicated to control and costly. Software balancing is more common

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Published online: 11 July 2024

than additional hardware balancing control, and software balancing can be subdivided into two categories: indirect control and direct control of voltage balancing. In [9, 10], each module is added an independent voltage balancing PI link in its control section, which is simple and easily scalable. In [11], it is proposed to inject a compensating component to change the modulating waveform to redistribute the module power and reach the voltage balance on the DC-side of the module, which is easy to implement and low cost. The above literatures are all based on carrier phase shifting-sinusoidal pulse width modulation (CPS-SPWM) indirectly controlled voltage balancing approach, which essentially adjusts the modulating waveforms of each module through independent voltage balancing control algorithms and thus changes the duty cycle to achieve the purpose of inner-phase balancing. But, the voltage balancing capability of this type of approach is weak and increases the burden on the system controller due to independent voltage balancing algorithm. Meanwhile, the control parameters of the algorithm are numerous and difficult to select.

For this reason, in [12–14], voltage balancing using SVPWM method with direct voltage control is proposed. This method can achieve voltage balancing by using the selection of redundant vectors, which has the advantages of strong voltage balancing capability, high-voltage utilization and simple control. In [15–17], SVPWM algorithms in different coordinate systems and the principle of redundant vector generation are studied. In [18] and [19], 1D-SVPWM on a one-dimensional straight line and 2D-SVPWM in a two-dimensional plane were proposed, respectively, which attracted more scholars to study SVPWM with voltage balancing algorithms. In [20–22], 3D-SVPWM with voltage balancing algorithm for three-module cascaded converters is proposed, which puts all the voltage vectors into a three-dimensional space for analysis. The above SVPWM algorithms are all able to achieve voltage balancing by selecting vectors, but they do not consider the case of module port level leapfrog hopping and simultaneous action, which will increase the switching losses. Also, with the increase of the number of cascades, the number of vectors will increase dramatically and the algorithm will be more complicated.

The main methods are negative-sequence current injection and zero-sequence voltage injection for mutual-phase balancing problem. In [23], mutual-phase balancing based on negative-sequence current injection is proposed but affects the input-side power quality due to the injection of negative-sequence currents, which is detrimental to the safe operation of the grid. In [24], a combination of hybrid modulation strategy and zero-sequence injection method is proposed for mutual-phase power balancing control, which has lower total harmonic distortion (THD) of the grid-side currents after balancing, but the control is more complicated.

Therefore, an easily scalable SVPWM algorithm with voltage balancing based on simplified vector is proposed in this paper using a three-phase CHB energy storage converters as the study topology. And the problems of high switching losses in the above literature and the sharp increase in the number of voltage vectors with the increase in the number of cascades are overcome by this algorithm. At first, the algorithm simplifies the voltage vectors with the goal of strong voltage balancing capability and low switching losses and selects the output vectors according to the magnitude of the DC-side voltage. Moreover, the change of module level is minimal when the level changes, and leapfrog hopping of the module level is prevented. Then, the inner-phase voltage balancing can be achieved using the selection of vectors. After that, the zero-sequence voltage injection method is used to achieve mutual-phase balancing control for more complex problems of mutual-phase voltage control. Finally, the correctness of the proposed method is verified by simulation and experimental results.

2 Modeling and power control

2.1 Mathematical modeling of energy storage converters

The topology of the CHB energy storage converters is shown in Fig. 1. The three phases of this converter are connected in star-arrangement with each phase consisting of n modules in cascade, and it is connected to the AC grid through filter reactors. In Fig. 1, u_{sa}, u_{sb}, and u_{sc} are the three-phase grid voltages, u_a, $u_{b,}$ and u_c are the three-phase output voltage of the converter, i_a, i_b and i_c are the three-phase current of the converter, L is the grid-side filter reactor, R is the equivalent losses, $U_{\mathrm{dc}a1}$, $U_{\mathrm{dc}a2}$, and $U_{\mathrm{dc}an}$ are the voltages of the supercapacitor of the energy storage unit, and C is the DC-side filter capacitance of the H-bridge of equal size. For example for phase A, U_{a1b1}, U_{a2b2}, and U_{anbn} are the output voltages of module 1, module 2, and module n, respectively, and the output phase voltage of the AC-side of phase A can be obtained as $u_a = U_{a1b1} + U_{a2b2} + U_{anbn}$. When the DC-side voltage of the CHB converter is balanced, i.e., $U_{dca1} = U_{dca2} = U_{dcan} = U_{dc}$, different switch combinations can be used, and the phase voltage u_a will have $2n+1$ levels from $-n \cdot U_{dc}$ to $n \cdot U_{\mathrm{dc}}$.

The upper and lower switching devices operate in complementary states, for a single H-bridge module. Take the i-th module of phase A as an example, define the switching function S_{ai} as:

$$S_{ai} = \begin{cases} 1 & (S_{\mathrm{ai1}},\ S_{\mathrm{ai4}}\ \mathrm{ON}) \\ 0 & ((S_{\mathrm{ai1}},\ S_{\mathrm{ai3}})\ \mathrm{or}\ (S_{\mathrm{ai2}},\ S_{\mathrm{ai4}})\ \mathrm{ON}) \\ -1 & (S_{\mathrm{ai2}},\ S_{\mathrm{ai3}}\ \mathrm{ON}) \end{cases} \tag{1}$$

where $i = 1 \sim n$.

Then, the mathematical model of the CHB energy storage converters in the abc three-phase stationary coordinate system is obtained as:

$$\begin{cases} L\dfrac{di_a}{dt} = u_{sa} - i_a R - \displaystyle\sum_{i=1}^{n} S_{\mathrm{ai}} U_{\mathrm{dc}} \\ L\dfrac{di_b}{dt} = u_{sb} - i_b R - \displaystyle\sum_{i=1}^{n} S_{bi} U_{\mathrm{dc}} \\ L\dfrac{di_c}{dt} = u_{sc} - i_c R - \displaystyle\sum_{i=1}^{n} S_{ci} U_{\mathrm{dc}} \end{cases} \tag{2}$$

where U_{dc} is the supercapacitor output voltage when each module is balanced.

2.2 System power control

The various physical quantities to be determined for the time-varying alternating current due to the abc three-phase stationary coordinate system, which is more complex to analysis. Thus, the mathematical model under the abc coordinate system is converted by coordinate transformation to under the dq-axis synchronous rotating coordinate system, as in

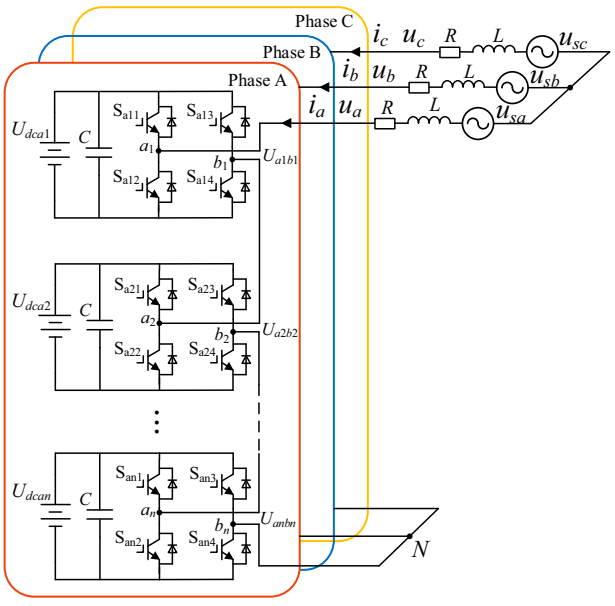

Fig. 1 Topology of a cascaded H-bridge energy storage converters

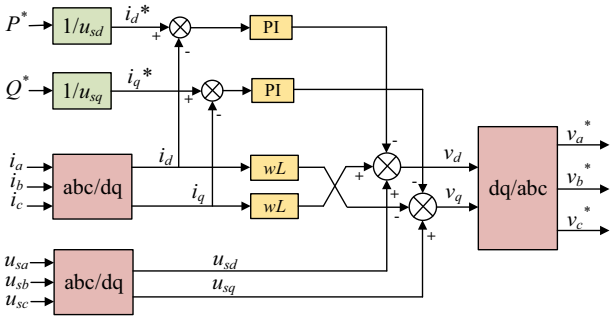

Fig. 2 Power control block diagram of the energy storage converter system

Eq. (3):

$$\begin{cases} L\dfrac{di_d}{dt} = u_{sd} - Ri_d - U_{\mathrm{dc}} S_d + \omega L i_q \\ L\dfrac{di_q}{dt} = u_{sq} - Ri_q - U_{\mathrm{dc}} S_q - \omega L i_d \end{cases} \tag{3}$$

where u_{sd}, u_{sq} and i_d, i_q and S_d, S_q denote the state quantities of the three-phase grid voltage and grid current and switching function of the AC-side in the dq coordinate system, respectively.

Neglecting the three-phase circuit equivalent losses and decoupling i_d and i_q to achieve independent control of active and reactive power, the system power control block diagram of the CHB converters can be obtained, as shown in Fig. 2. P^* and Q^* are given for active and reactive power, and then, the reference voltage signals v_d and v_q in dq coordinate system are obtained through the current inner loop decoupling control; then, the output voltage modulated waveforms $v_a{}^*$, $v_b{}^*$ and $v_c{}^*$ in abc coordinate system are obtained through the inverse Park's transformation. Finally, the SVPWM algorithm with voltage balancing based on simplified vector can be used to obtain PWM signals, which can be distributed to each module to complete the overall control of the system.

3 SVPWM algorithm with voltage balancing based on simplified vector

3.1 Principle of SVPWM algorithm with voltage balancing

For a multilevel converter, each of its phase outputs can output a multilevel phase voltage with different phases and the same level. The phase voltage u_a as the reference phase can be compared to a reference vector $\vec{V}$, whose Y-axis is always zero, and its trajectory is plotted in a planar diagram. The principle of the three-module seven-level CHB, for example, is shown in Fig. 3, assuming that the voltage on the DC-side of the converter is balanced. In Fig. 3, the seven-level [−

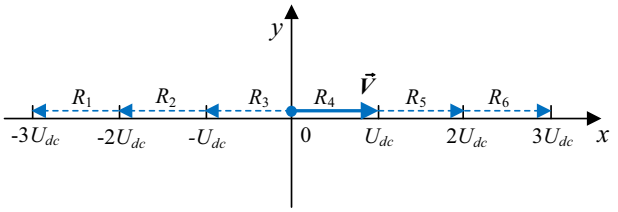

Fig. 3 Schematic diagram of SVPWM algorithm with voltage balancing for A-phase seven-level

$3U_{\mathrm{dc}}, -2U_{\mathrm{dc}}]$, $[-2U_{\mathrm{dc}}, -U_{\mathrm{dc}}]$, $[-U_{\mathrm{dc}}, 0]$, $[0, U_{\mathrm{dc}}]$, $[U_{\mathrm{dc}}, 2U_{\mathrm{dc}}]$, and $[2U_{\mathrm{dc}}, 3U_{\mathrm{dc}}]$ intervals are denoted as the R_1, R_2, R_3, R_4, R_5, and R_6 regions, respectively. When $\vec{V}$ is moving in the positive half-axis of the X-axis, the corresponding phase voltage is positive, and its modulus represents the proportion of time that it acts in a given region (how long the vector operates in a given region is equal to the amount of time the phase voltage acts in that level interval). The motion of $\vec{V}$ running from 0 increasing to $3U_{\mathrm{dc}}$ and then decreasing to 0 is equivalent to the period when the phase voltage is positive. The principle is the same when the vector moves in the negative half-axis of the X-axis as when the vector is in the positive half-axis of the X-axis.

Specifically, it is sufficient to determine that the reference vector $\vec{V}$ is running in a certain region, and output the level of that region. Assuming that the vector $\vec{V}$ is running in the R_4 region, this causes the system to issue commands for levels 0 and U_{dc}. The principles for phases B and C are the same as for phase A.

3.2 Calculation of leveling time

Taking the A-phase three-module cascade as an example, let the output phase voltages be $-3U_{\mathrm{dc}}$, $-2U_{\mathrm{dc}}$, $-U_{\mathrm{dc}}$, 0, U_{dc}, $2U_{\mathrm{dc}}$, and $3U_{\mathrm{dc}}$ with the action times $T_{a-3}, T_{a-2}, T_{a-1}, T_{a0}, T_{a1}, T_{a2}$, and T_{a3}, and the switching period is T_s. When the reference vector $\vec{V}$ is in the interval of $[0, U_{\mathrm{dc}}]$, it can be obtained according to the volt-second balance:

$$\begin{cases} T_{a0} \times 0 + T_{a1} U_{\mathrm{dc}} = \mathrm{V}T_s \\ T_{a0} + T_{a1} = T_s \end{cases} \tag{4}$$

Then, T_{a0} and T_{a1} can be solved as shown in Eq. (5):

$$\begin{cases} T_{a0} = \dfrac{T_s}{U_{\mathrm{dc}}}(U_{\mathrm{dc}} - V) \\ T_{a1} = \dfrac{T_s}{U_{\mathrm{dc}}} V \end{cases} \tag{5}$$

Similarly, the action time of $\vec{V}$ when it is in the region of R_1, R_2, R_3, R_4, R_5, and R_6 is shown in Table 1.

The time allocation can be done after calculating the action time for each level interval, and a three-stage allocation is used in this paper. The R_1 to R_6 area allocation is the same, take R_5 as an example, as shown in Fig. 4. The carrier wave is a triangular wave, T_s is the carrier period, so the carrier amplitude is also T_s because of $T_{a1} + T_{a2} = T_s$. The smaller number of levels T_{a1} is used as the modulating wave to compare with the carrier wave. The control signal T_{PWM} is 0 and outputs the U_{dc} level when the modulating wave is greater than or equal to the carrier wave. The control signal T_{PWM} is 1 and outputs the $2U_{\mathrm{dc}}$ level, when the modulating wave is smaller than the carrier wave.

Table 1 Acting time of each level interval in phase A

Region	Action times	
R_1	$T_{a-3} = \frac{-T_s}{U_{\mathrm{dc}}}(2U_{\mathrm{dc}} + V)$	$T_{a-2} = \frac{T_s}{U_{\mathrm{dc}}}(3U_{\mathrm{dc}} + V)$
R_2	$T_{a-2} = \frac{-T_s}{U_{\mathrm{dc}}}(U_{\mathrm{dc}} + V)$	$T_{a-1} = \frac{T_s}{U_{\mathrm{dc}}}(2U_{\mathrm{dc}} + V)$
R_3	$T_{a-1} = \frac{-T_s}{U_{\mathrm{dc}}} V$	$T_{a0} = \frac{T_s}{U_{\mathrm{dc}}}(U_{\mathrm{dc}} + V)$
R_4	$T_{a0} = \frac{T_s}{U_{\mathrm{dc}}}(U_{\mathrm{dc}} - V)$	$T_{a1} = \frac{T_s}{U_{\mathrm{dc}}} V$
R_5	$T_{a1} = \frac{T_s}{U_{\mathrm{dc}}}(2U_{\mathrm{dc}} - V)$	$T_{a2} = \frac{T_s}{U_{\mathrm{dc}}}(V - U_{\mathrm{dc}})$
R_6	$T_{a2} = \frac{T_s}{U_{\mathrm{dc}}}(3U_{\mathrm{dc}} - V)$	$T_{a3} = \frac{T_s}{U_{\mathrm{dc}}}(V - 2U_{\mathrm{dc}})$

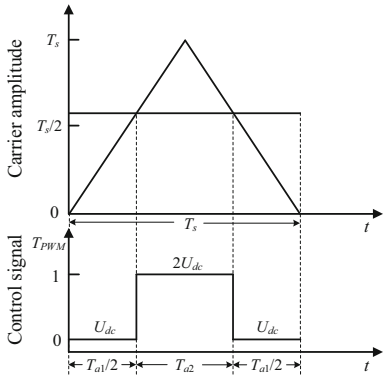

Fig. 4 Three-segment vector distribution diagram for the R_5 region

3.3 Principles of optimization for simplified vector algorithms

Knowing that each module can output a total of three states of 1, 0, and -1, which correspond to three levels of U_{dc}, 0, and $-U_{\mathrm{dc}}$, respectively, the A-phase three-module cascade converters can output 27 voltage vectors. Taking the output level number U_{a1b1}/U_{dc} of the first module of phase A as L_{a1} axis, the output level number U_{a2b2}/U_{dc} of the second module as L_{a2} axis, the output level number U_{a3b3}/U_{dc} of the third module as L_{a3} axis, the total phase voltage output level number is L_a, then:

$$L_a = L_{a1} + L_{a2} + L_{a3} \tag{6}$$

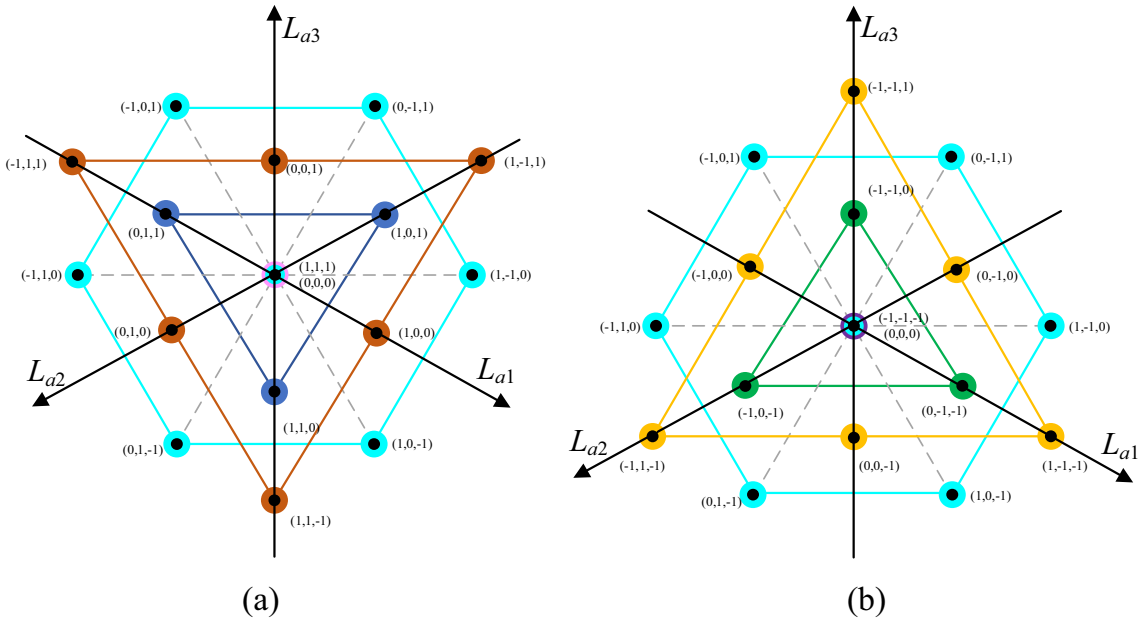

Fig. 5 A-phase seven-level converter space voltage vector diagram. **a** $u_a \geq 0$, **b** $u_a \leq 0$

where L_a, L_{a1}, L_{a2}, and L_{a3} are integers and $L_a \in [-3, 3]$.

All the voltage vectors are located in the three-dimensional space ofL_{a1}, L_{a2}, and L_{a3} axes and form a cube, and the vector points with equal values of L_a can form a tangent plane, and the coordinate origin (0, 0, 0) is located in the center of gravity of the cube. Therefore, the A-phase seven-level converter space voltage vector diagram can be established, as shown in Fig. 5. It can be seen that the equal values of L_a are redundant vectors, which have the same output level but different voltage balancing effects; there are 27 voltage vectors distributed in a total of seven cuts of $L_a = -3, -2, -1, 0, 1, 2, 3$, and the region between every two cuts corresponds to the level intervals and regions defined in Fig. 3. Where the voltage vector is not only at the boundaries of the cuts but also at the inner center of the cuts when$L_a = 0$, that is, the center of gravity of the cube.

From Fig. 5, it can be seen that the number of voltage vectors is large, and with the increase of the number of cascades, the voltage vectors will increase more, which makes it very difficult to choose the optimal vector for voltage balancing. To solve this problem, this paper simplifies the voltage vectors with the goal of strong voltage balancing capability and low switching losses, so that the computational difficulty and switching losses are greatly reduced, and it is easier to extend to more number of cascaded converters.

3.3.1 Strong voltage balancing capability

The voltage of the supercapacitor energy storage converters can be balanced by varying the charging and discharging speeds when the optimal voltage balancing effect is the goal. Modules with large voltages are charged less and discharged more, modules with small voltages are charged more and discharged less, and modules with faster charging and discharging speeds in a certain time have more power input or output. Therefore, the charging and discharging speed of the module can be controlled indirectly by controlling the power on the DC-side, which in turn changes the DC-side voltage of each module.

Assuming ideal conditions, the power on the AC-side of the i-th module of phase A of the converter is equal to the power on the DC-side of the module:

$$\begin{cases} P_{\mathrm{ai}} = U_{\mathrm{aibi}} i_a \cos\varphi \\ P_{\mathrm{dcai}} = U_{\mathrm{dcai}} i_a S_{ai} \\ P_{\mathrm{ai}} = P_{\mathrm{dcai}} \end{cases} \tag{7}$$

where P_{ai} is the AC-side power of the i-th module of phase A, P_{dcai} is the DC-side power of the i-th module of phase A, φ is the power factor angle, and $i = 1 \sim 3$.

From Eq. (7), it can be seen that the module DC-side and AC-side currents are equal, and the AC-side voltage U_{aibi} can be changed to balance the DC-side voltage U_{dcai} of the module. Assuming that the R_4 region is initially (0, 0, 0) at a certain point in time, since the output in the R_4 region alternates between the 0 level and the U_{dc} level, if the U_{dca1} voltage is to be increased at the next point in time, one of the three vectors (1, − 1, 1), (1, 0, 0), and (1, 1, − 1) on the AC-side can be selected for voltage balancing by selecting the U_{dc} level. Therefore, among the many vectors of the seven levels, the vector with high-voltage balancing capability represents the most input or output power and the largest input or output

voltage on the AC side. It can be made that m is the voltage balancing capability as in Eq. (8):

$$m = \left| \frac{U_{a1b1} + U_{a2b2} + U_{a3b3}}{U_{\mathrm{dc}}} \right| > 0 \tag{8}$$

As $L_{a1} = U_{a1b1}/U_{\mathrm{dc}}, L_{a2} = U_{a2b2}/U_{\mathrm{dc}}, L_{a3} = U_{a3b3}/U_{\mathrm{dc}}$, therefore:

$$m = |L_{a1} + L_{a2} + L_{a3}| > 0 \tag{9}$$

where m is a nonzero integer.

The larger m represents the strong voltage balancing capability, while the redundant vector at level 0 can be eliminated in a seven-level energy storage converter, but the internal voltage vector at level 0 should be retained in order for the converter to operate properly.

3.3.2 Low switching losses

Reduced switching times should be considered to prevent module level leapfrog hopping when aiming for low switching losses. For example, when in the R_4 region, a jump from level 0 (− 1, 0, 1) to level 1 (1, − 1, − 1) may occur; although the voltage balancing capability may be good, module 1 has undergone leapfrog hopping from a $-U_{\mathrm{dc}}$ level change to a U_{dc} level, and module 3 has undergone leapfrog hopping from a U_{dc} level change to a $-U_{\mathrm{dc}}$ level; And the three-module switching tubes will act at the same time, and the bridge arms need to be subjected to large voltage stress. Secondly, when the level of phase voltage changes, one of the three modules should be made to change the level of one of the modules, and the other two remain unchanged, to meet this requirement, can greatly reduce the switching losses. If the change from level 0 to U_{dc} level is initially (0, 0, 0), the next moment may be one of (0, 0, 1), (1, 0, 0), (0,1, 0) rather than one of (1, − 1, 1), (1, 1, − 1), (− 1, 1, 1).

Therefore, in combination with the goal of strong voltage balancing capability and low switching losses, (0, − 1, 1), (1, − 1, 0), (1, 0, − 1), (0, 1, − 1), (− 1, 1, 0), (− 1, 0, 1) should be removed at level 0 and (0, 0, 0) should be retained; at U_{dc} levels (− 1, 1, 1), (1, − 1, 1), (1, 1, − 1) should be removed; at $-U_{\mathrm{dc}}$ levels (− 1, − 1, 1), (1, − 1, − 1), (− 1, 1, − 1) should be removed; $\pm 2U_{\mathrm{dc}}$ levels and $\pm 3U_{\mathrm{dc}}$ levels are all retained. The 27 vectors in phase A can then be simplified to 15 vectors with strong voltage balancing capability, reducing the number of vectors by 44.4%, as shown in Fig. 6.

From Fig. 6(a), it can be seen that when L_a changes from 0 to 1 and 2 to 3, both are only one of the three modules level changes, and the change is 1, and there is no leapfrog hopping. Similarly, when L_a changes from − 1 to 0 and -3 to − 2, no leapfrog hopping occurs. And when L_a changes from 1 to 2 and − 2 to − 1, as shown in Table 2, there are 2/3 occurrences of only one module level change out of three modules, and the change is 1 and there is no leapfrog hopping, as shown in the second and third columns of Table 2; and there are 1/3 occurrences of three-module level changes, but with smaller chances of occurring and the change is 1 and there is no leapfrog hopping, as shown in the fourth column of Table 2.

The optimization principle of the simplified vector algorithm by analysis is:

1) It is necessary to keep the internal or boundary voltage vectors of the cut-outs for the system to function properly and to output the full level;
2) Screen the vectors with strong voltage balancing ability by substituting the boundary vectors in the remaining cuts into Eq. (9);
3) Prevent the module level leapfrog hopping, and when the level changes, one of the three modules should be made to change level and the other two should remain unchanged to reduce switching losses.

4 Inner-phase and mutual-phase DC-side voltage balancing control

4.1 Inner-phase DC-side voltage balancing control

According to Sect. 3.3, a total of 27 voltage vectors in phase A are simplified into 15 vectors with strong voltage balancing capability, and the DC-side voltage U_{dcai} of the balancing module is carried out by changing the AC-side voltage U_{aibi}. However, there are three voltage vectors at the output AC-side voltage of $\pm U_{\mathrm{dc}}$ level and $\pm 2U_{\mathrm{dc}}$ level, and the redundant voltage vectors at the same level can be considered to have different effects on the DC-side voltage. Then, the vector with stronger voltage balancing ability is selected to be different according to the DC-side voltage magnitude and input current direction. The voltage vectors at different output levels affect the DC-side voltage as shown in Table 3, where "↓" indicates a voltage decrease, "↑" indicates a voltage increase, and " + " indicates that the A-phase input current i_a is positive, and "−" indicates that the phase A input current i_a is negative.

From Table 3, it can be obtained that there is only one vector at $L_a = 0$ and $L_a = \pm 3$ after simplifying the vectors, and there is no need to make a selection, which reduces the burden on the system. At $L_a = \pm 1$ and $L_a = \pm 2$, the selection of the optimal vector is made according to the voltage magnitude and current direction. Take the R_5 region as an example, the flowchart is shown in Fig. 7, when the A-phase output level L_a is located in the R_5 region.

Firstly, the output U_{dc} level and $2U_{\mathrm{dc}}$ level are determined by determining that it is located in the R_5 region based on the

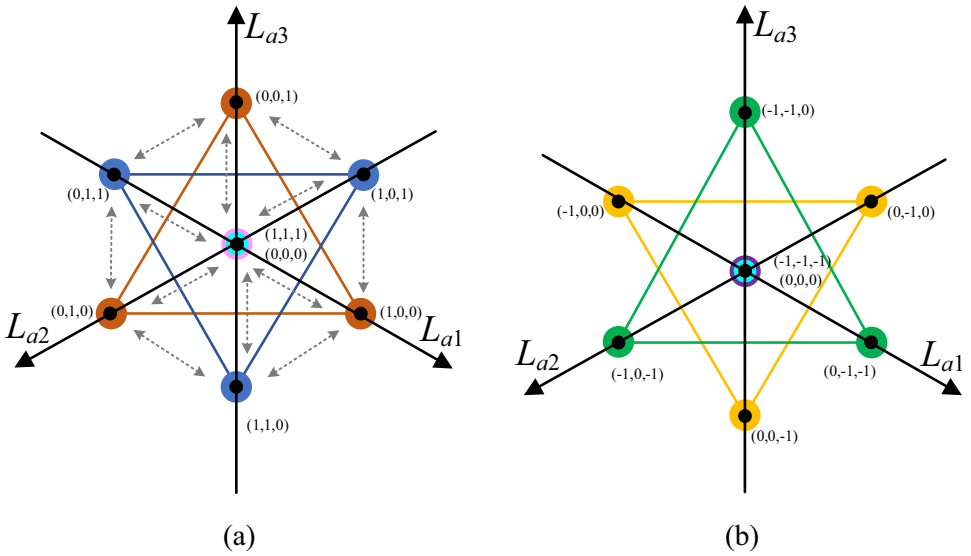

Fig. 6 Simplified vectorial A-phase seven-level space voltage vector diagrams. **a** $u_a \geq 0$, **b** $u_a \leq 0$

Table 2 Voltage vector variation in the region of R_2 and R_5

Region	Voltage vector change		
R_2	(− 1,− 1,0) (0,− 1,0)	(− 1,− 1,0) (0,− 1,0)	(− 1,− 1,0) (0,0,− 1)
	(0,− 1,− 1) (0,− 1,0)	(0,− 1,− 1) (0,0,− 1)	(0,− 1,− 1) (− 1,0,0)
	(− 1,0,− 1) (0,0,− 1)	(− 1,0,− 1) (− 1,0,0)	(− 1,0,− 1) (0,− 1,0)
R_5	(0, 0, 1) (0, 1, 1)	(0, 0, 1) (1, 0, 1)	(0, 0, 1) (1, 1, 0)
	(1, 0, 0) (1, 1, 0)	(1, 0, 0) (1, 0, 1)	(1, 0, 0) (0, 1, 1)
	(0, 1, 0) (1, 1, 0)	(0, 1, 0) (0, 1, 1)	(0, 1, 0) (1, 0, 1)

Table 3 Effect of different voltage vectors in phase A on DC-side voltage

L_a	L_{a1}	L_{a2}	L_{a3}	U_{dca1}	U_{dca2}	U_{dca3}
− 3	− 1	− 1	− 1	↓(+),↑(−)	↓(+),↑(−)	↓(+),↑(−)
− 2	0	− 1	− 1	Constant	↓(+),↑(−)	↓(+),↑(−)
	− 1	0	− 1	↓(+),↑(−)	Constant	↓(+),↑(−)
	− 1	− 1	0	↓(+),↑(−)	↓(+),↑(−)	Constant
− 1	− 1	0	0	↓(+),↑(−)	Constant	Constant
	0	− 1	0	Constant	↓(+),↑(−)	Constant
	0	0	− 1	Constant	Constant	↓(+),↑(−)
0	0	0	0	Constant	Constant	Constant
1	1	0	0	↑(+),↓(−)	Constant	Constant
	0	1	0	Constant	↑(+),↓(−)	Constant
	0	0	1	Constant	Constant	↑(+),↓(−)
2	0	1	1	Constant	↑(+),↓(−)	↑(+),↓(−)
	1	0	1	↑(+),↓(−)	Constant	↑(+),↓(−)
	1	1	0	↑(+),↓(−)	↑(+),↓(−)	Constant
3	1	1	1	↑(+),↓(−)	↑(+),↓(−)	↑(+),↓(−)

reference vector; then, T_{a1} and T_{a2} are calculated and time allocation is performed, and the operating level is determined to be either the U_{dc} level or the $2U_{\mathrm{dc}}$ level based on the T_{PWM} generated by the time allocation, which can be assumed to be the following moments:

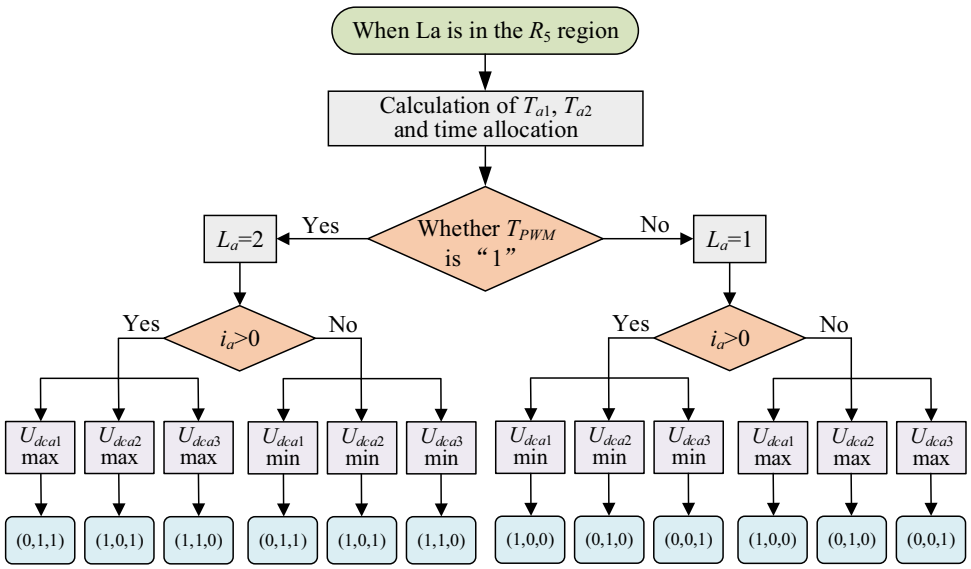

Fig. 7 A-phase three-module inner-phase DC-side voltage balancing control flowchart. (R_5 area)

1) The voltage vector is (1, 0, 0) when $L_a = 1$ i.e., output U_{dc} level at moment t;
2) If $i_a < 0$ and U_{dca2} is minimal at moment $t + 1$, the output (1, 0, 1) at $L_a = 2$ will decrease U_{dca1} and U_{dca3} according to Table 3;
3) If $i_a < 0$ and U_{dca1} is maximal at moment $t + 2$, the output (1, 0, 0) at $L_a = 1$ will decrease U_{dca1} according to Table 3;
4) If $i_a > 0$ and U_{dca3} is maximum at moment $t + 3$, the output (1, 1, 0) at $L_a = 2$ will increase U_{dca1} and U_{dca2} according to Table 3.

It can be seen that the above moments are all three modules in which only one module level changes, and the change is 1, there is no leapfrog hopping, reducing the switching losses. And through the relationship between the current direction and the DC-side voltage magnitude, and then, select the voltage vector with strong voltage balancing ability, it can achieve fast voltage balancing. Secondly, the SVPWM algorithm with voltage balancing based on simplified vector reduces numerous redundant vectors and can be implemented with only a simple ordering and a few logic judgements. Hence, the burden on the system is small, the operation speed is fast, and it can be extended to H-bridge converters with much number of modules.

4.2 Mutual-phase DC-side voltage balancing control

The three-phase input voltage and current can be decomposed into positive-sequence, negative-sequence, and zero-sequence components according to the method of symmetrical components. The additional zero-sequence voltage does not affect the total output power of the system due to the star-arrangement of the system, and the zero sequence current is zero. Then, the additional power generated by injecting zero-sequence voltage can be used to change the power distribution between the three mutual phases, thus achieving mutual-phase voltage balancing.

In Fig. 1, the three-phase current of the energy storage converters can be made to be expressed as:

$$\begin{cases} i_a = \sqrt{2} I \cos(\omega t + \delta_i) \\ i_b = \sqrt{2} I \cos(\omega t - \dfrac{2\pi}{3} + \delta_i) \\ i_c = \sqrt{2} I \cos(\omega t + \dfrac{2\pi}{3} + \delta_i) \end{cases} \tag{10}$$

where I is the three-phase current RMS value, δ_i is the initial phase of the current.

Then, the additional fluctuating power in the three phases generated by the zero-sequence voltage is:

$$\begin{cases} P_{a0} = U_0 I \cos(\theta_0 - \delta_i) \\ P_{b0} = U_0 I \cos(\theta_0 - \delta_i - \dfrac{2\pi}{3}) \\ P_{c0} = U_0 I \cos(\theta_0 - \delta_i + \dfrac{2\pi}{3}) \end{cases} \tag{11}$$

where P_{a0}, P_{b0}, *and* P_{c0} are the three-phase additional fluctuation power generated by the zero-sequence voltage, U_0 is the rms value of the zero-sequence voltage, and θ_0 is the phase angle of the zero-sequence voltage.

Making the sum of the DC-side voltages of each module of the three-phase cascade of a, b, and c of the CHB energy storage converters as shown in Fig. 1 to be U_{dca}, U_{dcb}, and U_{dcc}, respectively, the average values of the DC-side voltages of each module of each phase, U_{ava}, $U_{avb,}$ and U_{avc}, are:

$$\begin{cases} U_{ava} = U_{\mathrm{dca}}/n \\ U_{avb} = U_{\mathrm{dcb}}/n \\ U_{avc} = U_{\mathrm{dcc}}/n \end{cases} \tag{12}$$

The average value of the DC-side voltage U_{dcav} of each module of the three phases is:

$$U_{\mathrm{dcav}} = \frac{1}{3}(U_{ava} + U_{avb} + U_{avc}) \tag{13}$$

The deviation values of U_{ava}, U_{avb}, U_{avc}, and U_{dcav} are defined as ΔU_{dca}, ΔU_{dcb}, and ΔU_{dcc}:

$$\begin{cases} \Delta U_{\mathrm{dc}a} = U_{ava} - U_{\mathrm{dcav}} \\ \Delta U_{\mathrm{dc}b} = U_{avb} - U_{\mathrm{dcav}} \\ \Delta U_{\mathrm{dcc}} = U_{avc} - U_{\mathrm{dcav}} \end{cases} \tag{14}$$

Equation (14) reflects the mutual-phase DC-side voltage of the CHB energy storage converters degree of imbalance.

As the DC-side voltage unbalance between the three phases ΔU_{dca}, ΔU_{dcb}, *and* ΔU_{dcc} determines the size of the additional fluctuation power P_{a0}, P_{b0}, and P_{c0} injected into each phase during mutual-phase voltage balancing. So, the degree of voltage unbalance is proportional to the additional fluctuation power injected into each phase, as in Eq. (15), with the proportionality coefficient k.

$$\begin{cases} P_{a0} = k \cdot \Delta U_{\mathrm{dca}} \\ P_{b0} = k \cdot \Delta U_{\mathrm{dcb}} \\ P_{c0} = k \cdot \Delta U_{\mathrm{dcc}} \end{cases} \tag{15}$$

By associating Eqs. (11), (14), and (15), the RMS value of the injected zero-sequence voltage U_0 and the phase angle θ_0 required for mutual-phase balance can be found:

$$\begin{cases} U_0 = \dfrac{k\sqrt{\frac{2}{3}(\Delta U_{\mathrm{dca}}^2 + \Delta U_{\mathrm{dcb}}^2 + \Delta U_{\mathrm{dcc}}^2)}}{I} \\ \theta_0 = \delta_i - \lambda \end{cases} \tag{16}$$

where λ is:

$$\lambda = \begin{cases} \tan^{-1}\dfrac{\Delta U_{\mathrm{dc}\beta}}{\Delta U_{\mathrm{dc}\alpha}} & \Delta U_{\mathrm{dc}\alpha} \neq 0 \\ \dfrac{\pi}{2} & \Delta U_{\mathrm{dc}\alpha} = 0 \& \Delta U_{\mathrm{dc}\beta} > 0 \\ -\dfrac{\pi}{2} & \Delta U_{\mathrm{dc}\alpha} = 0 \& \Delta U_{\mathrm{dc}\beta} < 0 \end{cases} \tag{17}$$

The $\Delta U_{\mathrm{dc}\alpha}$ and $\Delta U_{\mathrm{dc}\beta}$ in Eq. (17) indicate that Eq. (14) is converted from the abc three-phase stationary coordinate system to the αβ two-phase stationary coordinate system for the convenience of computation, as shown below:

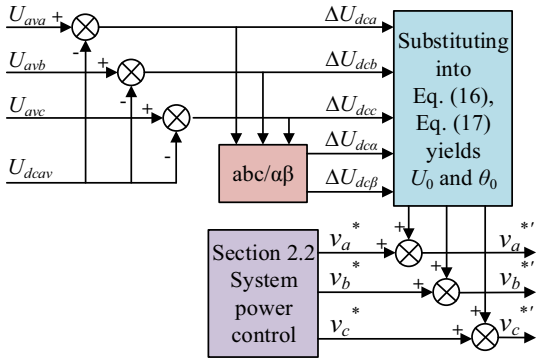

Fig. 8 Block diagram of mutual-phase DC-side voltage balancing control by zero-sequence voltage injection method

$$\begin{bmatrix} \Delta U_{\mathrm{dc}\alpha} \\ \Delta U_{\mathrm{dc}\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \Delta U_{\mathrm{dca}} \\ \Delta U_{\mathrm{dcb}} \\ \Delta U_{\mathrm{dcc}} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}}\Delta U_{\mathrm{dca}} \\ \sqrt{\frac{1}{2}}(\Delta U_{\mathrm{dcb}} - \Delta U_{\mathrm{dcc}}) \end{bmatrix} \tag{18}$$

Note that the larger the proportionality coefficient k, the larger the rms value of the zero-sequence voltage, and the larger its additional power, the more efficient the mutual-phase power balance of the energy storage converters will be. But, k must not be too large, it will affect the safe operation of the system due to too large will cause the system output voltage and current to produce large distortion.

The block diagram of mutual-phase DC-side voltage balancing control based on zero-sequence voltage injection method can be obtained from the above analysis, as shown in Fig. 8. It consists of two parts: system power control and zero-sequence voltage injection. The system power control has been introduced in Sect. 2.2, and its main function is to control the power of the storage converter to produce three-phase voltage modulated waves $v_a{}^*$, $v_b{}^*$, and $v_c{}^*$. The zero-sequence voltage injection module obtains the required zero-sequence voltage RMS value U_0 and the phase angle θ_0 by calculating, and the injection of the zero-sequence voltage component U_0 can change the power distribution among the three phases, making the mutual-phase DC-side voltage balancing. The three-phase modulating voltages $v_a{}^*$, $v_b{}^*$, *and* $v_c{}^*$ are superimposed with the zero-sequence voltage component U_0 to obtain the final modulating wave voltages $v_a{}^{*\prime}$, $v_b{}^{*\prime}$, *and* $v_c{}^{*\prime}$.

5 Simulation and experimentation

5.1 Simulation analysis

The three-module CHB energy storage converter simulation model is built based on Matlab/Simulink for analysis, in order to verify the inner-phase voltage balancing of the SVPWM algorithm with voltage balancing based on simplified vectors, as well as the mutual-phase voltage balancing effect of the zero-sequence voltage injection method. Setting the initial supercapacitor voltage of each module in each phase during charging and discharging is not equal to verify the inner-phase balance, and setting the initial supercapacitor voltage between the three phases is not equal to verify the mutual-phase balance, the main simulation parameters are shown in Table 4.

5.1.1 Inner-phase voltage balancing

The waveforms of the A-phase grid-side voltage, current, and three-phase grid-side current for verifying the DC-side voltage balancing in inner-phase are shown in Fig. 9. It can be seen that in Fig. 9a, the voltage is in the same phase as the current when charging at a given power, which enables the storage of power, and in Fig. 9b, the voltage is 180° out of phase with the current when discharging, which enables the release of power. And the three-phase AC currents of charging and discharging are still symmetrical when the initial voltages of supercapacitors of each module are unequal,

Table 4 Main simulation parameters for charging and discharging of energy storage converters

Parameter	Value
Grid-side line voltage RMS and frequency	380 V, 50 Hz
Switching frequency f_s	4 kHz
Charge/discharge given active power P^*	15 kW/−15 kW
Supercapacitor	0.3F
Filter Inductors L	4mH
A-phase charging initial voltage U_{dca1}, U_{dca2}, U_{dca3}	60 V, 80 V, 100 V
B-phase charging initial voltage U_{dcb1}, U_{dcb2}, U_{dcb3}	75 V, 95 V, 110 V
C-phase charging initial voltage U_{dcc1}, U_{dcc2}, U_{dcc3}	90 V, 110 V, 125 V
A-phase discharge initial voltage U_{dca1}, U_{dca2}, U_{dca3}	190 V, 210 V, 230 V
B-phase discharge initial voltageU_{dcb1}, U_{dcb2}, U_{dcb3}	205 V, 195 V, 185 V
C-phase discharge initial voltageU_{dcc1}, U_{dcc2}, U_{dcc3}	220 V, 200 V, 180 V

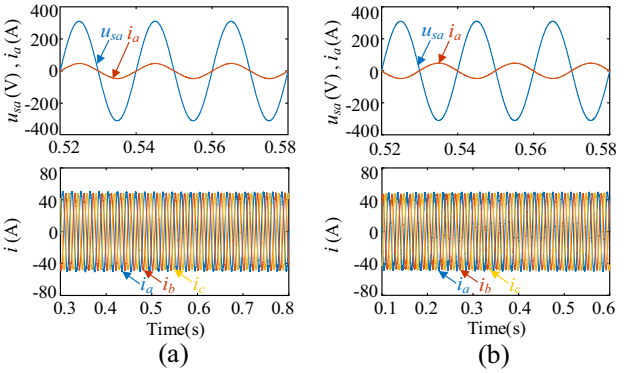

Fig. 9 A-phase grid-side voltage-current and three-phase current waveforms: **a** charging and **b** discharging

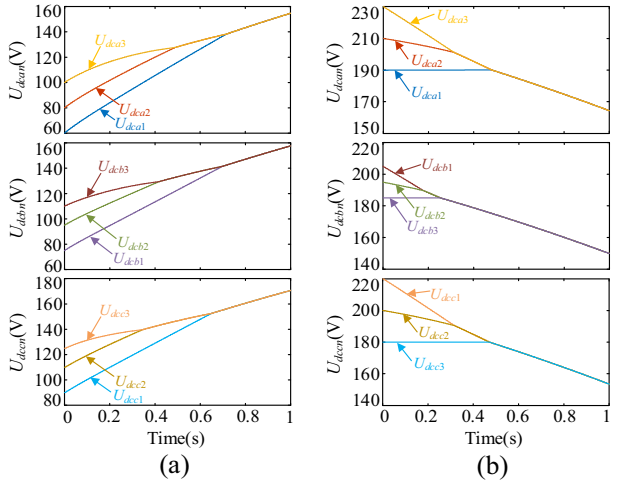

Fig. 10 Voltage on the DC-side of each three-phase module under in-phase balance: **a** charging and **b** discharging

and the voltage balancing algorithm of the simplified vector will not affect the three-phase AC current output.

The DC-side voltage waveform of each module in abc three-phase using the SVPWM algorithm with voltage balancing based on simplified vector is shown in Fig. 10. It can be seen, taking phase A as an example, that the energy storage unit with a large initial value voltage during charging charges at the slowest rate, and the energy storage unit with a small initial value voltage charges at the fastest rate. At last, it charges at the same rate at 0.72 s with decreasing degree of imbalance. Then, the rate of discharge is reversed to that of charging, and the eventual balance is reached at 0.48 s. Although the initial values of the voltages of each energy storage unit in each phase are set to be different, the voltages can still be balanced in a short time, and the charging and discharging can be carried out at the same charging rate. This proves that the proposed inner-phase voltage balancing algorithm has a strong voltage balancing capability.

Figure 11 shows the comparative analysis of the DC-side

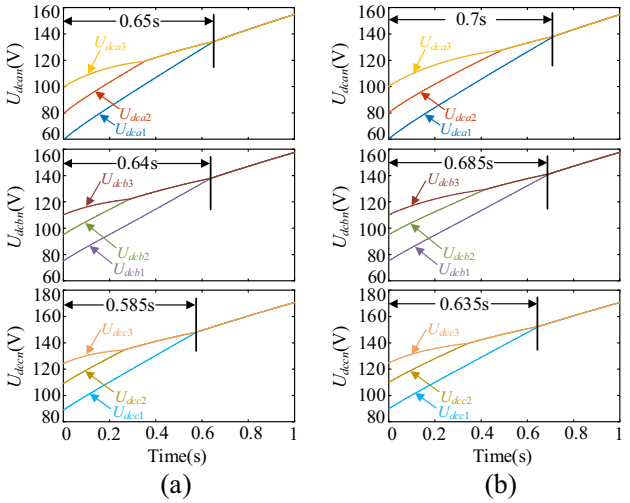

Fig. 11 Voltage on the DC-side of each module in three-phase during charging in inner-phase balance: **a** traditional 3D-SVPWM method and **b** proposed method

voltage of each module in three phases during charging under inner-phase balance. From the figure, it can be seen that the three-phase DC-side voltage of the traditional method takes about 0.65 s, 0.64 s, and 0.585 s to reach balance from unbalance, respectively; and the three-phase DC-side voltage of the proposed method takes about 0.7 s, 0.685 s, and 0.635 s to reach balance from unbalance, respectively. Both the proposed method and the traditional method can reach balance in short time, and the voltage balance of the proposed method is a little slower than that of the traditional method (< 0.05 s).

Figure 12 shows the voltage waveforms of each module port in phase A during charging under converter voltage unbalance. It can be seen that there is leapfrog hopping in the levels of modules 1, 2, and 3 under the traditional 3D-SVPWM method in Fig. 12a, and there is also a simultaneous change in the levels of the three modules when the level of the A-phase output voltage u_a changes. Since the vectors are not simplified, the module moves more frequently and the switching losses are higher. And because the initial supercapacitor voltages of modules 1, 2, and 3 are 60 V, 80 V, and 100 V, respectively, when setting up A-phase charging, module 1 needs to charge faster to get more power to maintain balance, followed by module 2 and finally module 3. Therefore, module 1 needs to have a high level to get more power and maintains the + 1 level when $i_a > 0$ in Fig. 12a. However, there still exists a situation that all three module levels change at the same time when the level changes under the non-simplified vectors, such as at voltage amplifica-tion (1) and (2) in Fig. 12a.

The port voltage of each module in phase A under the proposed method is shown in Fig. 12b. It can be seen that there is no leapfrog hopping in each module when the u_a level changes, presenting a step wave, and only one of the three modules has a change in level. It is indicated that the switching devices of each module of the converter under the SVPWM algorithm with voltage balancing based on simplified vector have fewer actions, low voltage stress, and small switching losses.

In addition, in order to further verify the advantages of the proposed method over the traditional method in terms of system switching loss, the average value of the number of

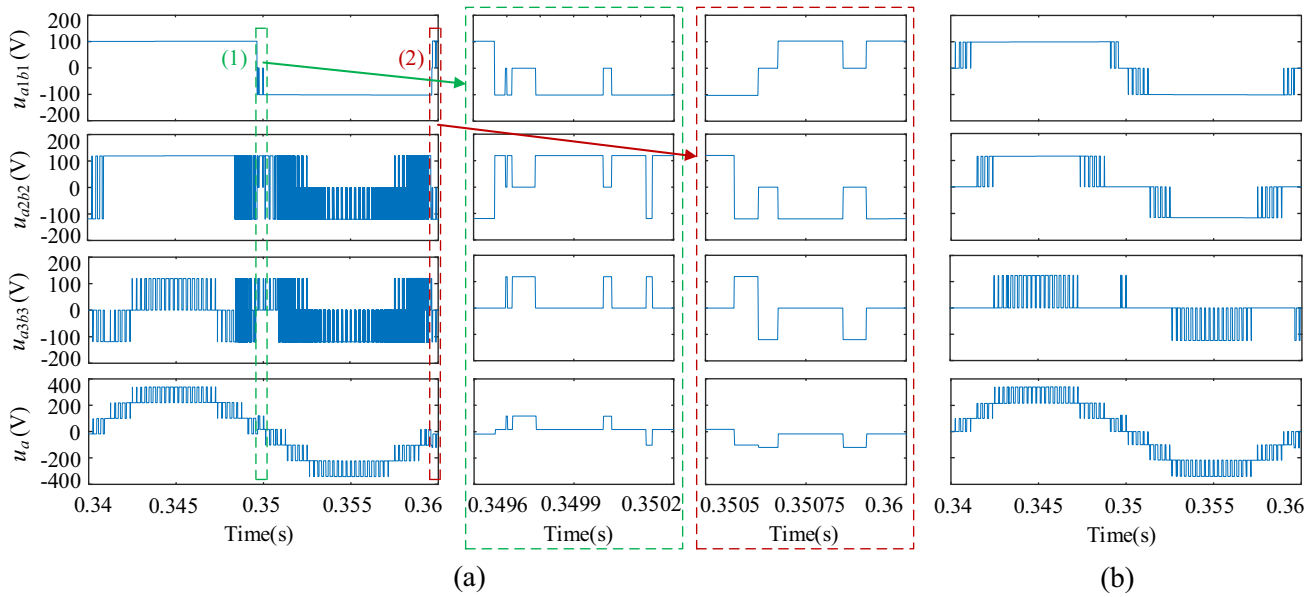

Fig. 12 Voltage waveforms of each module port in phase A during charging under voltage unbalance: **a** traditional 3D-SVPWM method and **b** proposed method

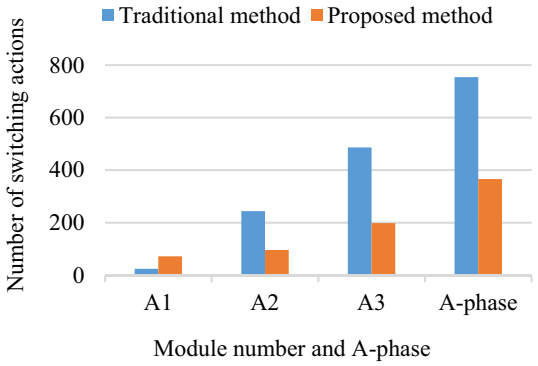

Fig. 13 Number of A-phase switching actions

Table 5 Comparison of traditional 3D-SVPWM algorithm with voltage balancing and the proposed algorithm

	The traditional 3D-SVPWM algorithm with voltage balancing [20, 21]	The proposed algorithm
Number of vectors used in phase A	27	**15**
System complexity	High	**Low**
Module level leapfrog hopping	Yes	**No**
Simultaneous module level change	Yes	**No**
Voltage balancing capability	High	**High**
Grid-side current THD (charging)	1.60%	**1.38%**
Grid-side current THD (discharge)	1.28%	**1.05%**

Bold indicates the advantages and innovations of the control algorithm proposed in this manuscript

switching actions for 3 cycles after 0.3 s is counted by simulation in Fig. 13, taking the converter A-phase as an example. It can be seen from the figure that although the number of switching actions in the first module A1 in phase A using the proposed method is slightly more than the traditional 3D-SVPWM with voltage balancing method. But, the number of switching actions in the other modules and the total number of switching actions in phase A is reduced by about 50% compared to the traditional method, which significantly reduces the switching losses.

According to the comparison between the traditional 3D-SVPWM algorithm with voltage balancing and the proposed algorithm in Table 5, it can be seen that the proposed algorithm has the following advantages over the traditional algorithm. First, the proposed algorithm reduces the number

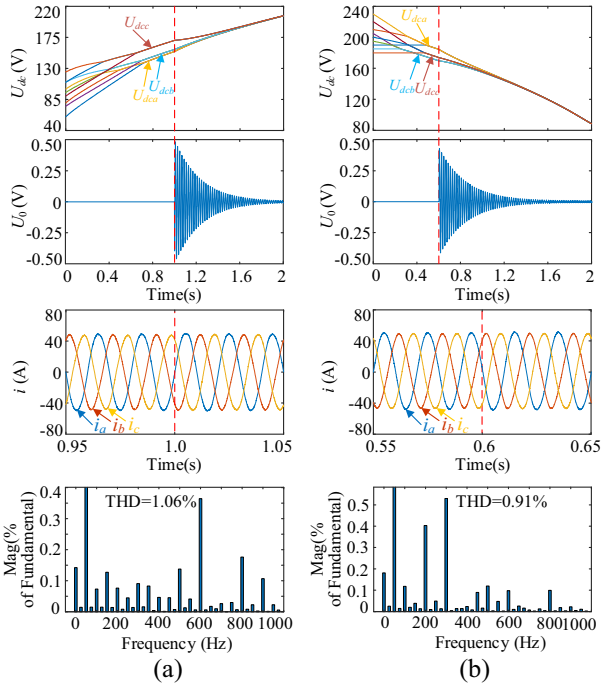

Fig. 14 Simulation results under mutual-phase balance: **a** charging and **b** discharging

of voltage vectors used in a single phase by 44.4%, which makes the system less burdensome and easy to expand to more modules in cascade. Second, compared with the traditional algorithm, the proposed algorithm greatly reduces the switching losses; and the network side current THD is also smaller.

5.1.2 Mutual-phase voltage balancing

Figure 14 shows the analysis of three-phase DC-side voltage, injected zero-sequence voltage, three-phase grid-side current, and grid-side current THD under mutual-phase balance after adding inner-phase balance. It can be seen that the mutual-phase voltage balancing in Fig. 14a cannot be achieved when charging without injecting zero-sequence voltage and there is a deviation value. The mutual-phase balancing starts after the injection of the zero-sequence voltage at 1 s. As the zero-sequence voltage decreases, the degree of unbalance between the three mutual-phases decreases, and eventually charges at the same rate at 1.8 s. Figure 14b shows the mutual-phase balancing by injecting the zero-sequence voltage at 0.6 s during discharge, and the balancing is achieved at 1.4 s as the zero-sequence voltage decreases. Also, the mutual-phase cannot be balanced automatically when it is not injected. Moreover, the three-phase grid-side current does not change when the zero-sequence voltage is injected at 1 s and 0.6 s. It means that zero-sequence voltage

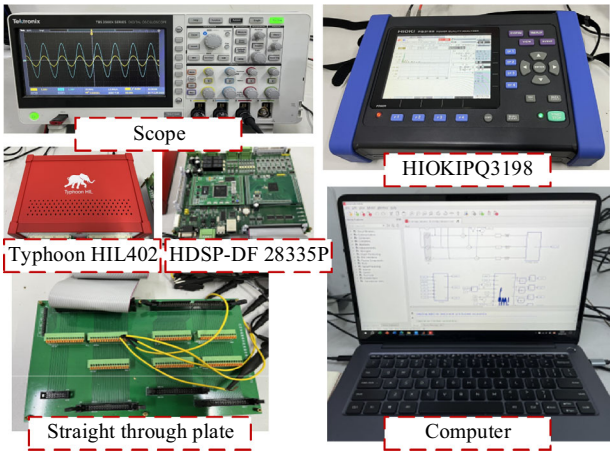

Fig. 15 HIL experimental platform

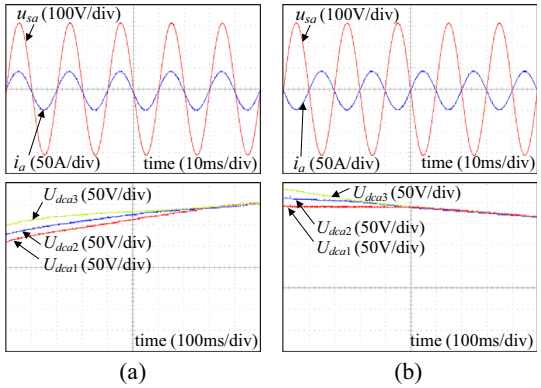

Fig. 16 HIL experimental waveforms of phase A under inner-phase balance: **a** charging and **b** discharging

injection does not affect the output of three-phase grid-side current, which verifies the feasibility and correctness of the zero-sequence voltage injection method. The grid-side currents are analyzed for THD after both inner-phase and mutual-phase are balanced. From the THD analysis of the grid-side currents in Fig. 14a and b, it can be seen that the grid-side current during charging: THD = 1.06%, and the grid-side current during discharging: THD = 0.91%, both of which are less than 2% and satisfy the national requirement of less than 5% of the grid entry.

5.2 HIL experimental verification

A hardware-in-the-loop (HIL) experimental platform as shown in Fig. 15 is built to further verify the feasibility of the simulation results. It mainly provides HIL experimental verification of the proposed SVPWM algorithm with voltage balancing based on simplified vector for inner-phase voltage balancing as well as the zero-sequence voltage injection method for mutual-phase voltage balancing. Among them, the main circuit is built in the Typhoon HIL402 platform, the HDSP-DF28335P controller is used to output pulses, and the harmonic distortion rate of the grid-side currents is analyzed by using the HIOKI power quality analyzer PQ3198. The main parameters of the HIL experiment are consistent with the simulation parameters in Table 4.

Figure 16 shows the HIL experimental waveforms of phase A under inner-phase balance, which shows that the voltage and current are in the same phase in Fig. 16a for charging, and the voltage and current are 180° out of phase in Fig. 16b for discharging. The experimental waveforms are consistent with the simulation results, and the storage and release of power are achieved. When charging, with the addition of SVPWM algorithm with voltage balancing based on simplified vector, it finally reaches balance at 0.8 s. When discharging, with the decrease of the degree of imbalance, it reaches balance at 0.5 s, and finally charging and discharging at the same rate, which verifies that the inner-phase voltage balancing algorithm proposed in this paper has a strong voltage balancing capability.

The HIL experimental waveforms of the port voltage and phase voltage of each module in phase A during charging under converter voltage unbalance are shown in Fig. 17. It can be seen that Fig. 17a under the traditional 3D-SVPWM method exists a situation in which the levels of the three modules change at the same time when the phase voltage u_a level changes, and level leapfrog hopping occurs in all three modules. And under the simplified vector in Fig. 17b, each module did not show the level leapfrog hopping when the phase voltage u_a level changes. In addition, the output voltage of only one module unit among three module units has one level change, which is the same as the simulation results, verifying that the proposed algorithm has small switching losses.

The average value of computing time for the proposed method and the traditional method calculated in the HIL platform is shown in Fig. 18. It can be seen from Fig. 18 that the algorithm computation time of the traditional method is 19.18 μs, which accounts for 27.4% of the control cycle, and the algorithm computation time of the proposed method is 13.51 μs, which accounts for 19.3% of the control cycle. The proposed method reduces 5.67 μs and enhances the operation speed by about 30% compared to the traditional method. This shows that the proposed simplified vectors algorithm can effectively reduce the computing burden of the controller and improve the response speed of the system.

Figure 19 shows the HIL experimental waveforms of mutual-phase voltage balancing without adding zero-sequence voltage injection and mutual-phase voltage balancing with adding zero-sequence voltage injection, as well as the THD analysis of the grid-side currents. The supercapacitor voltages of the first module in the three phases of A, B, and C are selected for the analysis because only four waveforms

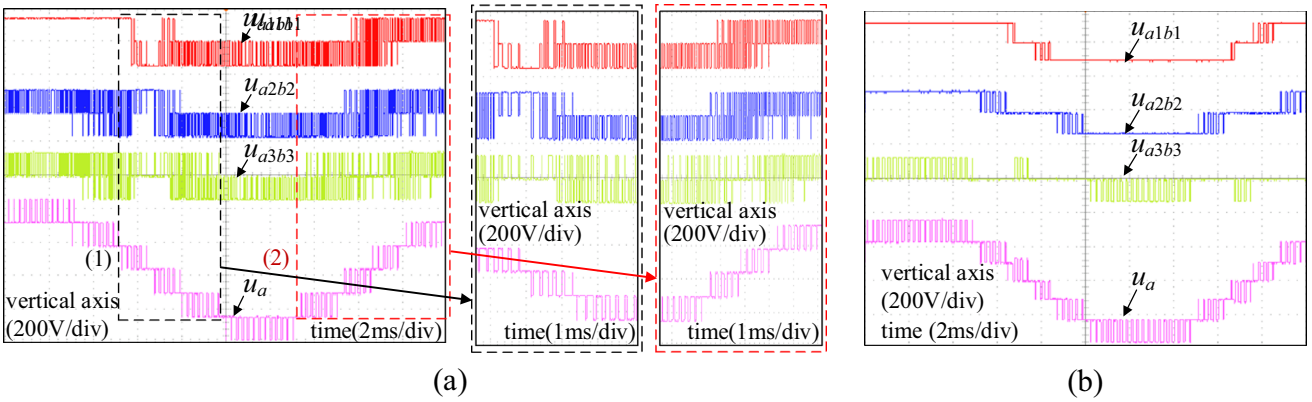

Fig. 17 Waveforms of each module port voltage and phase voltage in phase A during charging under voltage unbalance: **a** traditional 3D-SVPWM method and **b** proposed method

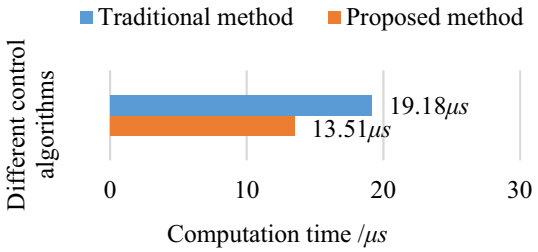

Fig. 18 Algorithmic computation time

can be observed at one time by the TBS 2000X SERIES oscilloscope. It can be seen that in Fig. 19a charging without adding the mutual-phase balance of zero-sequence voltage injection, it does not reach the balance automatically, while with the addition of the mutual-phase balance, it reaches the balance at 1.3 s. In Fig. 19b, the discharging is consistent with the charging, and finally balance at 0.8 s. Then, the THD of the grid-side current is 1.69% and 1.87%, respectively, after charging and discharging balance, both are less than 2% and meet the national requirement of less than 5% for grid entry.

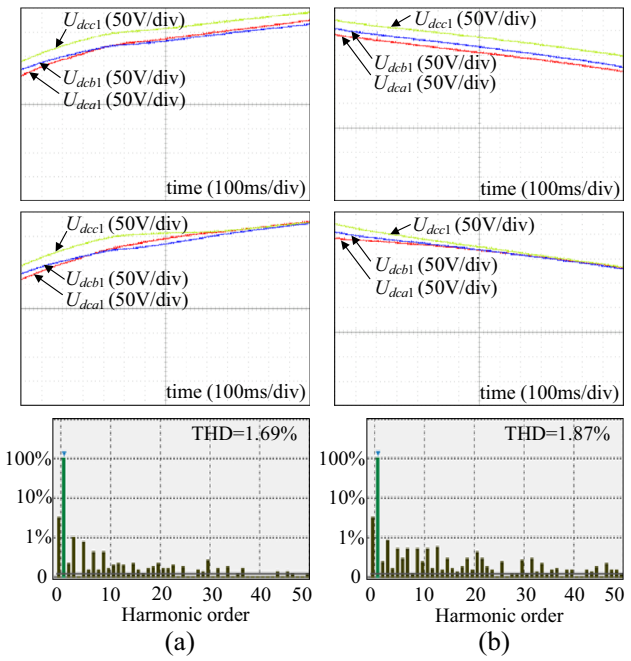

Fig. 19 Mutual-phase balance HIL experimental waveforms and grid-side current THD analysis diagrams: **a** charging and **b** discharging

6 Conclusion

A SVPWM algorithm with voltage balancing based on simplified vector is proposed in this paper for the converter inner-phase voltage balancing with CHB energy storage converters as the research background, which overcomes the problems of larger number of voltage vectors and higher switching losses. Firstly, the algorithm carries out simplification of voltage vectors by targeting strong voltage balancing capability and low switching losses and simplifies a total of 27 voltage vectors to 15 vectors in a single phase of a conventional SVPWM with voltage balancing, which is a reduction of 44.4% of the vectors. It makes the algorithm simpler, the system burden smaller, and it is easier to extend to cascaded H-bridge converters with more modules. Besides, the algorithm prevents the occurrence of leapfrog hopping in the level of each module and makes only one level change in one module when the phase voltage level changes, which greatly reduces switching losses. Finally, the additional power generated by zero-sequence voltage injection is used to change the distribution of power among the three phases, thus changing the charging and discharging speeds of the three-phase energy storage units, so that the mutual-phase voltage is balanced. The THD of the charging and discharging grid-side currents meets the requirements for grid-connection after both inner-phase and mutual-phase voltages are balanced.

It is verified by the simulation and experimental results that the proposed control algorithm is correct.

Author contributions ZL wrote the main manuscript text; DR wrote the section of simulation; and JC, KZ, YY, and FW wrote the section of experiment jointly.

Funding This work was supported in part by the National Natural Science Foundation of China under Grant 51907083 and in part by the Basic Research Project of Xuzhou under Grant KC23024.

Data availability The datasets used or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest The authors declared no potential conflicts of interest with respect to the research.

Ethical approval Not applicable.

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