Electrical Engineering (2023) 105:2889–2908
https://doi.org/10.1007/s00202-023-01829-z

ORIGINAL PAPER

Experimental investigation on a Solar Photovoltaic system using reduced multilevel connections for power quality improvement

P. Vivek[1] · **N. B. Muthu Selvan**[2]

Received: 9 November 2022 / Accepted: 8 April 2023 / Published online: 23 May 2023

Abstract
This research paper investigates the new multilevel connections with minimum number of components as a voltage source inverter (VSI) which is connected in parallel as shunt active power filter (SAPF) for the purpose of the improving power quality and reactive power compensation in power systems. The main contribution of this paper is the design & development of modular structure which is capable of producing a wide range of output levels (9,11,13,15,17,19,21,23,25,27,29 and 31) using Asymmetric PV sources. A comparative study is made with other (27-level) reduced multilevel connection (RMC) topologies suitable for asymmetric input sources from solar photovoltaics (SPV). In addition, the state space analysis and the loss calculations are performed in order to ensure that the inverter is superior to the conventional topologies. The switching angles are determined using Particle Swarm Optimization (PSO) method. The implementation part of RMC is carried out with the selective harmonic elimination (SHE) which mitigates harmonics in the system. MATLAB/Simulink software is used for modelling of the proposed system. An Experimental setup of the proposed multilevel connections is developed and then it is experimentally investigated. A capacity of 3 KWp Solar PV system which feeds the DC input to the developed prototype. On the basis of the research findings, it is possible to draw the conclusion that the proposed inverter topology minimizes the voltage harmonics by 2.56% and current harmonics by 2.33% which enhances power quality, compensates the reactive power, lessens the number of components used by 12 and more cost effective.

Keywords Multilevel inverter · Power quality enhancement · Harmonic mitigation · Reactive power compensation · Solar PV system

1 Introduction

The rising need for electricity has led to a widespread adoption of renewable energy sources(RESs). This means we need to do something to extend the usefulness of our most basic forms of energy. To extend the availability of fossil fuels, various distinct methods have been developed. Efficient use of existing power sources is one option, as is expanding the use of renewable energy technologies like solar panels, wind turbines, thermal energy conversion from the ocean, wave energy converters, and so on. As a matter of procedure, power electronic converters are liable for meeting those commitments by using an inverter (DC to-AC converter) that produces an asymmetrical square wave. Low-pass filters are employed to eliminate the high and low harmonics of a waveform, improving its overall quality. From the studies of [1–4], it can be seen that, two level inverters were firstly conceived to convert AC into DC. However, these converters had a number of drawbacks, including excessive switching losses, high switching losses, high THD, high voltage stress (dv/dt), low efficiency, and the requirement for filters, among others. This has led to the development of multilevel inverters (MLI), which are ideal for medium-voltage and high-power applications. MLI produces a frequency response with a better emission than two level inverters. [5, 6], find out by comparing multilevel inverters to two-level inverters, there are various advantages such as less voltage stress on switches, less harmonic distortion on voltage waveforms, and less dv/dt on switching devices. Its benefits are mostly concentrated on enhancing the output signal quality and increasing the nominal power of the inverters. [7–14],

✉ P. Vivek
vivekpsgped11@gmail.com

[1] Velammal Institute of Technology, Chennai, India

[2] Sri Sivasubramaniya Nadar College of Engineering, Chennai, India

Table 1 Conventional literature survey on 27 -Level reduced components count Multilevel inverter

S. no	Topology	N_{level}	N_{DC}	N_{SW}	N_{Gdv}	N_{Cap}	N_D
1	NPC	27	1	52	52	26	52
2	FC	27	1	52	52	26	52
3	CHB	27	12	52	52	13	52
4	[1]	27	3	14	14	0	20
5	[2]	27	13	28	28	–	28
6	[3]	27	13	26	26	–	26
7	[6]	27	3	13	13	-	13
8	[9]	27	1	13	52	3	16
9	[21]	27	13	28	18	–	28
10	[40]	27	1	52	52	–	52
11	[45]	27	1	52	52	325	52
12	[44]	27	13	52	52	–	52
13	[46]	27	13	30	30	–	30
14	[43]	27	13	28	28	–	28
15	[46]	27	7	18	18	12	18

N_{Level} Quantity of DC Sources, N_{DC} Quantity of DC Sources, N_{SW} Quantity of Switches, N_{Gdv} Quantity of Gate driver, N_{Cap} Quantity of Capacitors , N_D Quantity of Diodes

suggests that researchers and scholars may now concentrate exploring emerging innovations that must be linked to renewable power facilities due to the increasing attention on sustainable power resources, particularly solar photovoltaic (SPV) power. Multilevel inverters/converters (MLI_S), particularly, the field which has drawn the interest of many scholars [15]. shows that the usage of renewable energy is now more advantageous from a political and financial standpoint. Due to contemporary technology, ambiently renewable energies, encompass energy from the sun panels along with energy from the wind turbines, there are plenty different categories in energy and have grown incredibly common and challenging. In reality, PV solar sources have a variety of uses, such as pollution-free sources. [16–32], through their analysis shows cascaded H Bridge Multilevel (CHB) Inverters are typically utilised in static var uses, like as battery-based and renewable energy applications. The wye form or the delta form can be used with CHB multilevel inverters. From [30] it can be seen that modules can also be used to create multilayer converters, giving rise to multi-modular converters (MMCs). A certain multilevel converter can produce a levels using a DC source and two switches, hence it may be regarded as a module. More levels can be attained if these modules are joined in succession. Through the study by [33] it is a common fact that problems for grid-tied users significant concern with voltage stability, that can be brought on by frequency inverters in photovoltaic systems and affects utility firms as well as power variance. From the analysis of [34] nonlinear electric and electronic loads cause harmonics, which are multiples of the fundamental frequency. From studies of [35] multilevel converters with lower power switches & very few circuit components are necessary to construct in order to decrease the price, and inefficiencies in the multilevel inverter and satisfy the power needs. But at the other end, the symmetrical MLI has the ability to be a more effective PV converter because it can raise the inverter's voltage levels despite running at a lower switching frequency. [36–58], states the distortion of the harmonic components also with the resultant spectrum are also among the key benefits of using the SHE methodology over alternative methods. Since the total eradication of a specific set of harmonics, being the primary function of such filters, is guaranteed, it is essential to take into account this modulating technique in order to enhance the performance of passive active filters.

From Table 1 Based on the research findings the objectives to design the proposed topology has the following benefit.

- Reduces the number of Power switch components usage.
- Reduces the usage of DC sources, Capacitors & gate drive circuits.
- Increases the number of output voltage level with lesser number of components.
- Reduces the total harmonic distortion as per the IEEE519 standard.
- Implementation of SHE based on soft-computing technique with PI controller improves voltage regulation.
- Minimizes the losses which leads to the improvement of efficiency.
- Better the reactive power compensation

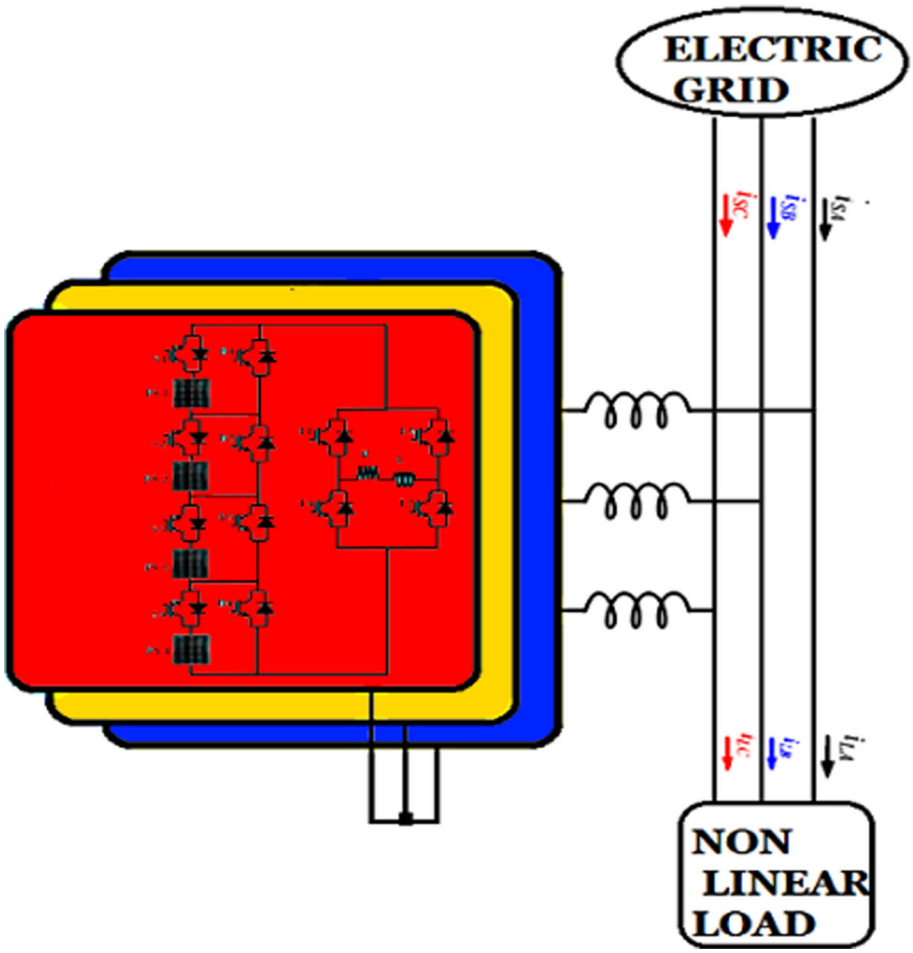
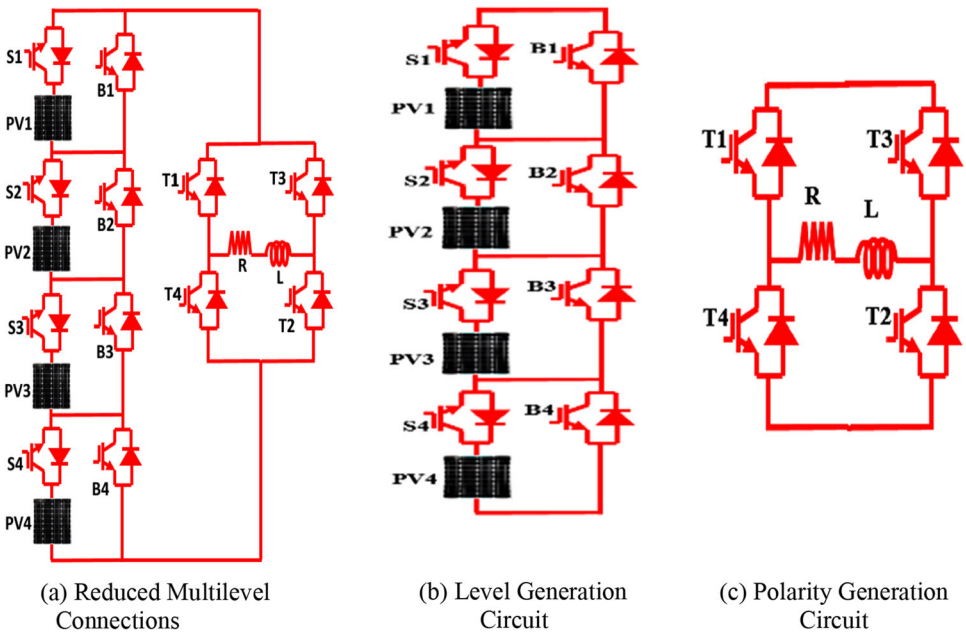


Fig. 1 Proposed Multilevel Connections



(a) Reduced Multilevel Connections (b) Level Generation Circuit (c) Polarity Generation Circuit

Fig. 2 **a** Reduced Multilevel Connections, **b** Level Generation Circuit, **c** Polarity Generation Circuit

Table 2 Elements based on proposed system

Elements	Constructed on the basis of N_L Asymmetric MLI	Constructed on the basis of units(n)
Number of levels	N_L	27n
Number of Switches	$(N_L\text{-}3) / 2$	12n
Number of Diodes	$(N_L\text{-}3) / 2$	12n
Number of Gate Drivers	$(N_L\text{-}3) / 2$	12n
Number of DC sources	$(N_L\text{-}3) / 6$	4n

The organisation of this article is as follows: The overview of reduced multilevel connections is covered in Sect. 2. The converter's operating modes are included in the design. The state space analysis of the converter is covered in Sect. 3. The modelling of solar PV Module is covered in Sect. 4. The Theory of SHE is covered in Sect.5. The switching process of the proposed converter is covered in Sect. 4. The loss analysis of the proposed RMC is shown in Sect. 5. The system's reactive power compensation is described in Sect. 6. The cost calculation is presented in Sect. 7. The result and discussion findings are presented in Sect. 8. The comparative analysis of an asymmetrical 27-level inverter is covered in Sect. 9 The ultimate conclusions are presented in Sect. 10.

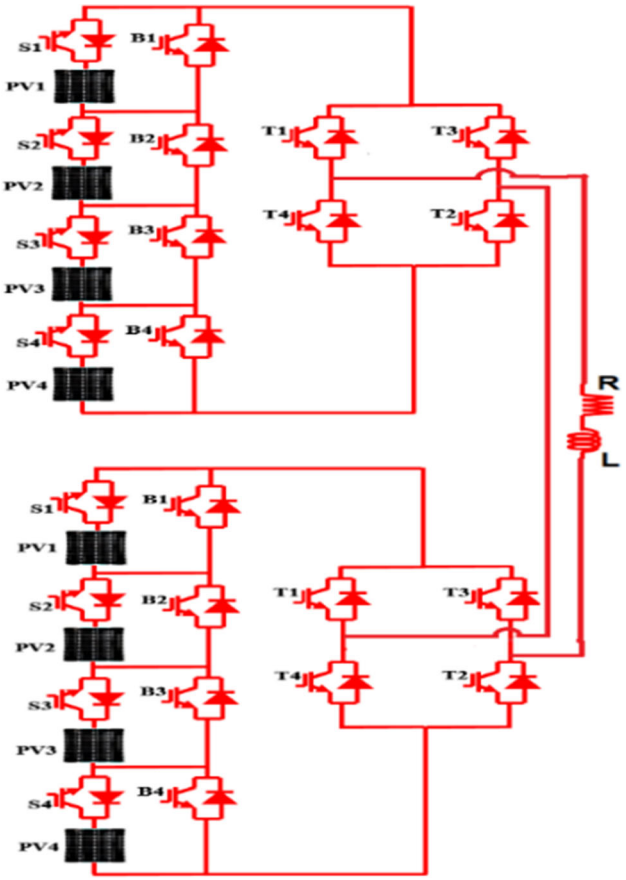


Fig. 3 Cascaded Mode Connection

2 Proposed multilevel connections

The proposed approach only needs twelve switches to build the power circuit, while the conventional and trinary structures each need a different control circuit in order to reach level 27. Figs.1 and 2a depicts the structure of a simple, single-phase RMC. The switching sequence indicates in order to achieve 27 levels, Fig. 2b the polarity generation switches that generate positive half-cycles (T1,T2) and negative half-cycles (T3,T4) must be set to the ON position, while the switches responsible for producing level generation (S1–S4, B1–B4) as shown in Fig. 2c must be adjusted so that intermediate levels are produced. The PV system supplies the DC input voltages. Most likely, PV1, PV2, PV3& PV4 are the inputs. PV1 is the only source of energy for the first tier while the other PV sources are running. As with the previous levels, Level 27 is unlocked by toggling switches. According to the PV inputs, the RMC has the potential to produce 11 different levels. The range of possible output levels from the RMC given the PV inputs. The level 27 is generated by a combination of input DC sources fed by the PV array in the following ratio: 1:2:3:7.

Table 2 shows the elements of the proposed inverter based on number of levels and number of units on symmetric & Asymmetric Configuration.

When the developed structure is connected in cascaded mode Fig. 3 the amount of voltage levels obtained is $2N_L$ i.e., it will be equal to 54-Voltage Levels for the above topology.

The proposed design has various modes of operation which are shown in Fig. 4a–n. During the positive half cycle the voltages $+1V_{dc}, +2V_{dc}, +3V_{dc}, +4V_{dc}, +5V_{dc}, +6V_{dc}, +7V_{dc}, +8V_{dc}, +9V_{dc}, +10V_{dc}, +11V_{dc}, +12V_{dc}, +13V_{dc}$ are obtained. For the negative obtained. e half cycle the output voltages obtained are– $1V_{dc}, -2V_{dc}, -3V_{dc}, -4V_{dc}, -5V_{dc}, -6V_{dc}, 7V_{dc}, 8V_{dc}, -9V_{dc}, -10V_{dc}, -11V_{dc}, -12V_{dc}, -13V_{dc}$ are. Table 3 shows the current path, number of switches in conduction and the developed voltage level corresponding to the switching strategy. The Positive voltage levels $V_0 = +1V_{dc}, +2V_{dc}, +3V_{dc}, +4V_{dc}, +5V_{dc}, +6V_{dc}, +7V_{dc}, +8V_{dc}, +9V_{dc}, +10V_{dc}, +11V_{dc}, +12V_{dc}, +13V_{dc}$ are obtained by using the same switching strategies at positive half cycle. In the negative half cycle, the polarity generation switches T1 and T2 are switched on and Stages (I-XIV) are achieved. Tables 4 and 5 show the voltage &

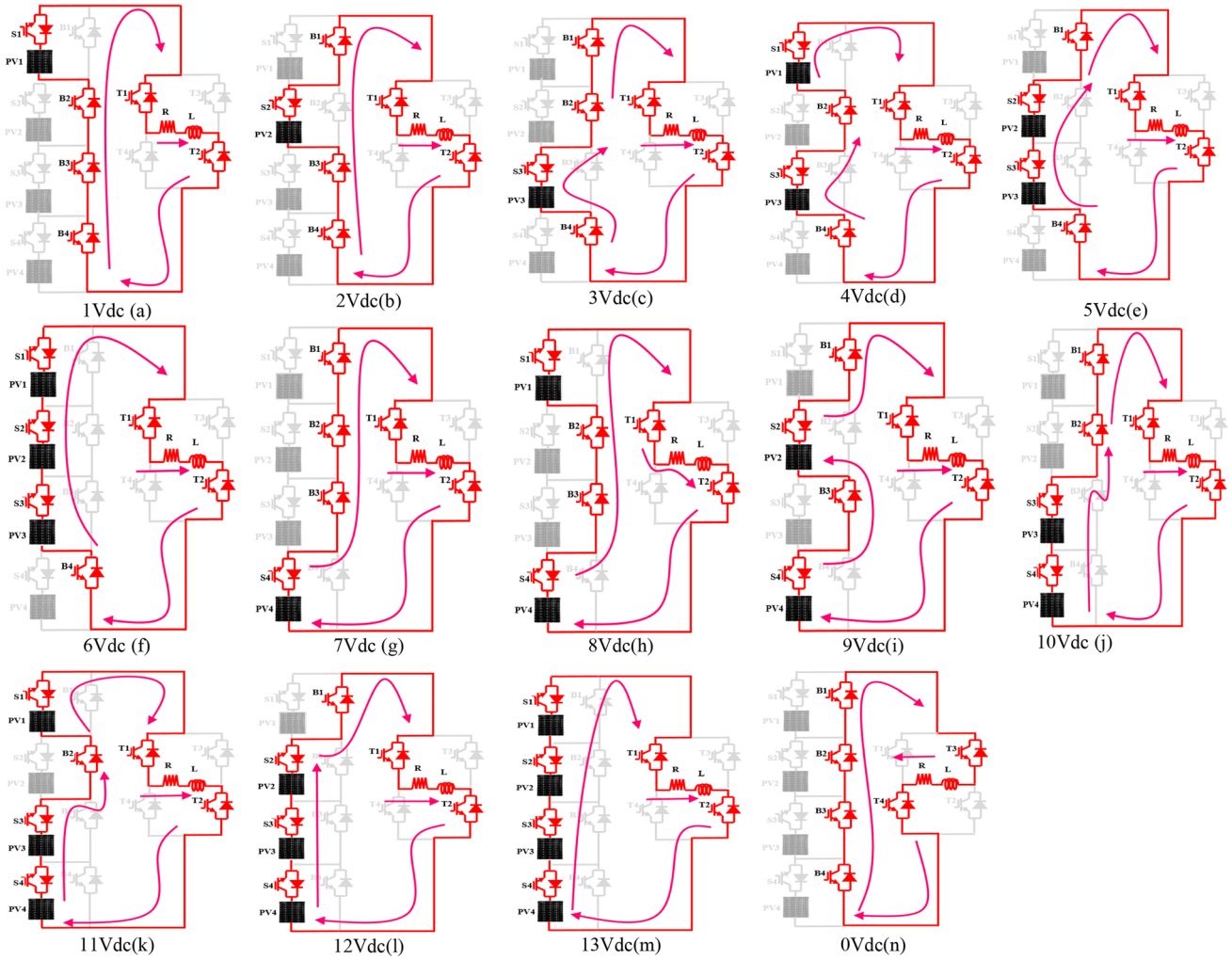


Fig. 4 **a**–**n**: Modes of operation of the RMC positive half cycle

current stress of the switches at each level which is significantly reduced from the proposed topology which leads to the reduction of switching & conduction loss. By the reduction of switching & conduction loss the overall efficiency is improved. Figure 5a, b shows the switching and conduction loss of the proposed topology when compared to the existing topology.

3 State space modeling of proposed RMC

A system is represented in state space model by taking the systems input, output parameters and state variables.

General state space model is given by

$$\dot{X} = AX + BU \text{ (State Space Equation)} \tag{1}$$

$$Y = CX + DU \text{ (Output Equation)} \tag{2}$$

Here X = State Variable, U = Input Variable, Y = Output Variable & $\dot{X}$ = State Derivative The state space model of the RMC is shown in Fig. 6.

Let,

$$\text{Hb} = \left\langle \begin{matrix} 1 \quad \text{for} \ + \text{ve half cycle} \\ -1 \ \text{for} \ - \text{ve half cycle} \end{matrix} \right\rangle \tag{3}$$

The variable Hb is denoted for the H-Bridge in the proposed topology. Hence, the net output V_{L} for the inverter is given by:

$$\text{V}_{\text{L}} = \|1111\| \begin{bmatrix} \vartheta 1 \ \text{Hb} \\ \vartheta 2 \ \text{Hb} \\ \vartheta 3 \ \text{Hb} \\ \vartheta 4 \ \text{Hb} \end{bmatrix} \|\text{Vdc}\| \tag{4}$$

where, V_{dc} is the sum of each dc source, and $\vartheta 1$ to $\vartheta 4$ is the comparator output signals.

Table 3 Current Path of the Proposed system

Stages	Switches in conduction	Current path	Figure	Output voltage
I	S1,B2,B3,B4,T1,T2	$PV_1^+ \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow B3 \rightarrow B2 \rightarrow PV_1^-$	4a	V_{dc}
II	S2,B1,B4,B3,T1,T2	$PV_2^+ \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow B3 \rightarrow PV_2^-$	4b	$2V_{dc}$
III	S3,B1,B2,B4,T1,T2	$PV_3^+ \rightarrow B2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow PV_3^-$	4c	$3V_{dc}$
IV	S1,S3,B2,B4,T1,T2	$PV_3^+ \rightarrow B2 \rightarrow PV_1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow PV_3^-$	4d	$4V_{dc}$
V	S2,S3,B1,B4,T1,T2	$PV_3^+ \rightarrow PV_2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow PV_3^-$	4e	$5V_{dc}$
VI	S1,S2,S3,B4,T1,T2	$PV_3^+ \rightarrow PV_2 \rightarrow PV_1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow B4 \rightarrow PV_3^-$	4f	$6V_{dc}$
VII	S4,B1,B2,B3,T1,T2	$PV_4^+ \rightarrow B3 \rightarrow B2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4 g	$7V_{dc}$
VIII	S1,S4,B2,B3,T1,T2	$PV_4^+ \rightarrow B3 \rightarrow B2 \rightarrow PV_1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4 h	$8V_{dc}$
IX	S2,S4,B1,B3,T1,T2	$PV_4^+ \rightarrow B3 \rightarrow PV_2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4i	$9V_{dc}$
X	S3,S4,B1,B2,T1,T2	$PV_4^+ \rightarrow PV_3 \rightarrow B2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4j	$10V_{dc}$
XI	S1,S3,S4,B2,T1,T2	$PV_4^+ \rightarrow PV_3 \rightarrow B2 \rightarrow PV_1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4 k	$11V_{dc}$
XII	S2,S3,S4,B1,T1,T2	$PV_4^+ \rightarrow PV_3 \rightarrow PV_2 \rightarrow B1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4 l	$12V_{dc}$
XIII	S1,S2,S3,S4,T1,T2	$PV_4^+ \rightarrow PV_3 \rightarrow PV_2 \rightarrow PV_1 \rightarrow T_1 \rightarrow R^L \rightarrow T_2 \rightarrow PV_4^-$	4 m	$13V_{dc}$
XIV	B1, B2, B3, B4, T3, T4	$B1 \rightarrow T_3 \rightarrow R^L \rightarrow T_4 \rightarrow B4 \rightarrow B3 \rightarrow B2$	4n	$0V_{dc}$

Table 4 Voltage stress on the switches for each level

Levels	S_1	S_2	S_3	S_4	B_1	B_2	B_3	B_4	T_1	T_2	T_3	T_4
+ 1 V_{dc}	0 V	2 V	3 V	7 V	1 V	0 V	0 V	0 V	0 V	0 V	1 V	1 V
+ 2V_{dc}	1 V	0 V	3 V	7 V	0 V	2 V	0 V	0 V	0 V	0 V	2 V	2 V
+ 3 V_{dc}	1 V	2 V	0 V	7 V	0 V	0 V	3 V	0 V	0 V	0 V	3 V	3 V
+ 4 V_{dc}	0 V	2 V	0 V	7 V	1 V	0 V	3 V	0 V	0 V	0 V	4 V	4 V
+ 5 V_{dc}	1 V	0 V	0 V	7 V	0 V	5 V	5 V	0 V	0 V	0 V	5 V	5 V
+ 6 V_{dc}	0 V	0 V	0 V	7 V	6 V	6 V	6 V	0 V	0 V	0 V	6 V	6 V
+ 7 V_{dc}	1 V	2 V	3 V	0 V	0 V	0 V	0 V	7 V	0 V	0 V	7 V	7 V
+ 8 V_{dc}	0 V	2 V	3 V	0 V	1 V	0 V	0 V	7 V	0 V	0 V	8 V	8 V
+ 9 V_{dc}	1 V	0 V	3 V	0 V	0 V	2 V	0 V	7 V	0 V	0 V	9 V	9 V
+ 10 V_{dc}	1 V	2 V	0 V	0 V	0 V	0 V	10 V	10 V	0 V	0 V	10 V	10 V
+ 11 V_{dc}	0 V	2 V	0 V	0 V	1 V	0 V	10 V	10 V	0 V	0 V	11 V	11 V
+ 12 V_{dc}	1 V	0 V	0 V	0 V	0 V	12 V	12 V	12 V	0 V	0 V	12 V	12 V
+ 13 V_{dc}	0 V	0 V	0 V	0 V	13 V	13 V	13 V	13 V	0 V	0 V	13 V	13 V
0 V_{dc}	13 V	13 V	13 V	13 V	13 V	13 V	13 V	13 V	0 V	0 V	13 V	13 V

Table 5 Current stress on the switches for each level

Levels	S_1	S_2	S_3	S_4	B_1	B_2	B_3	B_4	T_1	T_2	T_3	T_4
+ 1 V_{dc}	I_{RL}	0A	0A	0A	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 0V_{dc}	0A	I_{RL}	0A	0A	I_{RL}	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 3 V_{dc}	0A	0A	I_{RL}	0A	I_{RL}	I_{RL}	0A	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 4 V_{dc}	I_{RL}	0A	I_{RL}	0A	0A	I_{RL}	0A	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 5 V_{dc}	0A	I_{RL}	I_{RL}	0A	I_{RL}	0A	0A	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 6 V_{dc}	I_{RL}	I_{RL}	I_{RL}	0A	0A	0A	0A	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 7 V_{dc}	0A	0A	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	I_{RL}	I_{RL}	0A	0A
+ 8 V_{dc}	I_{RL}	0A	0A	I_{RL}	0A	I_{RL}	I_{RL}	0A	I_{RL}	I_{RL}	0A	0A
+ 9 V_{dc}	0A	I_{RL}	0A	I_{RL}	I_{RL}	0A	I_{RL}	0A	I_{RL}	I_{RL}	0A	0A
+ 10 V_{dc}	0A	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}
+ 11 V_{dc}	I_{RL}	0A	I_{RL}	I_{RL}	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	0A
+ 12 V_{dc}	0A	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	0A	0A	I_{RL}	I_{RL}	0A	0A
+ 13 V_{dc}	I_{RL}	I_{RL}	I_{RL}	I_{RL}	0A	0A	0A	0A	I_{RL}	I_{RL}	0A	0A
0 V_{dc}	0A	0A	0A	0A	0A	0A	0A	0A	I_{RL}	I_{RL}	0A	0A

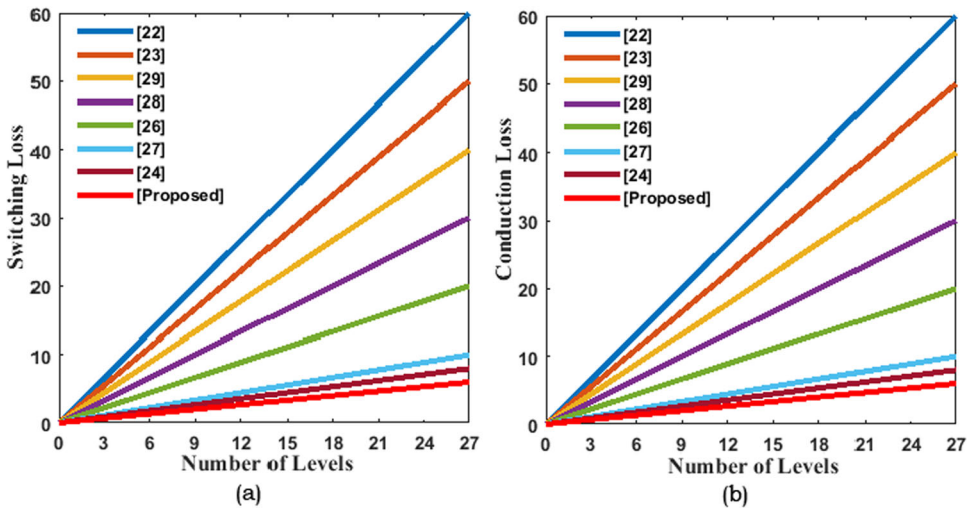


Fig. 5 **a** Switching loss, **b** Conduction loss

By applying KVL to the circuit:

$$V_L = R_{switch}\, i_L(t) + R_o i_L(t) + L\frac{di_L(t)}{dt} \tag{5}$$

where, $R_0 = R_e + R_{inductor}$, and R_e, $R_{inductor}$, R_{switch}, and L are the total load resistance, internal resistance of inductor, Resistance of all conducting IGBTs in the ON state and load inductance in mH at each level. In this RMC the total conducting component in each level is same therefore in equation (15) substitute the value of VL from equation (14).

$$L\frac{di_L(t)}{dt} = -(R_{switch} + R_o)i_L(t) + \|1111\| \begin{bmatrix} \vartheta 1Hb \\ \vartheta 2Hb \\ \vartheta 3Hb \\ \vartheta 4Hb \end{bmatrix} \|V_{dc}\| \tag{6}$$

Assuming the state variable as $X = i_{L(t)}$ (current through the inductor) and the input variable $U = V_{dc}$

$$\frac{di_L(t)}{dt} = \frac{-(R_{switch} + R_0)i_L(t) + \|1111\| \begin{bmatrix} \vartheta 1Hb \\ \vartheta 2Hb \\ \theta 3Hb \\ \vartheta 4Hb \end{bmatrix} \|V_{dc}\|}{L} \tag{7}$$

where,

$$\dot{X} = \frac{di\,L(t)}{dt}(\text{StateDerivative}); \tag{8}$$

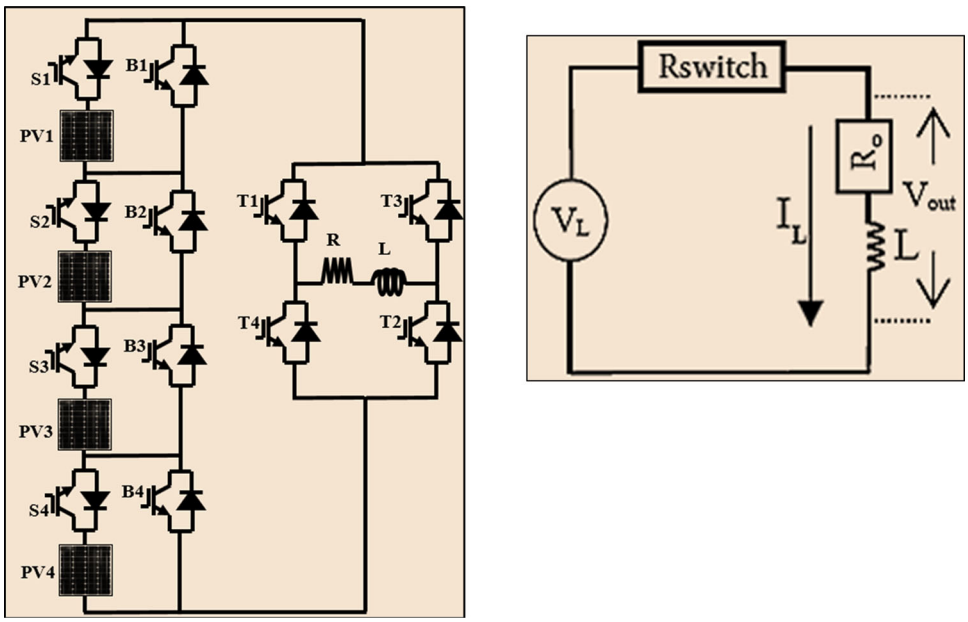


Fig. 6 **a** Basic structure of RMC, **b** Simplified RMC circuit for modelling

$A = -(R_{\text{Switch}} + R_O)$; B = [1111][$\vartheta$1Hb$\vartheta$2Hb$\vartheta$3Hb$\vartheta$4Hb]$^{\text{T}}$

The output voltage across the load

$$V_{\text{out}} = R_O i_L(t) + L\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} \tag{9}$$

where $Y = V_{\text{out}}$; $C = \left(R_0 + L\frac{\mathrm{d}i_L(t)}{\mathrm{d}t}\right)$

Therefore, the generalized (State space & Output) equation for proposed topology is given by:

$$\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \frac{-(R_{\text{switch}} + R_0)i_L(t) + [\vartheta 1\text{Hb}\ \vartheta 2\text{Hb}\ \vartheta 3\text{Hb}\ \vartheta 4\text{Hb}]^T[\text{V}_{\text{dc}}]}{L} \tag{10}$$

$$\text{V}_{\text{out}} = R_o i_L(t) + L\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} \tag{11}$$

where V_{dc} is the magnitude of each dc source fed from solar PV and $i_{\text{L}}(t)$ is the current through the inductor.

4 Modelling of solar PV module

Photo Voltaic system consist of.

- Photo voltaic modules
- Boost converter (DC/DC Converter).
- Maximum Power Point Tracking (MPPT) controller.

Solar PV cells are contained in Solar PV modules (SPV), which are connected in series. By interconnecting the PV segments in parallel and series, a solar PV array is created. The voltage–current (V–I) characteristics of individual solar cells vary. In order to simulate the MPPT boost converter, various elements are used, including the PV model.The major purpose of the PV model is to generate the Current–Voltage I–V characteristic curve of PV module. A reverse biased diode that is shunted across a resistor Rsh is used in the equivalent circuit of a solar panel, as shown in Fig. 7.

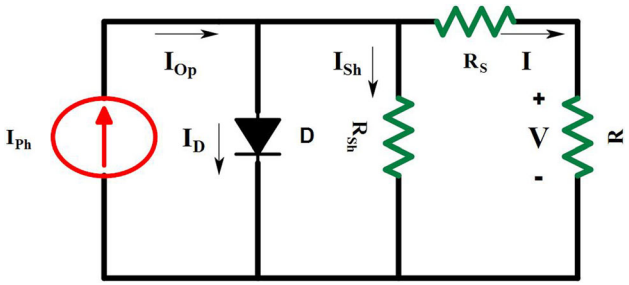


Fig. 7 Equivalent circuit of Solar PV Panel

4.1 Design of solar PV panel

Each solar cell has an open circuit voltage of 0.5 V and a short circuit current of 7 A. There are 24 solar cells in a single module. At typical test circumstances (1000 W/m^2 and 25 °C), these cells are wired in series to provide 12 V, 7A. A 24 V, 7 A solar PV array is created by connecting two single modules in series. [54, 55],. The fixed interconnection design is put into place, and the ratio of DC sources is kept at 1: 2: 3: 7. The designed inverter produces 27 levels of output voltage from four DC sources.

$$\begin{aligned}\text{V}_{\text{peak}} &= 24\text{V} + 48\text{V} + 72\text{V} + 168\text{V} \\ &= 312\text{V}\end{aligned}$$

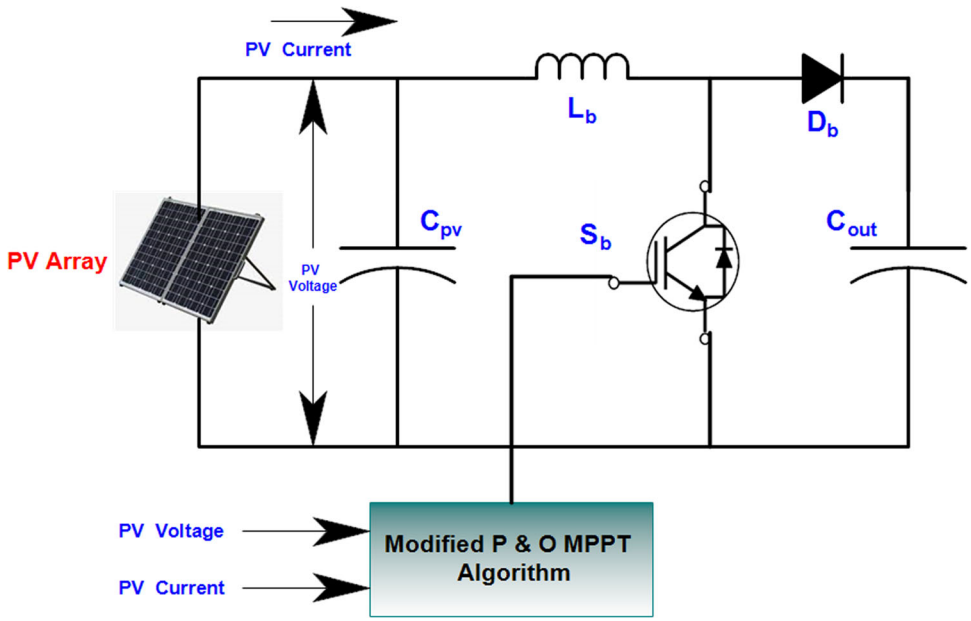


Fig. 8 Circuit Diagram of DC–DC converter

4.2 DC–DC (BOOST) converter with MPPT control

To deal with the issue of the PV module being partially shaded, DC-DC converters are used. The Converter used in the proposed system is a boost converter. [48, 49]. A boost converter is a most efficient type of converter module that has been incorporated into this system. The boost converter is essentially a DC–DC converter that generates an output voltage that is higher than the input voltage.

As shown in Fig. 8, where the inducer, diode, capacitor and switches are the components of the boost converter which provides there required voltage level with the MPPT controller, the MPPT technique provides the extracted voltage and current from the PV source to the boost converter.

4.2.1 Maximum power point tracking (MPPT) method

To achieve 27 Levels, the proposed inverter uses various DC Sources. So, a discrete boost converter integrated with MPPT is used to obtain the desired output voltage [48, 49],. The power output by PV panels can be increased by using the MPPT method as shown Fig. 9 which employs an Adaptive modified perturb and observe algorithm [59]

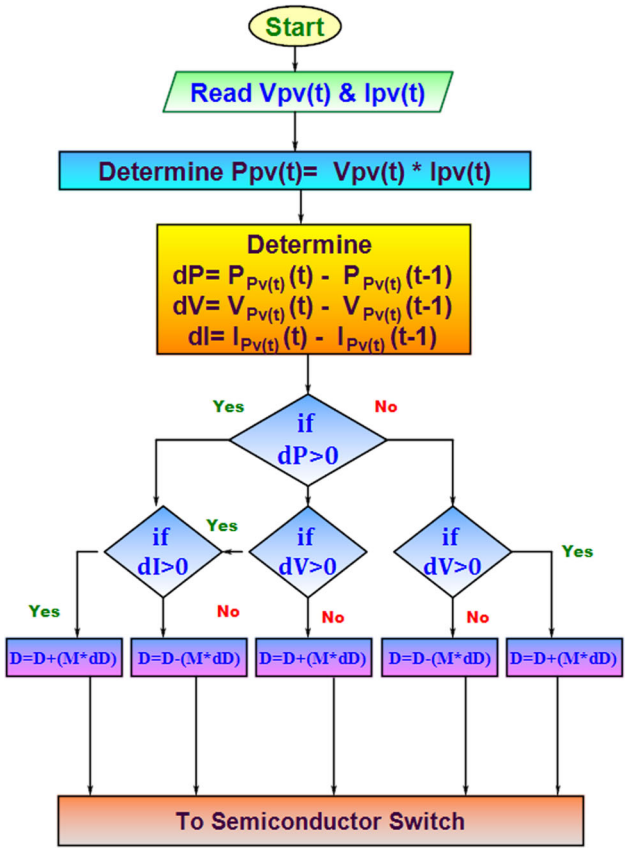


Fig. 9 Flow chart of Adaptive modified P & O Method

5 Theory on selective harmonic elimination (SHE)

Among the various modulation techniques (Sinusoidal PWM, Multi-Carrier PWM, SHE PWM & Space-Vector PWM) the most efficient way to eliminate specific lower order harmonics is done by SHE-PWM[55],.It is derived from the Fourier transform, which contains a variety of triggering states over its complete cycle. These degrees of freedom can be calculated to verify that it is possible to

Table 6 Switching angles of the proposed system for different inverter levels (Mi = 0.95)

Levels	9	11	13	15	17	19	21	23	25	27	29	31
Switch angles												
β_1	5.30	3.13	3.54	3.27	2.91	3.82	1.12	2.34	1.62	1.25	1.79	0.72
β_2	11.80	8.89	8.55	7.83	5.54	4.29	5.12	3.87	3.96	4.03	2.91	3.26
β_3	23.07	18.18	12.86	9.65	10.04	8.52	7.95	7.32	7.04	5.69	5.83	5.73
β_4	38.67	27.31	23.08	18.65	14.96	13.44	11.65	10.65	9.22	9.10	8.13	7.17
β_5		41.00	28.83	23.01	19.95	17.25	14.68	13.01	12.66	10.57	10.63	10.10
β_6			42.35	31.62	26.18	22.44	20.24	17.36	14.93	14.12	12.25	11.52
β_7				41.49	32.66	27.73	23.69	21.13	18.97	16.94	16.19	14.78
β_8					42.39	34.28	28.88	25.34	22.67	20.62	17.74	16.13
β_9						43.20	35.12	30.01	26.76	23.54	22.30	20.03
β_{10}							43.50	35.80	31.71	27.83	24.22	22.58
β_{11}								43.10	36.55	31.72	28.74	25.93
β_{12}									43.46	36.94	32.26	29.26
β_{13}										43.53	37.44	33.05
β_{14}											43.41	37.73
β_{15}												43.18

generate a fundamental voltage component without (S-1) harmonics. By developing a set of equations to indicate when the triggering of switches should occur, these degrees of freedom are employed. In this work it is mainly focused to cancel the odd order harmonics.

In order to lower the 'S ang-1' harmonics for an N-level inverter, 'S ang' triggering angles must be determined. Therefore, in order to get the triggering angles for the 27-level RMC, the following Equation must be utilized.

$$S_{\text{ang}} = \frac{27-1}{2} = 13 \tag{12}$$

The switching angles must adhere to the following requirements:

$$\beta_1 < \beta_2 < \beta_3 < \ldots \beta_{13} < \prod/2$$

Equations below presents the nonlinear equations required to obtain the triggering angles.

$$B_1 = \frac{4\mathrm{V_{PV}}}{1\pi}[\cos\beta_1 + \cos\beta_2 + \ldots + \cos\beta_{13}] \tag{13}$$

$$B_5 = \frac{4\mathrm{V_{PV}}}{5\pi}[\cos 5\beta_1 + \cos 5\beta_2 + \ldots + \cos 5\beta_{13}] \tag{14}$$

$$B_7 = \frac{4\mathrm{V_{PV}}}{7\pi}[\cos 7\beta_1 + \cos 7\beta_2 + \ldots + \cos 7\beta_{13}] \tag{15}$$

$$B_{11} = \frac{4\mathrm{V_{PV}}}{11\pi}[\cos 11\beta_1 + \cos 11\beta_2 + \ldots + \cos 11\beta_{13}] \tag{16}$$

$$B_{13} = \frac{4V_{PV}}{13\pi}[\cos 13\beta_1 + \cos 13\beta_2 + \ldots + \cos 13\beta_{13}] \tag{17}$$

$$B_{17} = \frac{4\mathrm{V_{PV}}}{17\pi}[\cos 17\beta_1 + \cos 17\beta_2 + \ldots + \cos 17\beta_{13}], \tag{18}$$

$$B_{19} = \frac{4\mathrm{V_{PV}}}{19\pi}[\cos 19\beta_1 + \cos 19\beta_2 + \ldots + \cos 19\beta_{13}], \tag{19}$$

$$B_{23} = \frac{4\mathrm{V_{PV}}}{23\pi}[\cos 23\beta_1 + \cos 23\beta_2 + \ldots + \cos 23\beta_{13}] \tag{20}$$

$$B_{25} = \frac{4\mathrm{V_{PV}}}{25\pi}[\cos 25\beta_1 + \cos 25\beta_2 + \ldots + \cos 25\beta_{13}], \tag{21}$$

$$B_{29} = \frac{4\mathrm{V_{PV}}}{29\pi}[\cos 29\beta_1 + \cos 29\beta_2 + \ldots + \cos 29\beta_{13}], \tag{22}$$

$$B_{31} = \frac{4\mathrm{V_{PV}}}{31\pi}[\cos 31\beta_1 + \cos 31\beta_2 + \ldots + \cos 31\beta_{13}] \tag{23}$$

$$B_{35} = \frac{4\mathrm{V_{PV}}}{35\pi}[\cos 35\beta_1 + \cos 35\beta_2 + \ldots + \cos 35\beta_{13}], \tag{24}$$

$$B_{37} = \frac{4\mathrm{V_{PV}}}{37\pi}[\cos 37\beta_1 + \cos 37\beta_2 + \ldots + \cos 37\beta_{13}] \tag{25}$$

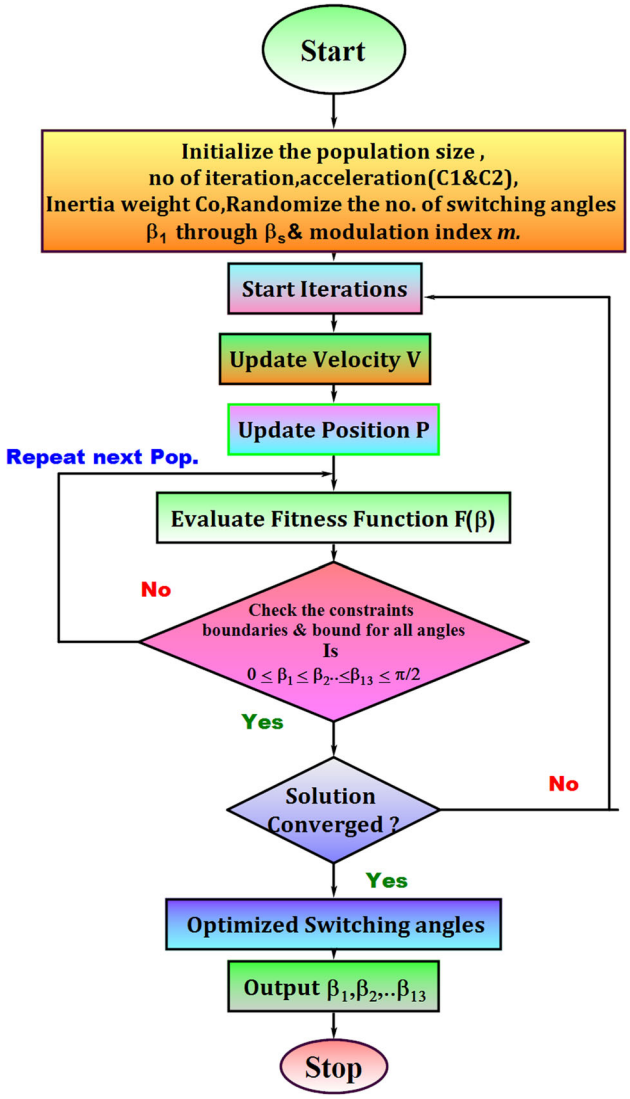


Fig. 10 Flow chart of PSO Algorithm for calculating Switching angles

The resultant equations, however, must be solved using quantitative tools because they are nonlinear and transcendental in nature. Due of limitations in computing the optimal switching angles mathematically, optimization techniques like Newton Rampson (NR), Particle Swarm Optimization (PSO) and Genetic Algorithm (GA) are employed to compute the triggering angles. The PSO approach is superior among other methods [59]. in terms of switching angles prediction accuracy, fundamental output voltage generation and total harmonic distortion reduction in the case of different level CHB inverters. So, in this research work, the switching angles determined for the asymmetric 27-level RMC using the PSO approach is shown in Fig. 10.

By solving the preceding equations, we obtain 13 triggering angles from that the harmonics of orders 5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, and 34 are cancels each other. The SHE

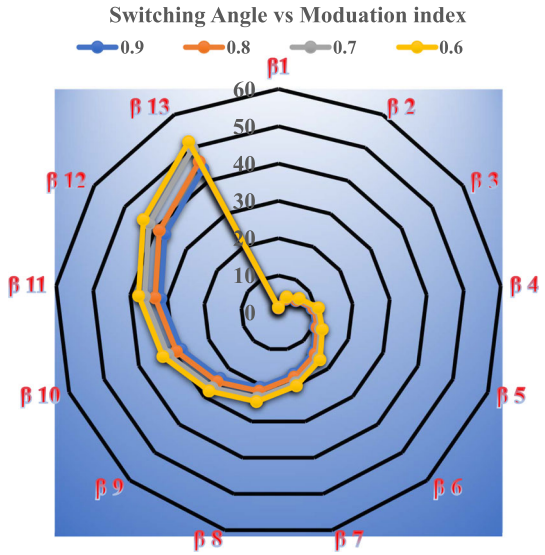


Fig. 11 Modulation Index Vs Switching Angles for 27-Level RMC

approach was applied for the 27-level RMC.For RMC with Mi = 0.95, the corresponding switching angles are listed in Table 6 which is shown in Fig. 11.

6 Reactive power compensation in power system

Generally Reactive power can be compensated using solar power systems as per the IEEE1547a standard (Fig. 12). The designed controller injects reactive power into the photovoltaic inverter and smooths its apparent power transition. To reduce voltage, drop, reactive power is fed into the distribution line, when real power drops unexpectedly. However, frequent reactive power from the PV fed inverter generates reactive current, which increases power system losses. When the PV system's power reaches the proportional gain Kp maximum, the slope of the apparent power of inverter (Sin *v*) is fixed with a constant integral gain Ks value.

The MPPT controller receives PV panel voltage and current. The proposed system tracks solar panel power using the Adaptive Improved P and O method [58]. Cascaded control loops use the MPP block output signal as a voltage reference. A PLL determines grid phase and angle. The PI controller detects the DC error. The PLL angle and PI controller current signal form the reference active current component, i_a^{ref}. Q produces reactive current, i_a^{ref}. The inner current controller of the cascaded control system tracks the sum of the actual and reactive current references The PI controller receives the error from the inverter current and the reference currents ($i_a^{ref} + i_r^{ref}$). The SHE block receives the output from PI. The proposed inverter's switches are triggered by pulses from the SHE block, compensating reactive power.

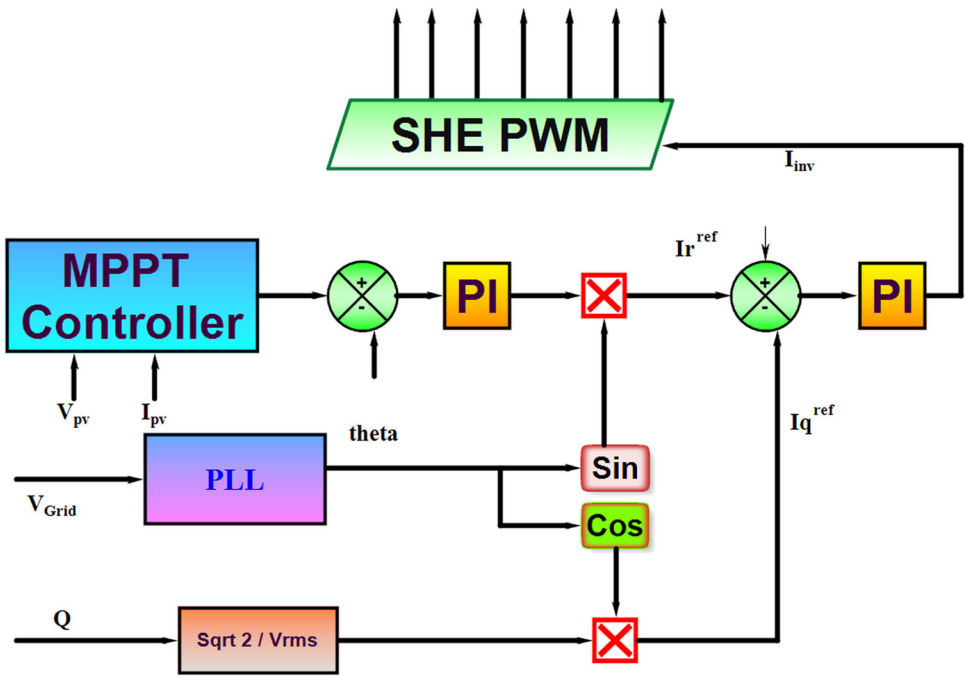


Fig. 12 Reactive Power Compensation Method

The reactive power Q can be calculated by performing the steps.

Step 1: Sense the Grid voltage and Inverter current.

Step 2: Determine the active power, the active power's rate of change over time, and the apparent power.

Step 3: After determining $\frac{dP_{inv}}{dt}$ value, equate the obtained $\frac{dP_{inv}}{dt}$ value with the proportional gain $(-K_p)$.This stage decides the amount of reactive power needed for compensation by the proposed inverter.

Step 4: This stage helps to determine, At this point, we determine how much reactive power the proposed inverter needs to compensate for.

$$\text{If} \frac{dP_{inv}}{dt} < -K_p; \text{ than } \frac{dS_{inv}}{dt} \text{is fixed to} -K_s$$

$$\text{If } \frac{dP_{inv}}{dt} \not< -K_p; \text{ then check}$$

$$\text{If } S_{inv} > P_{inv} \text{ than; } \frac{dS_{inv}}{dt} \text{ is fixed to } -K_s$$

$$\text{If } S_{inv} \not> P_{inv}; \text{ than } \frac{dS_{inv}}{dt} = \frac{dP_{inv}}{dt} \text{ no reactive power injection}$$

Step 5: The apparent power S_{inv} is updated by using $\frac{dS_{inv}}{dt}$.The updated S_{inv} and the P_{inv} values are used to determine reactive power (Q). From this Q value, the reactive reference current is achieved. The Q value is updated from time to time to successfully fix the reactive power compensation (Fig. 13).

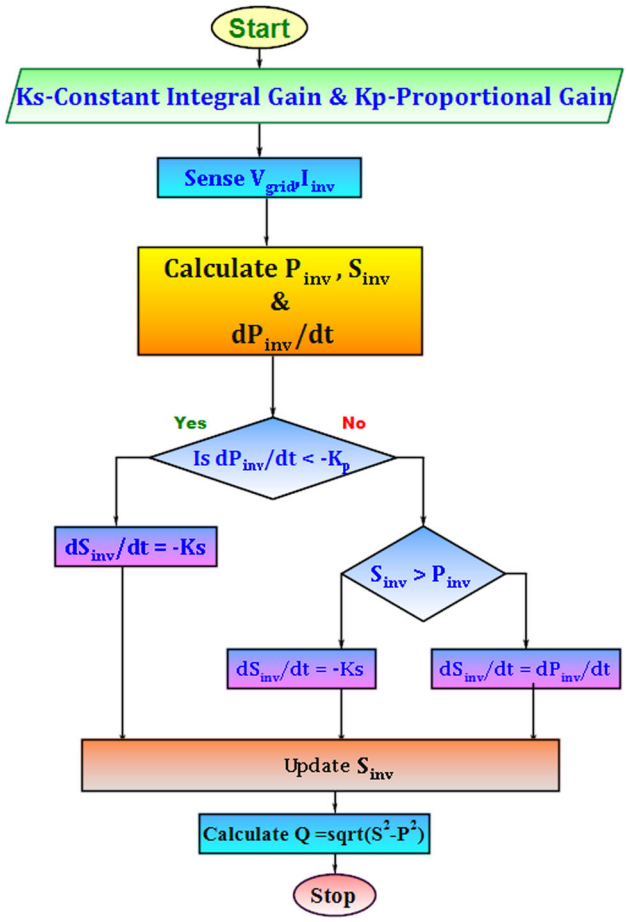


Fig. 13 Flow chart to determine reactive power Q

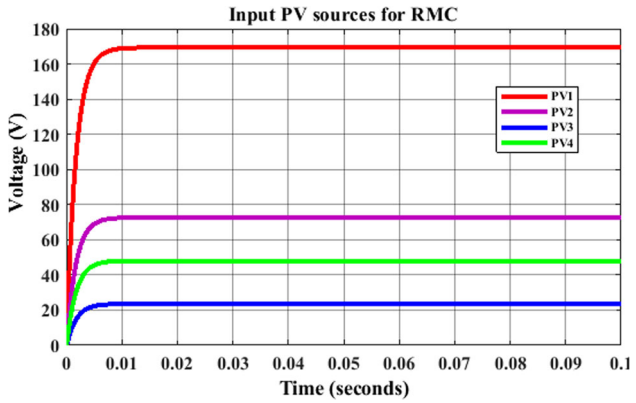


Fig. 14 Solar input to the RMC

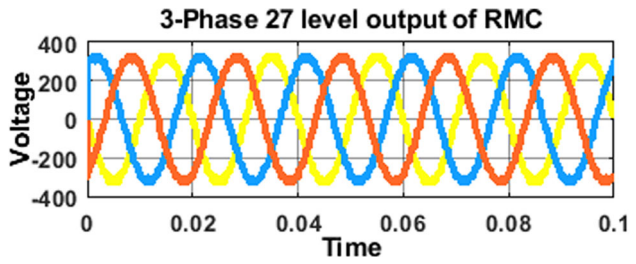


Fig. 15 27-level output of RMC

7 Cost calculation

The total cost of the RMC depends on the voltage and current rating of the switches. It also depends on the voltage blocking capacity of switces if it doubles it cost of RMC will be more.The cost of RMC depends on the number of IGBT's, number of driver circuits, number of different DC sources and standing voltage rating of switches.The quantity of IGBTs N_{IGBT}, the quantity of driver circuits (N_{driver}), the variety of DC sources ($Nd_{iff\ DC}$), and the standing voltage rating of the switches (V_{TSV}) all affect the price of RMC.

$$\text{RMC cost} = N_{IGBT} + N_{driver} + Nd_{iff\ DC} + \zeta V_{TSV} \quad (26)$$

The weight coefficient of total standing voltage on switches is ζ which is inverse to total power switches. Greater total standing voltage requires higher ζ. The proposed RMC uses fewer N_{IGBT}, N_{driver}, and lesser V_{TSV} than the conventional configuration.

8 Results and discussion

8.1 Simulation results

Utilizing MATLAB/Simulink, the proposed PV fed RMC is simulated. A Diode rectifier in combination with R- L Load is used as Non-Linear Load. The simulation results is obtained for the duration 0.01–0.2 s for the proposed shunt active filter. To achieve a steady, constant DC voltage A series connection is made among 2,4,6,14 batteries of 12 V range. This RMC generates a peak voltage of 312 V. The DC inputs of 24 V, 48 V, 72 V and 168 V as in Fig. 14 The switching angles produced using PSO techniques are stored in the lookup table for switching sequences generation. The output waveform of the 27-level RMC is shown in Figs. 15 and 16 along with an analysis using the Fast Fourier Transform (FFT). The system's measured Total Harmonic Distortion (THD), which is

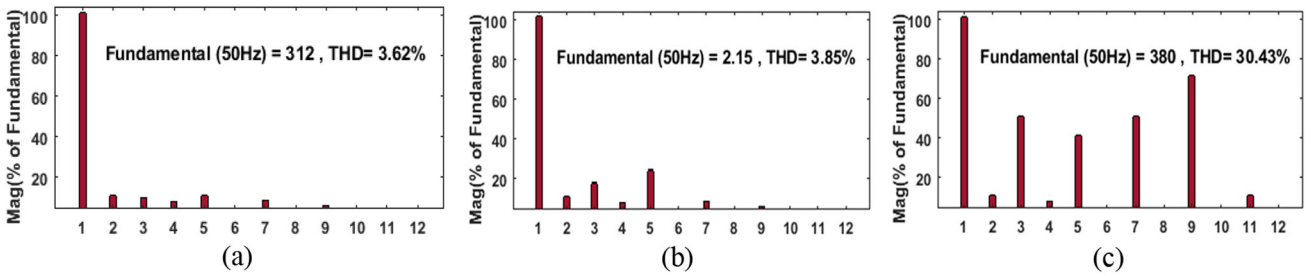


Fig. 16 **a** 27-level output of RMC, **a** Voltage THD, **b** Current THD, **c** Voltage THD without APF

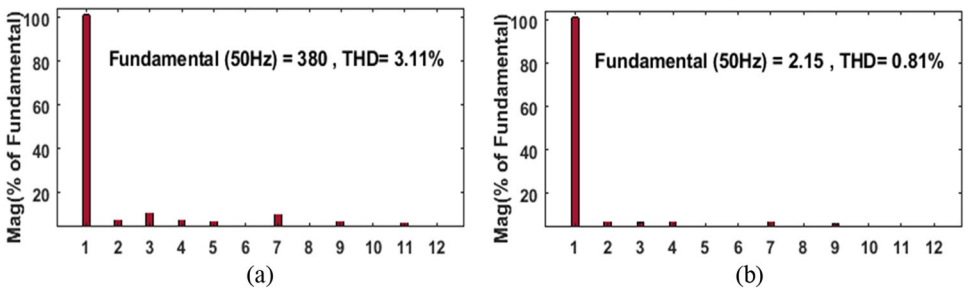


Fig. 17 FFT analysis of **a** Voltage THD with SAPF, **b** Current THD with SAPF

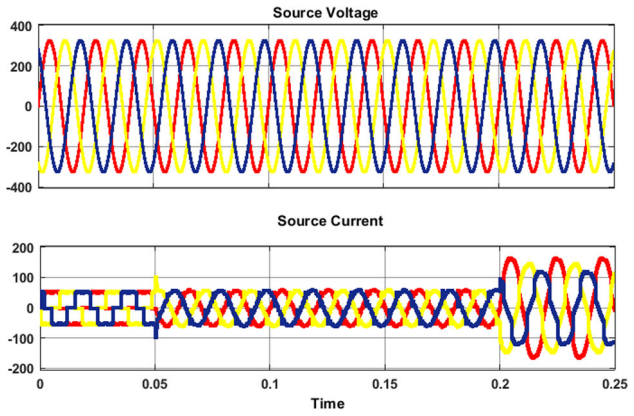


Fig. 18 Source Voltage and Source Current

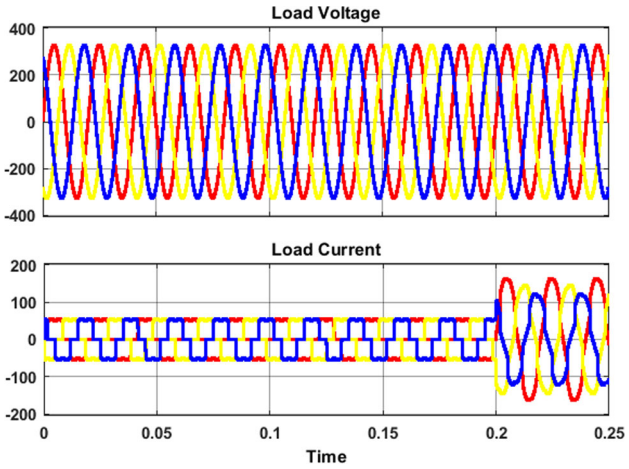


Fig. 19 Load Voltage and Load Current

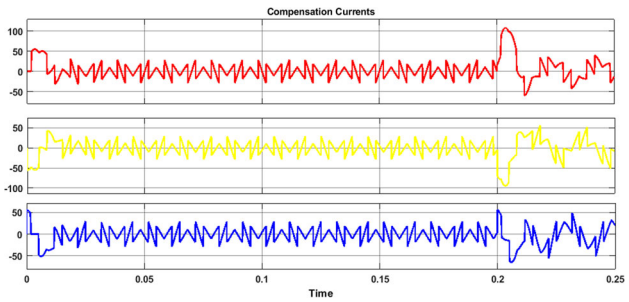


Fig. 20 Compensation currents of each phase

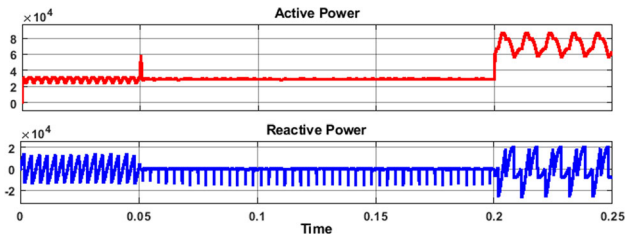


Fig. 21 Active Power & Reactive Power

does not include RMC-based APF, is shown in Fig. 16. The proposed active power filter is changed from 0.05 to 0.2 s in order to acquire the simulation results in the simulation model. Figure 16 displays the measured THD of the RMC-based APF.The measured voltage THD value for $0 \leq t \leq 0.05$ s in Fig. 16c is non-sinusoidal in character and has a measured THD value of 30.43%.(not including APF). The measured voltage THD value drops to 3.11% when the APF is turned on for $0.05 \leq t \leq 0.2$ s, and the current THD value is obtained as 0.81%, which is within IEEE -519 standards and suggests the waveform obtained is sinusoidal in nature. The measured current and voltage THDs after compensation are shown in Fig. 16a, b. After compensation, there is some short-term fluctuation in the source voltage, which has a harmonics of 3.11% The system's source voltage and source current are shown in Fig. 17. The system's load voltage and load current are shown in Fig. 18. The source current is initially not sinusoidal due to the nonlinear load, as shown in the Fig. 16 However, after the SAPF is switched from 0.05 to 0.2 s, it is discovered that the source current more closely resembles a sinusoidal waveform. When nonlinear loads are used in the load side of the SAPF, the RMC generates compensation currents that act as right angles to the harmonic currents generated by those nonlinear loads. Harmonic currents and compensation currents cancel each other at the Point of Common Coupling (PCC), which frees from the source current harmonics (Figs. 19, 20 and 21).

8.2 Experimental validation

The prototype of the proposed RMC-based SAPF is developed. The developed prototype's is shown in Fig. 22. Each leg of the voltage source inverter consists of 12 switches FGA25N120 with a gate driver HCPL316J running at a switching frequency of 1 kHz to test the performance of the proposed system. To reduce current harmonics and balance reactive power, coupled inductors (1.9mh) are connected in series with the RMC (Fig. 23). As the load, a diode rectifier is used in. The Components list with their respective rating are shown in Table 7. The voltage and current sensors connected to the Controller board's analogue to digital converters generate the reference currents for the SAPF. Harmonics are introduced into the system through the introduction of a nonlinear load on the DC side. The Solar PV Systems parameters for hardware design are shown in Table 8. The hardware output of the 27-level RMC is shown in Fig. 24. The hardware output of the three phases' source voltage is shown in Fig. 22. The compensating currents generated by the RMC-based SAPF to reduce the current harmonics in the source side are shown in Fig. 23. The hardware output of the load

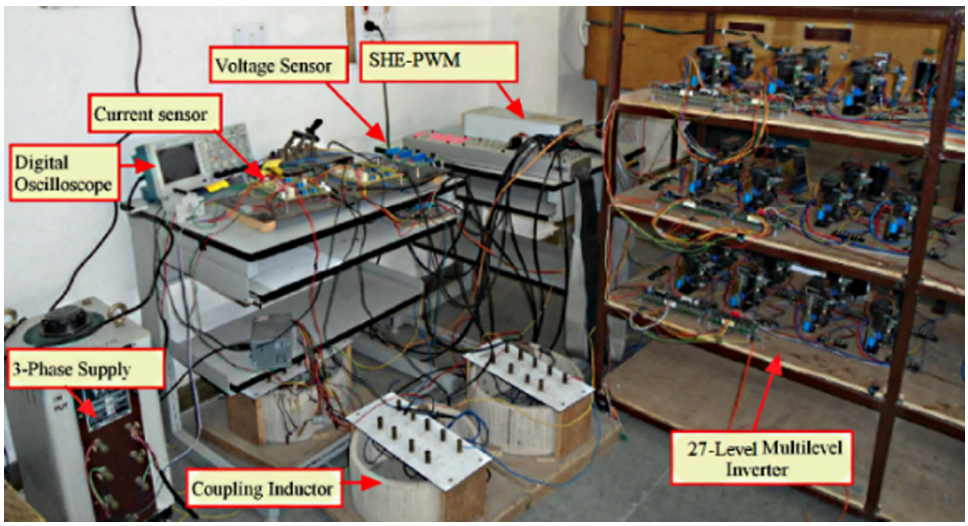


Fig. 22 Prototype of the Proposed system

Fig. 23 Solar Plant of rating 3kWp

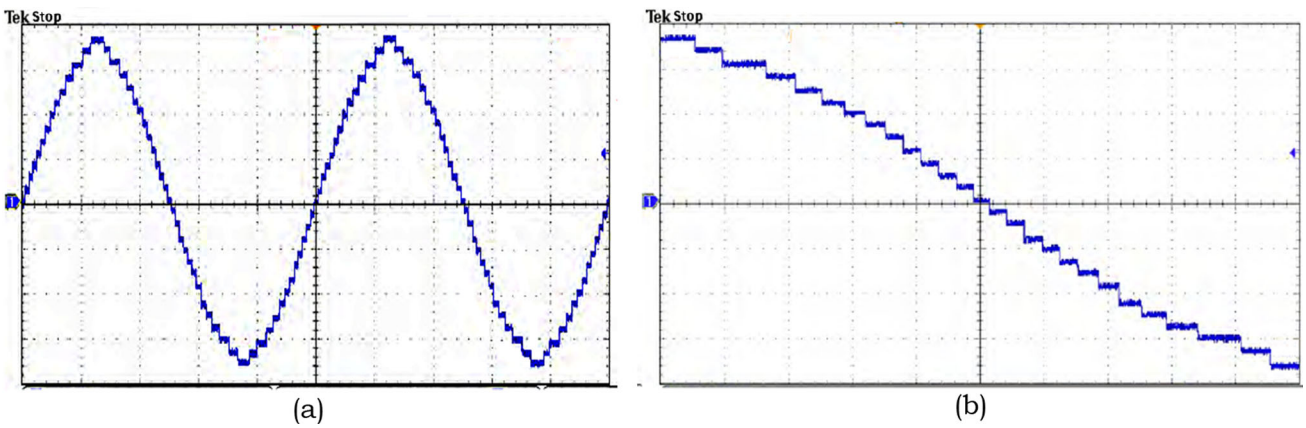


Fig. 24 **a** 27-level Output of RMC, **b** Magnified view of 27-levels

Table 7 Components list with their respective rating

Components Name	Ratings
Battery (solar tubular)	Exide 6LMS150L
Battery Rating	12 V,150AH
Number of batteries	28
RMC IGBT Switches	FGA25N120 (12)
Ultra-fast diode	MUR1560
Opto isolators	TLP250
IGBT Drivers	HCPL316J
Processor Board	ATMEGA-16AVR
Snubber circuit	1000 V,10W,10Ω,0.01μF
Power Quality Analyzer	Fluke
Fundamental supply voltage	380 V
Supply frequency	50 Hz
Switching frequency	1 kHz
Coupled inductors	2nos (1.9mh)
Three-phase diode rectifier-Non linear Load	$L = 50$mh,100 mH, and $R =$ 50Ω,100Ω load

Table 8 Solar PV Systems Parameters

System characteristics	
Panel Model	Sun power SPR-X20-250-BLK
Maximum power	3220Wp
Open circuit voltage Voc	24.6 V
Short circuit current Isc	7.2A
Number of panels	28
Vpm,Ipm	16.5 V,6.9A
Maximum system voltage	312 V
Tolerance rate @ peak power	± 5%

current is shown in Fig. 24. The hardware output of the source current is shown in Figs. 25 and 26. Due to the injection of compensating currents at PCC, it can be shown in Figs. 27 and 28 that the source current has a sinusoidal nature.

The active and reactive power of the system are represented in Fig. 21. The proposed PV fed RMC-based APF corrects the source side's power factor almost to unity by injecting harmonic currents. Only active power is provided from the source side, as can be shown in Fig. 21. The figure also shows that source-side reactive power delivered is almost negligible, resulting in a power factor of unity there. As a result, the RMC-based APF injects harmonic currents that are similar in size but in phase opposition at PCC to make the distorted source current approximately sinusoidal. Consequently, the proposed technology improves the quality of the power.

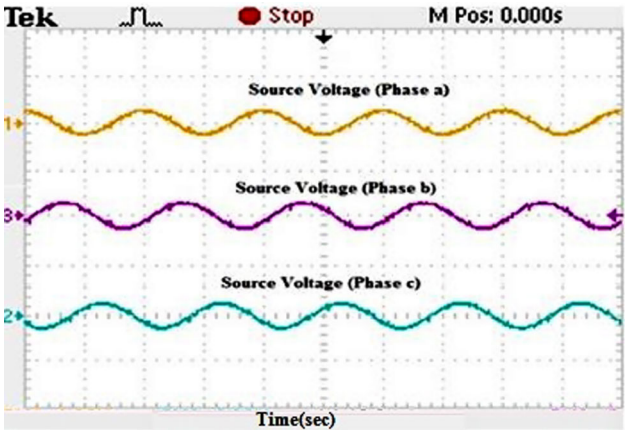


Fig. 25 Experimental output source Voltage

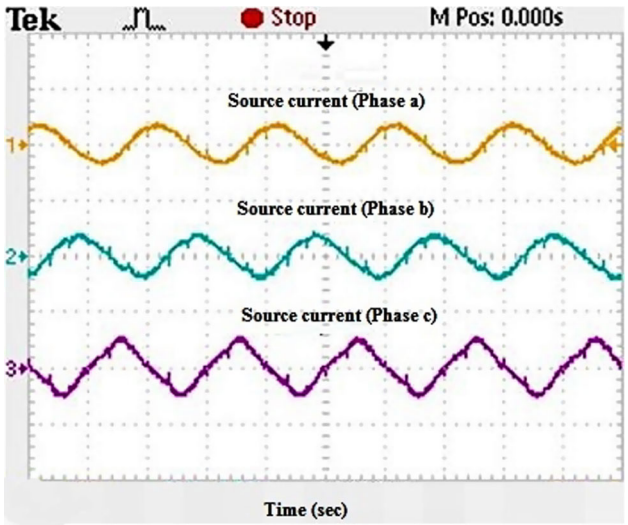


Fig. 26 Experimental output source Current

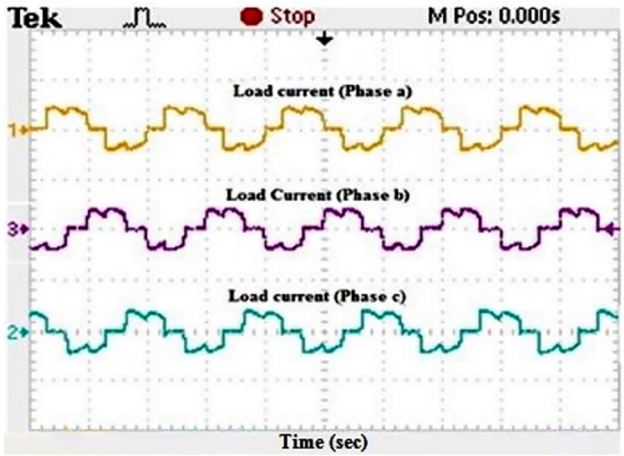


Fig. 27 Experimental output Load Current

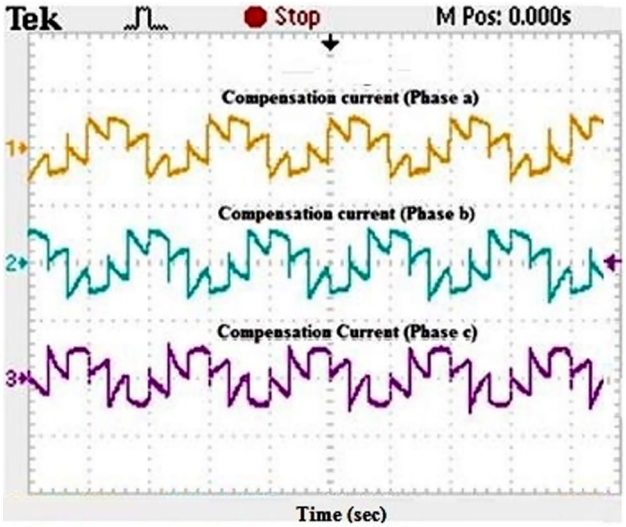


Fig. 28 Experimental output Compensation Currents

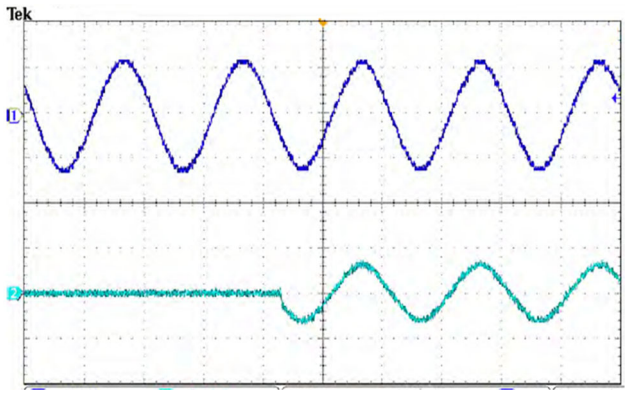


Fig.29 Experimental output voltage & output current when the R load is switched from 0 to 100Ω

Figure 29 presents the change in output current when the resistive load is switched from 0 to 100 Ω. Figure 27 illustrates the change of output current when the RL load is changed from 50Ω + 100mh to 50Ω + 50mh (Fig. 30).

Figure 31 illustrates the switching reaction of the system with and without SAPF. From Fig. 26, it is clearly seen that the source current before switching on the ASAPF is non-sinusoidal in nature and after switching exhibits there is a sinusoidal current wave of the injection of the compensation current.

As a result, RMC topology improves power quality. The frequency spectrum of the proposed topology is acquired using a power quality analyzer and is shown in Fig. 32. The proposed topology, when used with SAPF, produces measured current THD of 2.33% and measured voltage THD

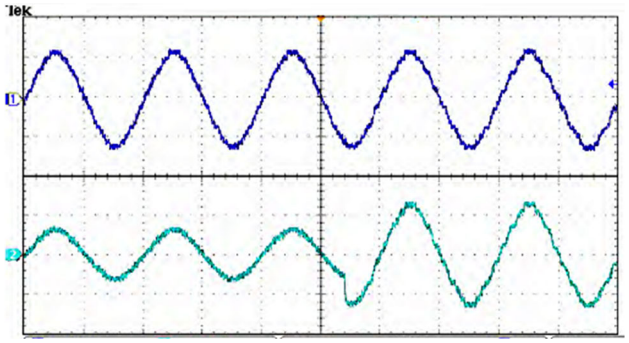


Fig.30 Experimental output voltage and output current when the RL load is changed from 50Ω + 100mh to 50Ω + 50mh

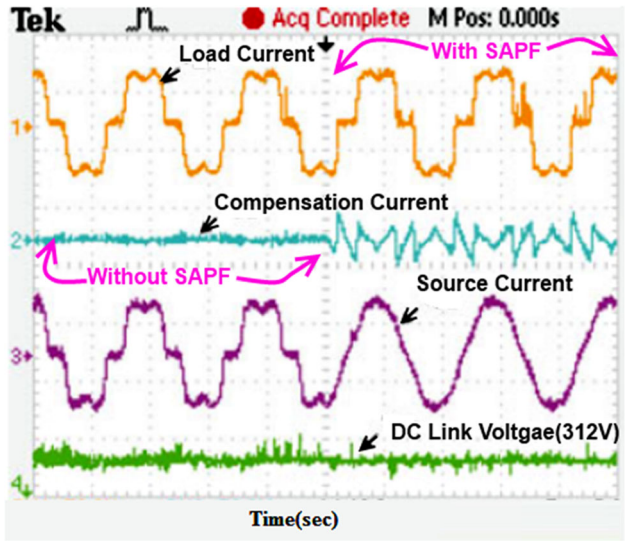


Fig. 31 Switching reaction of RMC based SAPF

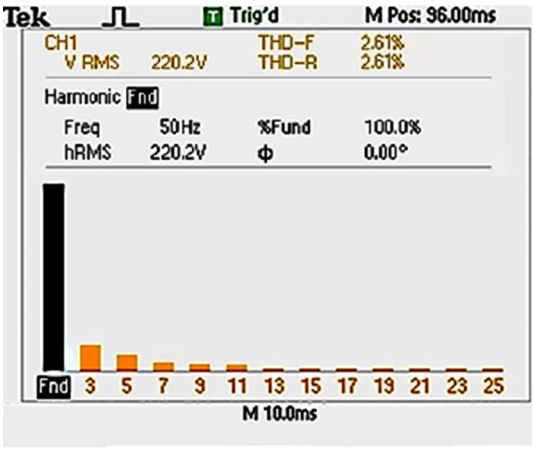
of 2.61%, as can be shown in Fig. 32. The permitted IEEE standard limitations are not exceeded by this measured THD %. It has been demonstrated through simulation and experimentation that the suggested RMC decreases THD, raises voltage levels with fewer components, and compensates reactive power (Fig. 33).

9 Comparative analysis

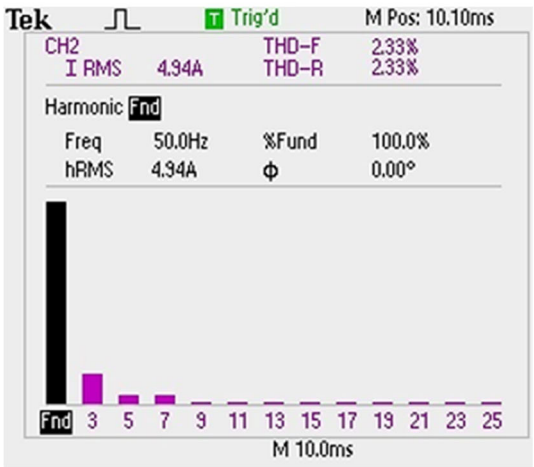
Table 9 shows the comparison of the proposed work with other existing work, From the table, it is clear that the proposed 27 Level Multilevel inverter topology reduce the THD by 2.61 which is lower than 5%,satisfying the standard of IEEE519.

Table 9 Comparison of the Proposed work with other existing work

S. No	References	Methodology	Levels	THD%
1	[37]	NLC	27	5.45
2	[1]	PID	27	4.53
3	[10]	IPD	27	4.23
4	[31]	NLM	27	3.45
5	[11]	PID	27	3.4
6	[13]	–	27	3.22
7	[33]	PID	27	3
8	[32]	–	27	2.97
9	[9]	PI	27	2.74
10	[57]	–	27	2.65
11	Proposed Topology	PSO-PI	27	2.61



(a)



(b)

Fig. 32 Voltage & Current THD of the proposed system

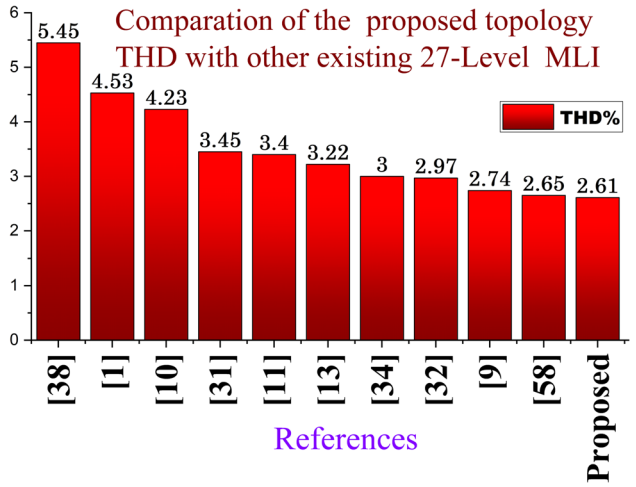


Fig. 33 Comparative Analysis of the Proposed system THD with other 27-Level Asymmetric MLI

10 Conclusions

In this research paper, Novel multilevel connections have been Modelled & Developed, when compared with conventional topologies it is more superior in terms of number of components, number of levels, simple switching pattern, reduction in total losses with improved efficiency.Interms of switch count, proposed topology uses only 12 IGBT's & only 4 DC sources with various configuration for achieving 27-Levels.And switch stress is reduced to nearly 50% which leads to the improvement of efficiency. Modelling of PV Panels is carried out with integrated Step-up Converter(Boost converter) which uses Adaptive Modified P&O (MPPT) method for voltage regulation. In terms of harmonic mitigation, the SHE method is implemented with Particle swam optimization technique for the generation of 13 switching angles apart for this, the cost calculation is also done for the proposed method. Simulation analysis is carried out with the help of MATLAB-SIMULINK (R2020A) which proves that the total harmonic distortion is reduced to 3.62% for voltage and 3.85% for current. The Proposed RMC is experimentally investigated & Votlage THD is around 3.11% & Current THD is around 0.81% which is less as per IEEE 519 standard. Further, the developed inverter acts as shunt active

filter is for reactive power compensation in power system application.Finally, this paper is concluded with the comparative analysis with other recent work.

Author contributions Each author participated actively in conducting analyses, drafting sections of the manuscript, editing and approving the final, submitted version. None of the authors has a financial or other conflict of interest.

Funding No government, private, or non-profit organization provided direct funding for this research.

Declarations

Conflict of interest The authors declared no potential conflict of interest.

References

1. Ullah M, Shah SW, Ali F (2022) Multilevel inverter topology having reduced number of input DC sources and switches. Int J Eng Works 9(03):89–99
2. Babaei E, Kangarlu MF, Mazgar FN (2012) Symmetric and asymmetric multilevel inverter topologies with reduced switching devices. Electr Power Syst Res 86:122–130
3. Babaei E, Laali S, Bayat Z (2015) A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. IEEE Trans Ind Electron 62(2):922–929
4. Harbi IA, Azazi HZ, Lashine AE, Elsabbe AE (2018) A higher levels multilevel inverter with reduced number of switches. Int J Electron 105(8):1286–1299
5. Alishah RS, Hosseini SH, Babaei E, Sabahi M, Gharehpetian GB (2016). New high step- up multilevel converter topology with self-voltage balancing ability and its optimization analysis. 1–11
6. Gautam SP, Kumar L, Gupta S (2018) Single-phase multilevel inverter topologies with self-voltage balancing capabilities. IET Power Electron 11(5):844–855
7. Arif MSB, Sarwer Z, Siddique MD, Ayob SM, Iqbal A, Mekhilef S (2021). Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. Int J Circ Theor Appl. 1–19.
8. Varsha S (2013).New topology with re- duced number of switches in asymmetrical cascaded mul- tilevel inverter. In Fifth International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2013)
9. Arunima S, Bindu S, Unni KP (2020) A flyback converter based asymmetrical cascaded h-bridge 27 level grid connected inverter from a single source using FPGA. In: 2020 International Conference for Emerging Technology, INCET 2020, 1–6
10. Periyaazhagar D, Irusapparajan G (2019) Design and completion of asymmetric single phase 27 level cascaded mli for various pwm scheme. Int J Innov Technol Explor Eng 8(6):792–797
11. Muñoz J, Gaisse P, Baier C, Rivera M, Gregor R, Zanchetta P (2016). Asymmetric multilevel topology for photovoltaic energy injection to microgrids. In: 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics, COMPEL 2016.
12. Monicka JG (2016) A modified topology for three phase asymmetric multilevel inverter. World Appl Sci J 34(10):1343–1350. https://doi.org/10.5829/idosi.wasj.2016.1343.1350
13. Vijayaraja L, Kumar SG, Rivera M (2021) An investigation and design of symmetric and asymmetric inverter for various applications. Electr Electron Dev Circuits Mater Technol Chall Solut. https://doi.org/10.1002/9781119755104.ch25
14. Shunmugham Vanaja D, Stonier AA (2020) A novel PV fed asymmetric multilevel inverter with reduced THD for a grid-connected system. Int Trans Electr Energy Syst 30(4):e12267
15. Vivek P, Muthuselvan NB (2021). Investigation on photovoltaic system based asymmetrical multilevel inverter for harmonic mitigation. In: Proceedings of the 7th International Conference on Electrical Energy Systems, ICEES 2021, 334–339
16. Azli NA, Choong YC (2006). Analysis on the perfomance of a three-phase cascaded h-bridge multilevel inverter. In: First International Power and Energy Conference.
17. Ajami A, Oskuee MRJ, Mokhberdoran A, van den Bossche, (2014) A developed cascaded multilevel inverter topology to minimise the number of circuit devices and voltage stresses of switches. IET Power Electron 7(2):459–466
18. Samanbaksh R, Ibanez FM, Koohi P, Martin F (2021) A new asymmetric cascaded multilevel converter topology with reduced voltage stress and number of switches. IEEE 9:92276
19. Hosseinpour M, Seifi A, Feyez E (2020) A new symmetric/asymmetric multilevel inverter based on cascaded connection of sub-multilevel units aiming less switching components and total blocked voltage. J Telecommun 12:53
20. Babaei E, Laali S, Alilu S (2014) Cascaded multilevel inverter with series connection of novel H-bridge basic units. IEEE Trans Industr Electron 61(12):6664–6671
21. Kangarlu MF, Babaei E (2012) A generalized cascaded multilevel inverter using series connection of submultilevel inverters. IEEE Trans Power Electron 28(2):625–636
22. Massoud AM, Finney SJ, Cruden AJ, Williams BW (2007) Three-phase, three-wire, five-level cascaded shunt active filter for power conditioning, using two different space vector modulation techniques. IEEE Trans Power Deliv 22(4):2349–2361
23. Ranjith Kumar G, Zhu GR, Lu J, Chen W, Li B (2017) Thermal analysis and reliability evaluation of cascaded H-bridge MLPVI for grid-connected applications. J Eng 2017(13):1595–1599
24. Sonti V, Jain S, Bhattacharya S (2017) Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter. IEEE Trans Power Electron 32(2):1156–1169
25. Uthirasamy R, Kumar Chinnaiyan V, Ragupathy US, Karpagam J (2018) Investigation on three-phase seven-level cascaded DC-link converter using carrier level shifted modulation schemes for solar PV system applications. IET Renew Power Gener 12(4):439–449
26. Villanueva E, Correa P, Rodriguez J, Pacas M (2009) Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems. IEEE Trans Ind Electron 56(11):4399–4406
27. Wu F, Li X, Feng F, Gooi HB (2015) Modified cascaded multilevel grid-connected inverter to enhance european efficiency and several extended topologies. IEEE Trans Ind Inf 11(6):1358–1365
28. Xiao B, Hang L, Mei J, Riley C, Tolbert LM, Ozpineci B (2015) Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications. IEEE Trans Ind Appl 51(2):1722–1731
29. Coppola M, Di Napoli F, Guerriero P, Iannuzzi D, Daliento S, Del Pizzo A (2016) An FPGA-based advanced control strategy of a GridTied PV CHB inverter. IEEE Trans Power Electron 31(1):806–816
30. Samanbakhsh R, Ibanez FM, Koohi P, Martin F (2021) A new asymmetric cascaded multilevel converter topology with reduced voltage stress and number of switches. IEEE Access 9:92276–92287

31. Nikouei B, Tan NML, Taghizadeh SF, Younis MAA, Tan NML, Taghizadeh SF, Design MAAY (2015) Design of a 27-level cascaded converter as FACTS device for voltage sag mitigation. Austr J Electr Electron Eng 12(3):232–241. https://doi.org/10.1080/1448837X.2015.1092994
32. Hasan MM, Abu-Siada A, Islam SM, Dahidah MSA (2018) A new cascaded multilevel inverter topology with galvanic isolation. IEEE Trans Ind Appl 54(4):3463–3472. https://doi.org/10.1109/TIA.2018.2818061
33. Aliaga R, Rojas D, Muñoz J, Villalón A (2020) 27 - Level asymmetric multilevel inverter for photovoltaic energy conversion. J Power Electron 20:904–915
34. Reddy AKVK, Narayana KVL (2020). Optimal total harmonic distortion minimization in multilevel inverter using improved whale optimization algoritham, 21(3).
35. Kumar DG, Ganesh A, Sireesha NV, Kshatri SS, Mishra S, Sharma NK, Bajaj M, Kotb H, Milyani AH, Azhari AA (2022) Performance analysis of an optimized asymmetric multilevel inverter on grid connected SPV system. Energies 15(20):1–25
36. Torres I, Muñoz J, Rojas D, Espinosa EE (2022) Selective harmonic elimination technique for a 27-level asymmetric multilevel converter. Energies 15(10):1–17
37. Raj MD, Thiyagarajan V, Selvan NBM, Vanaja DS (2022) Amelioration of power quality in a solar PV fed grid-connected system using optimization-based selective harmonic elimination. Electr Eng 104:2775
38. Deng E, Borucki L, Lutz J (2021) Correction of delay-time-induced maximum junction temperature offset during electrothermal characterization of IGBT devices. IEEE Trans Power Electron 36(3):2564–2573
39. Franquelo L, Rodriguez J, Leon J, Kouro S, Portillo R, Prats M (2008) The age of multilevel converters arrives. IEEE Ind Electron Mag 2(2):28–39
40. Gupta KK, Jain S (2013) Multilevel inverter topology based on series connected switched sources. IET Power Electron 6(1):164–174
41. Hoon Y, Radzi MAM, Hassan MK, Mailah NF (2018) Operation of three-level inverter-based shunt active power filter under non-ideal grid voltage conditions with dual fundamental component extraction. IEEE Trans Power Electron 33(9):7558–7570
42. Hu H, Shi Q, He Z, He J, Gao S (2015) Potential harmonic resonance impacts of PV inverter filters on distribution systems. IEEE Trans Sustain Energy 6(1):151–161
43. Jana J, Saha H, Das Bhattacharya K (2017) A review of inverter topologies for single-phase grid-connected photovoltaic systems. Renew Sustain Energy Rev 72:1256–1270
44. Nabae A, Takahashi I, Akagi H (1981) A new neutral point clamped PWM inverter. IEEE Trans Ind Electron 7(2):518–523
45. Najafi E, Yatim AHM (2012) Design and implementation of a new multilevel inverter topology. IEEE Trans Ind Electron 59(11):4148–4154
46. Selvaraj J, Rahim NA (2009) Multilevel inverter for grid-connected PV system employing digital PI controller. IEEE Trans Industr Electron 56(1):149–158
47. Jagabar Sathik MA, Abdel Aleem SHE, Kannan R, Zobaa AF (2017) A new switched DC-link capacitor-based multi-level converter (SDC2MLC). Electr Power Compon Syst 45(9):1001–1015
48. Shunmugham Vanaja D, Stonier AA (2021) Grid integration of modular multilevel inverter with improved performance parameters. Int Trans Electr Energy Syst 31(1):e12667
49. Shunmugham Vanaja D, Albert JR, Stonier AA (2021) An experimental investigation on solar PV fed modular STATCOM in WECS using intelligent controller. Int Trans Electr Energy Syst 31(5):e12845
50. Wu F, Sun B, Duan J, Zhao K (2015) Online variable topology-type photovoltaic grid-connected inverter. IEEE Trans Ind Electron 62(8):4814–4822
51. "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems - Amendment 1,"IEEE Std 1547a-2014 (Amendment to IEEE Std 1547–2003) , vol., no., pp.1–16, May 21 2014.
52. E. Troester, "New German Grid codes for connecting PV systems to the medium voltage power grid," 2nd International Workshop on Concentrating Phtovoltaic Power Plants : Optical Design, Production, Grid connection
53. Bihari SP, Sadhu PK (2020) Design analysis of high level inverter with EANFIS controller for grid connected PV system. Analog Integr Circ Sig Process 103(3):411–424
54. Vivek P, Vignesh V, Vigneshwaran T (2016). A novel approach on power quality improvement by multi-carrier multilevel inverter topology. In: 2016 3rd International Conference on Electrical Energy Systems, ICEES 2016, 13–17.
55. Vivek P, Ayshwarya R, Amali SJ, Sree ASN (2016). A novel approach on MPPT algorithm for solar panel using buck boost converter. In: 2016 International Conference on Energy Efficient Technologies for Sustainability, ICEETS 2016, 396–399.
56. Kannan C, Kishore CK (2014) A comparision of three phase 27 level inverter scheme under no load and multiple load conditions. Bull Electr Eng Inform 3(4):245–250. https://doi.org/10.11591/eei.v3i4.302
57. Roposed IIP, Opology BAT (2021). Novel switched-capacitor-based multilevel inverter topology for renewable energy. 5–9.
58. Manoharan P, Subramaniam U, Babu TS, Padmanaban S, Holm-Nielsen JB, Mitolo M, Ravichandran S (2021) Improved perturb and observation maximum power point tracking technique for solar photovoltaic power generation systems. IEEE Syst J 15(2):3024–3035. https://doi.org/10.1109/JSYST.2020.3003255
59. Marín-Reyes M, Aguayo-Alquicira J, De León-Aldaco SE (2020) Calculation of optimal switching angles for a multilevel inverter using NR, PSO and GA- a Comparison. Eur J Electr Eng 22(45):349–355. https://doi.org/10.18280/ejee.224-506