**ORIGINAL PAPER** 



# An energy-efficient CMOS interface circuit with maximum power point tracking and power management capabilities for self-powered sensor node applications using 50/60 Hz transmission line magnetic field harvesters

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#### Abstract

In this paper, an interface circuit for far-distance energy harvesting from magnetic field of overhead lines is presented. Due to the specific conditions of this type of energy harvesting, such as low available power, low induced voltage in the energy harvester coil, and change of energy harvester impedance, a direct AC/DC switching converter should be used. A maximum power point tracking solution is also necessary to guarantee impedance matching at different operation points. Since the harvested power is in the range of a hundred micro-watts, the power usage of the control circuitry is of significant importance and conventional design approaches based on microcontrollers and FPGAs which require ADCs, DACs and digital signal processing cannot be applied here. The proposed processing circuitry presented in this paper uses three feedback loops to perform the harvesting and energy transfer control. Only low-power comparators and basic digital gates are used as signal-processing elements to limit the power dissipation of the designed control blocks. The impedance matching inner loop samples the H-bridge voltage drop to extract the output load current and perform PWM impedance matching while transferring a rectified current to the output capacitor. Another inner feedback loop is used at the output capacitor using two-level comparison to regulate the output voltage. For maximum power point tracking an outer feedback loop samples the output voltage transfer rate and using a 50 Hz reference generator, adjusts the parameters of the impedance matching circuit of the first inner loop. With the proposed approach, in addition to converting the AC input power to a DC voltage, the output load is regulated at a fixed potential and using the MPPT control loop, the maximum power available from the coil is delivered to the output with relatively low dissipation. The proposed circuit is evaluated using a 0.18  $\mu$ m standard CMOS technology and operates as a self-powered circuit without an external power source. Based on the obtained results, the efficiency of the proposed circuit at 119  $\mu$ W input power is about 92.4%, and the MPPT efficiency is about 95%, which is suitable for low-power applications.

**Keywords** Magnetic field energy harvester · Impedance matching · Maximum power point tracking · Low power CMOS interface circuit · Self-powered sensors

## **1** Introduction

Today, intelligent sensors are used in a wide range of applications. One of the concerns in this field is the supply of a sustainable energy source with long life and small dimensions to power up the sensor. In recent years, the

Mehdi Habibi mhabibi@eng.ui.ac.ir use of different environment energy harvesting methods has received considerable attention [1–5]. Applications of self-powered low-power smart sensors include monitoring of weather conditions and the status of overhead power transmission lines [6–9]. Due to the importance of power transmission lines in the power grid, online and continuous monitoring of these lines and their ambient conditions such as temperature, humidity, and wind intensity allow optimal use of these lines [10]. The use of solar energy and magnetic fields around power transmission lines is among the options

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Fig. 1 Configuration of the proposed interface circuit, energy harvester coil, sensor and transmitter in a self-powered wireless sensor node



to supply power for this application. Due to the lack of sunlight during the night and in cloudy weather and the need for periodic cleaning of photovoltaic cells due to contaminations, the use of solar energy is limited. For magnetic field energy harvesting, conventional methods use a current transformer (a coil through which the transmission line passes) to transfer power to the electronic circuitry [11–14]. One of the problems with this method is the need to turn off the transmission line to access the conductor wire. Also, due to the high height of these lines from the ground, access and installation are challenging. Using an energy harvesting coil at a suitable distance from the overhead line is another solution that provides the power needed for intelligent sensors [15–18], as shown in Fig. 1.

Due to the low power level produced in this method, in addition to the need to design low power circuits, it is necessary to increase energy extraction efficiency using maximum power point tracking (MPPT). In some designs, instead of the MPPT approach, an energy management method is used in which the processing circuits are activated or deactivated based on the input energy level [19]. Such methods, in addition to having complicated and high power-consuming control circuits, will interrupt the actual harvesting at some time intervals and are not able to receive the maximum energy from the harvester.

In the MPPT method presented in [20], an auxiliary energy harvester is used in addition to the main harvester. Using the active rectifier and the adjustable RC filter at the output of the unloaded auxiliary harvester, the reference voltage required for the MPPT algorithm is provided. The use of active rectifiers, off-chip elements and auxiliary harvester has reduced the efficiency of this method.

Due to the nature of energy harvesting from the magnetic field, matching the output impedance of the harvester with

the input impedance of the interface circuits is one of the most effective methods in transferring maximum power [21–24]. In this method, the use of additional circuits and sensors in order to obtain the parameters related to the matching impedance usually leads to increased design complexity and power consumption.

In [25], a conduction-angle-controlled MPPT method is proposed. In this method, an active rectifier is used as the AC/DC converters. By sampling the active rectifier voltage and the input AC voltage and processing the data in the digital domain, the control signals required by the DC/DC boost converter and the active rectifier are generated to follow the maximum power point.

The MPPT method presented in [26] is suitable for piezoelectric energy harvester because it uses the relatively large internal capacitor of the piezoelectric together with an offchip inductor to adjust the output voltage of the harvester close to the optimum voltage corresponding to the maximum power point. In this method, the piezoelectric AC voltage is rectified using a zero-cross detection circuit. With different types of piezoelectrics, the capacitors used in this method must be readjusted manually based on the internal capacitor of the piezoelectric using an array of capacitors.

In the MPPT presented in [27], the output voltage of the harvester is first sampled and the target reference current is calculated using an external microprocessor. This reference current is compared with the sampled current on the load side by a hysteresis comparator, and the control signals of the transistors used in the H-bridge are generated to match the impedance. The use of the current sensor and microprocessor increases power consumption and reduces the efficiency of the energy harvesting system.

To adjust the output voltage of the Synchronized Switch Harvesting on Inductor (SSHI) circuit to the optimal value, in [28], a fractional open circuit voltage (FOCV) MPPT scheme is used to change the DC/DC boost converter frequency using pulse skipping modulation (PSM). In this method, the MPPT circuit is activated once almost every 15 s and the circuit efficiency is 77%. In contrast, in [29], the MPPT circuit dynamically measures the input impedance at each switching period (about a few microseconds) to match the impedance. The use of two current sensors and the need to pre-configure analog processing circuits in accordance with the energy harvester parameters are the weaknesses of this method.

Previously in [30] an approach was presented to perform impedance matching on a known coil resistance without current sampling shunts. The problems related to power loss due to current sampling were eliminated by sampling the voltage drop across the transistors used in the H-bridge. Unlike conventional methods which required symmetric positive and negative supply rails for the analog processing elements, a modified pulse width modulation (PWM) method was also proposed so that the control circuits could be operated with a single asymmetric power supply available at the output node. The proposed design, however, was incapable of maximum power point tracking in the event when coil parameters vary.

In this paper, a low-power and integrated interface circuit for maximum power point tracking is proposed for energy harvesting from magnetic fields at long distance from the overhead power line. The proposed design performs several functions such as impedance matching on AC input waveforms without the need for initial rectification, maximum power point tracking based on the harvester coil parameters and output voltage regulation all based on low-power mixed-signal circuits. The AC current harvested by the coil is initially transferred to an output capacitor using an H-bridge MOSFET configuration. Unlike previous methods which use microcontrollers and OPAMPs [27, 31, 32], the switching sequence of the bridge is controlled using only low-power comparators and basic digital gates. A Schmitt trigger-based voltage regulator is designed at the output node to keep the capacitor output potential constant. With this approach when the available input power increases, the rate at which the load is activated increases, while at low available input powers, this rate will decrease. Furthermore, since the coil resistance can change due to ambient thermal conditions, a low power MPPT controller is presented to adjust the impedance matching circuit operation point. The optimum operation point for the impedance matching circuit is discovered by the tracking circuit using a feedback loop which monitors the voltage ripples on the presented output regulator. Thus, in the proposed design, instead of using rectifiers and methods based on DC to DC converters [33–35], the H-bridge structure is used to directly convert induced AC voltage to DC voltage, which simultaneously provides an impedance matching condition to transfer the maximum power using the MPPT circuit. The proposed processing blocks are used to adjust the output DC voltage, receive feedback from the ripple period of the DC output voltage, perform processing related to MPPT, and adjust the optimal threshold voltage required for the PWM signal generation section. The use of low-power digital and analog circuits in the proposed method has led to an acceptable efficiency despite the low input power levels.

To evaluate the effectiveness of the proposed design several performance factors are investigated under different operation conditions. Throughout the evaluations, the MPPT efficiency (ratio of power received at the circuit input to the maximum available power from the coil), circuit efficiency, and overall efficiencies are studied under different input powers, temperature conditions, coil parameters and output potentials. It has been shown that at an input power of 119  $\mu$ W a circuit efficiency of about 92.4% and an MPPT efficiency of about 95% are obtainable.

In the rest of this paper, in Sect. 2, an overview of the proposed system and its different blocks is presented along with the MPPT algorithm. The circuit implementation of the various sections of the proposed system is given in Sect. 3. In Sect. 4, the complete system is evaluated, and the results of the circuit operation and comparison with previous works are presented. Finally, Sect. 5 provides a conclusion and summarizes the proposed approach.

## 2 Proposed system overview

Figure 2a shows the overview of the AC/DC converter previously presented in [30], in which a new method was used to generate the PWM signal. In [30], without the need for symmetrical power supply and without current sampling, the current is transferred from the coil side to the output battery, and at the same time, impedance matching is performed in order to transmit the maximum power. As can be seen, there is no output voltage regulator in this structure, and the presented AC/DC converter can only charge a battery with a constant voltage at the output. In addition, in the previous circuit, in different environmental conditions, if the coil parameters are changed, the appropriate set point required to transmit the maximum power should be adjusted manually. Figure 2b shows the overall diagram of the proposed magnetic field energy harvesting system with the ability to automatically track the maximum power point and regulate the output voltage. In the proposed structure, the appropriate operation point for the impedance matching section is continuously provided by the tracking section. In this way, maximum power is always received from the coil and transferred to the load in different conditions. In addition, without the need for a battery and simply by using a low leakage capacitor in the output port, the output voltage is fixed and adjusted at the required voltage level.



Fig. 2 Overview of a AC/DC converter using modified PWM/matching circuit without MPPT and output voltage regulator previously presented in [30] b the proposed energy harvesting system with MPPT and output voltage regulator

The main components are AC to DC voltage converter with impedance matching capability, an output voltage regulator, and a tracking circuit. If the optimal PWM signal is applied to the AC/DC converter, the input impedance of the converter will be matched to the output impedance of the harvester at the same time as the AC to DC voltage conversion. Capacitor  $C_{strg}$  used at the output of the AC/DC converter acts as an energy storage element and its voltage is regulated by a voltage regulator in a specified voltage range. The voltage regulator block, based on a hysteresis curve, establishes the energy transfer path to the load when the capacitor voltage is in the specified voltage range using a transmission gate (TG). In addition, the voltage regulator block generates the signal required for the tracking circuit. The tracking circuit, which consists of low-power digital and analog circuits, controls the amount of energy received from the energy harvester

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**Fig.3** Equivalent circuit of the H-bridge block for matching the input impedance of the AC/DC converter with the output impedance of the energy harvester

by examining the number of times the capacitor is charged and discharged (which corresponds to the frequency of the capacitor voltage ripple) at specified intervals. So, the voltage needed to generate the sawtooth wave with a suitable amplitude is produced to finally achieve the optimal PWM signal for impedance matching. The following describes how the main components of the proposed circuit work.

#### 2.1 AC/DC converter

The AC/DC converter used in the proposed system is based on the use of H-bridge transistors. The main advantage of using an H-bridge is that it can adjust the input impedance of the converter by changing the duty cycle of the PWM signal without the need for off-chip elements and using the inductor effect of the coil itself. By adjusting the impedance seen after the coil, maximum power transfer can be achieved.

Figure 3 shows an equivalent circuit for impedance matching using the H-bridge circuit. The effect of the coil inductor  $(L_S)$  at the AC line frequency is neglected, assuming that the resistance of the energy harvester coil  $(R_S)$  is much smaller than the inductance of the coil inductor  $(|\omega L_S| \ll R_S)$ or assuming that the inductor effect is compensated by proper capacitance at the frequency of the voltage source  $V_S$ (50/60 Hz). This circuit is equivalent to a dependent voltage source  $(V_{adj})$  series with the drain-source resistance  $(R_{DS})$ of the transistors used in the H-bridge (Fig. 2). By changing the duty cycle of the PWM signal (D) from zero to one, the voltage value of  $V_{adj}$  changes from  $-V_{dd}$  to  $+V_{dd}$ . Hence, it can be written:

$$V_{adj} = (2\mathbf{D} - 1)V_{dd} \tag{1}$$

Also from Fig. 3, Eq. (2) can be obtained as follows:

$$V_i = V_{adj} + V_{R_{DS}} \tag{2}$$

where  $V_{R_{DS}}$  is the voltage drop across the transistors used in the H-bridge. By replacing Eq. (1) in Eq. (2) the following equation is obtained:

$$V_i = (2D - 1)V_{dd} + V_{R_{DS}}$$
 (3)

Since  $V_{R_{DS}}$  is about a few millivolts, in general  $(2D - 1)V_{dd} \gg V_{R_{DS}}$ , so Eq. (3) can be simplified to:

$$V_i \approx (2D - 1)V_{dd} \tag{4}$$

Thus, considering Eq. (4), the resistance seen at the output of the energy harvester  $(R_{out})$  can be expressed as follows:

$$R_{out} \approx \frac{(2\mathrm{D}-1)V_{dd}}{I_s} \tag{5}$$

By instituting  $I_s = \frac{V_{R_{DS}}}{R_{DS}}$  in Eq. (5) we have:

$$R_{out} \approx \frac{(2\mathrm{D}-1)V_{dd}}{\frac{V_{R_{DS}}}{R_{DS}}} = \frac{(2\mathrm{D}-1)V_{dd}R_{DS}}{V_{R_{DS}}}$$
(6)

According to the PWM signal and the sawtooth wave shown in Fig. 3, the duty cycle D is equal to:

$$D = \frac{1}{2} \left( 1 + \frac{V_{R_{DS}}}{V_{amp}} \right) \tag{7}$$

where  $V_{amp}$  is the amplitude of the sawtooth wave. By replacing Eq. (7) in (6) and simplifying it, the following equation is obtained:

$$R_{out} \approx \frac{V_{dd} R_{DS}}{V_{amp}} \tag{8}$$

According to the maximum power transfer theorem, to receive the maximum power from the energy harvester and transfer it to the circuit,  $R_{out}$  must be equal to  $R_S$  ( $R_{out} = R_S$ ). Therefore, for maximum power transfer, the following equation can be obtained:

$$R_S = \frac{V_{dd} R_{DS}}{V_{amp}} \tag{9}$$

By rewriting Eq. (9) with regard to  $V_{amp}$ , the following equation is obtained:

$$V_{amp} = \frac{V_{dd} R_{DS}}{R_S} \tag{10}$$

Equation (10) shows that for a given amplitude of the sawtooth ( $V_{amp}$ ), the optimal duty cycle is created for the PWM signal, and as a result, the maximum power is transferred by providing the impedance matching condition. As shown in Fig. 2, the appropriate value of  $V_{amp}$  is generated in a feedback loop by the MPPT circuit and sent to the PWM/matching circuit. The control signals required by the tracking circuit, including the clock signal (clk) and PWM' signals, are also generated by the PWM/matching circuit.

Unlike conventional methods of generating a PWM signal, this voltage converter uses a modified method to generate a PWM signal, which its operation and related relationships are described in our previous work in detail [30]. The features of the modified PWM signal generation method can be summarized as follows: 1- No need for a current sensor to sample the converter input current, 2- Use of voltage drop of transistors used in H-bridge to generate control signals, 3-No need to process symmetrical signals, and thus, no need for circuits with positive and negative power supply rails.

#### 2.2 Voltage regulator

This part of the circuit regulates the capacitor  $C_{strg}$  voltage (vdd) using the hysteresis characteristic of a Schmitt trigger. By selecting  $V_{ref2} > V_{ref1}$  in the hysteresis characteristic, if the capacitor voltage exceeds  $V_{ref2}(vdd > V_{ref2})$ , the output of the Schmitt trigger  $(V_{schmitt})$  becomes high and the transmission gate connected to the load is activated; thus, the energy stored in the capacitor  $C_{strg}$  is transferred to the load. By transferring the capacitor energy to the load and reducing the capacitor voltage below the  $V_{ref1}$ , the output of the Schmitt trigger becomes zero and the transmission gate is deactivated; thus, the load is disconnected from the capacitor and the capacitor is recharged to  $V_{ref2}$ . The Schmitt trigger output, in addition to its role in voltage regulation, is also used as the main input of the tracking circuit for the delivered power estimation. In other words, as the input power increases, the rate of to be on increases for the load, and as the input power decreases, the rate decreases. The number of Schmitt trigger output pulses corresponds to the ON rate of the load and the input power, which will be discussed in the next section.

#### 2.3 Maximum power point tracking

The operation of the proposed low power circuit for the proposed tracking circuit is based on the perturbation and observation (P&O) method. In this way, the power delivered to the output of the AC/DC converter is monitored over a period of time, and depending on the amount of power received, the amplitude of the sawtooth changes in such a way that more power is transferred to the output of the converter. According to Fig. 3, and assuming that the voltage across the

capacitor  $C_{strg}$  (vdd) is constant, the power received at the output of the converter ( $P_{out}$ ) can be written:

$$P_{out} = I_{out} v dd \tag{11}$$

Using the voltage regulator circuit, the voltage ripple of the capacitor  $C_{strg}$  ( $\Delta vdd$ ) is small and constant ( $\Delta vdd = V_{ref2} - V_{ref1}$ ), so the relationship between current and voltage of the capacitor  $C_{strg}$  can be expressed as follows:

$$I_{out} = C_{strg} \frac{\Delta v dd}{\Delta t_{ch}} \tag{12}$$

where  $\Delta t_{ch}$  is the time that the capacitor charges from  $V_{ref1}$  to  $V_{ref2}$ . Replacing Eq. (12) in Eq. (11) results in:

$$P_{out} = C_{strg} \frac{\Delta v dd}{\Delta t_{ch}} v dd \tag{13}$$

The charging frequency of the capacitor  $(f_{ch})$  can be substituted for  $\frac{1}{\Delta t_{ch}}$ . Since the charging frequency of the capacitor is equal to the number of times the capacitor is charged  $(N_{ch})$  at a given constant time  $(T_{PE})$ , Eq. (13) can be rewritten as follows:

$$P_{out} = v ddf_{ch} C_{strg} \Delta v dd = C_{strg} \frac{N_{ch} \Delta v dd}{\Gamma_{PE}} v dd \qquad (14)$$

where  $T_{PE}$  is a constant time interval for power estimation. In other words, during this time, the number of the capacitor charging is counted to obtain the charging frequency of the capacitor which corresponds to the ripple frequency of the capacitor voltage. If the values of  $C_{strg}$ ,  $\Delta vdd$ , vdd, and  $T_{PE}$  are kept constant, Eq. (14) can be simplified to:

$$P_{out} = k N_{ch} \tag{15}$$

where k is a constant coefficient equal to:

$$k = C_{strg} \frac{\Delta v dd}{T_{PE}} v dd \tag{16}$$

According to Eq. (15) in the proposed MPPT method, assuming the load is constant, the amount of available power is examined by counting the number of times the capacitor is charged in a certain time interval, which is proportional to the frequency of the capacitor voltage ripple. Thus, the more number of times the capacitor is charged ( $N_{ch}$ ) in a certain time interval ( $T_{PE}$ ), indicates a short capacitor charging time, more ON-rate of the load, and more available power, and vice versa. This requires a proper time reference generator to keep  $T_{PE}$  constant. Due to the constant frequency of the transmission line, this paper will use the proposed low-power zero-crossing detection circuit for this purpose. This circuit converts the input sinusoidal signal to a 50 Hz



**Fig.4** Waveforms of capacitor voltage (*vdd*), Schmitt trigger output ( $V_{schmitt}$ ) and input AC voltage ( $V_S$ ) for  $V_{ref1} = 1.7V$  and  $V_{ref2} = 1.9V$  in the proposed MPPT

clock pulse (clk\_50 Hz signal). As will be explained later, to reduce power dissipation, no extra comparators are used for the zero crossing detection and the required waveform is generated by the signals already available from the PWM impedance matching section.

As discussed in Sect. 2.2, each output pulse of the Schmitt trigger ( $V_{schmitt}$ ) in the voltage regulator block corresponds to a single charge and discharge of the capacitor  $C_{strg}$ . Therefore, the number of Schmitt trigger pulses is equal to the number of times the capacitor is charged  $(N_{ch})$ , as shown in Fig. 4. Figure 4 shows an example of a capacitor voltage waveform charging and discharging between 1.7 and 1.9 V along with a Schmitt trigger output at one period of the input AC voltage. Since in the positive cycle of input AC voltage, the power transfer conditions are similar to the negative cycle of input AC voltage, in the proposed method, the number of Schmitt trigger pulses is counted only in half of the input AC voltage period (i.e.,  $T_{PE} = 10ms$ ) and compared with the value counted in half of the previous period of the input AC voltage. According to the comparison result and the history of changes in the voltage  $V_{amp}$  in the previous cycle, the new  $V_{amp}$  voltage is generated to increase the amount of transferred power.

The flowchart of the proposed MPPT algorithm is shown in Fig. 5. In this algorithm,  $R_i$  is a register that expresses a history of changes in the  $V_{amp}$  voltage. Where  $R_i = 1$  and  $R_i = 0$  indicate the increase of  $V_{amp}$  and the decrease of  $V_{amp}$  in the previous period, respectively. At the beginning of the algorithm, since the  $V_{amp}$  voltage is zero, the register  $R_i$  is initialized. The number of Schmitt trigger pulses at half of the current period  $(N_{ch}[n])$  is compared with the number of pulses at the half of the previous period  $(N_{ch}[n-1])$ . If the number of Schmitt trigger pulses in the current state is unchanged or increased  $(N_{ch}[n] \ge N_{ch}[n-1])$  which is equivalent to not changing or increasing the amount of transferred power, given that in the previous state  $V_{amp}$  increased (or decreased), then also  $V_{amp}$  increases (or decreases). Whenever the number of Schmitt trigger pulses at half of the current period decreases compared to the previous state  $(N_{ch}[n] < N_{ch}[n-1])$ , if in the previous state  $V_{amp}$  increased (decreased) then  $V_{amp}$  decreases (increases) for the next state. Thus, by continuing this process, the  $V_{amp}$  voltage is always adjusted to generate the sawtooth wave required by the AC/DC converter, and as a result, the PWM signal is generated with an optimal duty cycle. If the optimal amplitude of the sawtooth wave  $(V_{amp})$  shown in Eq. (10) changes and the circuit deviates from the impedance matching and maximum power transferring conditions, the proposed MPPT method by adjusting the amplitude of the sawtooth wave  $(V_{amp})$  will be able to track the maximum power point again.

The 50 Hz square wave signal (clk\_50 Hz) in the proposed MPPT method is generated using the clk and PWM signals of the AC/DC converter part. After counting the number of Schmitt trigger pulses during the half period of the clk\_50 Hz signal (i.e., 10 ms), in the other half of the period, the necessary processing is performed according to the proposed MPPT algorithm. The increment and decrement signals generated by the logic circuits are sent to the amplitude voltage generator (AVG) block, causing the voltage  $V_{amp}$  to change. The circuit implementation of various parts of the proposed MPPT method is presented in the next section.

## **3 Circuit implementation**

#### 3.1 AC/DC converter control circuit

The implementation of the PWM impedance matching section control circuit and the detailed operation principle is explained in our previous work [30]. Here, the overall circuit is shown in Fig. 6a for review. The sample and hold unit (S&H) consist of two capacitors and two NMOS switches. The sampled voltages are sent to the pulse width domain signal processing unit. This unit which is made of an analog multiplexer, comparator block (Comp1), and some digital gates generates the PWM signal needed to control the gate of the transistors used in the H-bridge. The output of the comparator Comp1 (PWM') is also sent to the tracking circuit in addition to generating a PWM signal. The variable ramp/clk signal generator unit consists of digital and analog parts. The analog circuit generates the sawtooth wave (ST) using a comparator (Comp2) based on the linear charge of capacitor C2 and its instantaneous discharge. The digital part, which is a frequency divider, generates the clk signal at half the frequency of the sawtooth wave, which in addition to generating the PWM signal, it is also sent to the tracking circuit.

The internal circuit of the Comp1 and Comp2 comparators is shown in Fig. 6b. Since the drain-source voltages of



Fig. 6 Circuit implementation of a the AC/DC controller, b comparator circuit using PMOS differential pair as the input stage [30]

transistors M1 and M3 used in the H-bridge and the amplitude of the sawtooth wave (ST) are in the millivolt range, the input stage of the comparators is designed using a PMOS differential pair to perform the comparison process even with low input voltages. As depicted in Fig. 6, all of the circuits are implemented using only a single power supply.

## 3.2 Schmitt trigger

The Schmitt trigger circuit implementation used in the voltage regulator part is shown in Fig. 7a. As can be seen, the Schmitt trigger circuit consists of two low-power comparators and an RS-flip-flop. Based on the hysteresis curve shown in Fig. 7b, when the input voltage of the Schmitt trigger ( $V_{in}$ ) exceeds the voltage  $V_{ref2}$ , the output of the Schmitt trigger ( $V_{schmitt}$ ) becomes one, and as long as the voltage  $V_{in}$ is more than the voltage  $V_{ref1}$ , the Schmitt trigger output remains one. When the voltage  $V_{in}$  falls below  $V_{ref1}$ , the output of the Schmitt trigger goes zero, and as long as  $V_{in}$ is less than the voltage of  $V_{ref2}$ , the output of the Schmitt trigger remains zero. The circuit structure of the low-power comparators Comp3 and Comp4 is shown in Fig. 7c. As



Fig. 7 a Circuit implementation of the Schmitt trigger, b Schmitt trigger hysteresis transfer curve (c) comparator circuit used in the Schmitt trigger

depicted, an open-loop two-stage operational amplifier circuit with NMOS differential pair at the input stage is used as a comparator. Since the input voltages are in the range close to vdd, the NMOS differential pair is chosen for the input stage. To generate the bias voltages shown in Figs. 6b and 7c, as well as the voltages  $V_{ref1}$  and  $V_{ref2}$ , voltage references designed for low-power applications can be used for this purpose [36].

## **3.3 MPPT**

The circuit implementation of the proposed MPPT method is shown in Fig. 8. All flip-flops used in the proposed tracking circuit are the positive edge-sensitive type. As shown in Fig. 8b, a square wave signal with a frequency of 50 Hz is generated using a D-flip-flop, and the *clk* and *PWM* signals generated in the AC/DC converter control circuits. This generated signal is used as the clock signal for the logic circuit block shown in Fig. 8a. When the clk\_50 Hz signal is zero, the number of Schmitt trigger pulses is counted by the counter. At the rising edge of the clk 50 Hz signal, the current output of the counter  $(N_{ch}[n])$  is compared with the counter output in the previous period of the clk\_50 Hz signal  $(N_{ch}[n-1])$ . Depending on the result of the comparison and the value of  $R_i$ , increment and decrement signals are generated and sent to the AVG block. In this section and as shown in Fig. 8c, the voltage across the capacitor  $C_{amp}$  is used as the  $V_{amp}$  voltage required for the AC/DC voltage converter. To change the  $V_{amp}$  voltage, the capacitor  $C_{amp}$  is charged and discharged by  $M_i$  and  $M_d$  transistors, respectively. The required bias voltage of these transistors is supplied by increment and decrement signals using voltage dividers made with N-type diode-connected transistors.

Since the rate of change of the voltage  $V_{amp}$  at each period is about a few millivolts, and given that the capacitor  $C_{amp}$  is charged and discharged during the half period of the clk\_50 Hz signal (i.e., 10 ms), it is necessary for the charging and discharging current of the capacitor  $C_{amp}$  to be small (in the range of several pico amperes) so that by selecting a small capacitor, it can be implemented without off-chip elements. Therefore, the width to length ratio of transistors  $M_i$  and  $M_d$  should be chosen as small as possible. For this purpose, a series connection of several transistors with the minimum width and maximum channel length is used, in which case the width to length ratio of the equal transistor is equal to  $\frac{W}{L_{eq}}$ . In addition, to reduce the drain current of transistors  $M_i$  and  $M_d$ , their bias voltage must be selected to operate the transistors in the sub-threshold region.

# 4 Evaluation of the proposed interface circuit

## 4.1 Simulation results

In this section, the whole structure of the proposed energy harvesting system including AC/DC converter with control circuits, voltage regulator and tracking circuit is designed using 0.18 µm standard CMOS technology. To select the amount of elements used in the simulation, the usual values in similar energy harvesters have been used [15]. Accordingly, the amplitude of the AC output voltage ( $A_{Vs}$ ) is equal to 1 V and its frequency ( $f_{Vs}$ ) is equal to 50 Hz. The values of resistance and inductor related to energy harvesting coil, output load resistance and energy storage capacitor are equal to  $R_S = 1 \text{ k}\Omega$ ,  $L_S = 100\text{ mH}$ , Load = 3.3 k $\Omega$  and  $C_{strg} = 100$ nF, respectively. The output voltage of the AC/DC converter, which is used as the supply voltage of the proposed circuit and the load voltage, is equal to vdd =  $1.8 \pm 0.1$  V. Thus,

comparato V<sub>schmitt</sub>  $N_{ch}[n]$ clk Count AgeB  $(A \ge B)$ D 0 decrement counter register MI cremen  $N_{ch}[n$ AlB RST (A < Bin out R D D 0 R. logic circuit (a) increment decremen Clk 50 Hz 50 Hz clk generator amplitude voltage generator (b) (c)

**Fig.8** Circuit implementation of the proposed tracking circuit **a** Logic circuit related to the implementation of the proposed MPPT algorithm, **b** 50 Hz square wave generator, **c** amplitude voltage generator (AVG)

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the voltages  $V_{ref1}$  and  $V_{ref2}$  used in the voltage regulator are equal to 1.7 V and 1.9 V, respectively.

To evaluate the correctness of the proposed circuit operation, the waveforms of the various parts of the circuit are shown in Fig. 9. For a better view of the vdd voltage ripple and the Schmitt trigger output, part of the figure is magnified when the clk\_50 Hz signal value is zero. As can be seen in the middle of this interval, which corresponds to the maximum amplitude of the AC input voltage, the frequency of the vdd voltage ripple and the Schmitt trigger output has been increased due to the greater input power. The number of Schmitt trigger output pulses ( $V_{schmitt}$ ) in this interval is indicated on the figure (#29). At the rising edge of the clk\_50 Hz signal, which indicated by the letter A in Fig. 9, the number #29 is compared to the number of pulses at the previous cycle (#26). Since 29 > 26, according to the proposed MPPT algorithm, the change of the amplitude voltage  $V_{amp}$  will be at the same direction of the change of  $V_{amp}$  at the previous cycle. Because the  $V_{amp}$  voltage has decreased in the previous cycle, (shown in the figure with the letter B) then the  $V_{amp}$  voltage decreases again (shown in the figure with the letter C).

In order to ensure the correct operation of MPPT, the maximum power point tracking efficiency diagram ( $\eta_{MPPT}$ ) versus processing cycle is shown in Fig. 10. A processing cycle is a 20 ms interval in which the number of Schmitt trigger output pulses is counted and the amplitude voltage ( $V_{amp}$ ) changes. The following equation is used to calculate  $\eta_{MPPT}$ :

$$q_{MPPT} = \frac{P_{in}}{P_{max}} \times 100 \tag{17}$$

where  $P_{in}$  is the power input to the transistor bridge ignoring the  $L_S$  effect and is equal to:

$$P_{in} = P_{V_S} - P_{R_S} \tag{18}$$

where  $P_{V_S}$  and  $P_{R_S}$  are the power of the input source  $V_S$  and the power dissipated in the resistor  $R_S$ , respectively.  $P_{max}$  is the maximum power transferred to the input of the transistor bridge ignoring the effect of  $L_S$  and in impedance matching conditions ( $R_{out} = R_S$ ) ( $R_{out}$  is shown in Fig. 2). According to the values selected in the simulation, the value of  $P_{max}$ is equal to 125  $\mu$ W. Due to the symmetry of the sinusoidal signal of the input source, the power calculation is done at half the frequency of the clk\_50 Hz signal at which the amplitude voltage ( $V_{amp}$ ) is constant. In addition, in Fig. 10, to show the relationship between MPPT efficiency and amplitude voltage changes, the amplitude voltage sampled in half cycle which the  $V_{amp}$  voltage is constant ( $V_{amp_{sampled}}$ ) is displayed over processing cycle.

As shown in Fig. 10, when the MPPT efficiency decreases, by reversing the direction of change of the voltage  $V_{amp}$ , the value of  $\eta_{MPPT}$  increases. In this way, the efficiency of MPPT is maintained in the range of 93–96%, which indicates the proper performance of MPPT. As expected from the P&O MPPT algorithm, the  $V_{amp}$  voltage has an oscillatory behavior. For example, Fig. 10 shows that the  $V_{amp}$ 



Fig. 9 Output waveform of different sections of the proposed circuit

**Fig. 10** MPPT efficiency diagram ( $\eta_{MPPT}$ ) and sampled amplitude voltage ( $V_{amp_{sampled}}$ ) versus processing cycle



Fig. 11 MPPT efficiency diagram and sampled amplitude voltage  $V_{amp_{sampled}}$  versus processing cycle for different values of  $R_S = 0.5, 1, 1.5$ 



voltage fluctuates in the range of 30–55 mV with an oscillation amplitude about 20 mV.

To calculate the efficiency of the proposed circuit including AC/DC converter, control circuit, tracking circuit, and voltage regulator, the following relation is used:

$$\eta_{circuit} = \frac{P_{Load}}{P_{in}} \times 100 \tag{19}$$

in which  $P_{Load}$  is the delivered power to the load. Accordingly, the efficiency of the proposed circuit at input power of  $P_{in} = 119\mu W$  is equal to 92.4%. In addition, the power consumption of the various parts of the proposed circuit is shown in Table 1. As can be seen, the highest power consumption is related to the AC/DC converter (including impedance matching circuit and transistor bridge). By increasing the dimensions of the transistors used in the H-bridge, the losses caused by them can be reduced, but instead the corresponding drain-source voltage drop is also reduced, and as a result, it becomes difficult to compare the resulting voltage drop with the sawtooth voltage.

Since the value of the winding resistance  $(R_S)$  changes with the change of ambient temperature as well as the change of the energy harvesting coil, a simulation was performed to evaluate the performance of the proposed circuit for three values of  $R_S = 0.5$ , 1,  $1.5k\Omega$ . The results including MPPT efficiency and the amplitude voltage changing are shown in Fig. 11. As can be seen, by changing the resistance  $R_S$ , first the efficiency of MPPT decreases (points A shown in Fig. 11), but then, after 3 processing cycles, by changing the amplitude voltage  $(V_{amp})$ , the impedance matching conditions are provided again and the maximum power point is tracked, thus increasing the MPPT efficiency.

To evaluate the performance of the proposed circuit at different temperatures, simulations were performed at temperatures between  $-30^{\circ}$ C and  $+90^{\circ}$ C. For different

temperatures, the proposed circuit efficiency ( $\eta_{circuit}$ ), the average of MPPT efficiency ( $\eta_{MPPTAvg}$ ) and the average of the amplitude voltage change at each step ( $V_{amp_{step}}$ ) are shown in Fig. 12. As can be seen, the efficiency of the proposed circuit does not change much at different temperatures and remains in the range of 92 to 94%. In addition, as the temperature increases, the voltage  $V_{amp_{step}}$  increases, leading to an increase in the  $V_{amp}$  voltage fluctuation amplitude and thus a decrease in the average MPPT efficiency. However, the average MPPT efficiency at +90°C is still above 83%.

To further investigate the relationship between MPPT efficiency and  $V_{amp}$  voltage oscillation range ( $V_{amp_{osc}}$ ), different steps of  $V_{amp}$  voltage change ( $V_{amp_{step}}$ ) can be generated using different values of  $C_{amp}$  capacitor. Figure 13 shows  $V_{amp_{step}}$ ,  $V_{amp_{osc}}$ , and  $\eta_{MPPT_{Avg}}$  versus different values of capacitor  $C_{amp}$ . As can be seen, by increasing the value of capacitor  $C_{amp}$ , the changing step of  $V_{amp}$  voltage is reduced, and as a result, the oscillation range of  $V_{amp}$  is reduced. So, the oscillation around the maximum power point is reduced and the average efficiency of MPPT ( $\eta_{MPPT_{Avg}}$ ) is increased.

Since the amplitude of the input AC voltage source  $(A_{V_S})$  can change according to the amplitude of the magnetic field in the environment, the effect of the change of  $A_{V_S}$  on the performance of the proposed circuit is simulated, which results are shown in Fig. 14. As can be seen, as the voltage amplitude  $A_{V_S}$  decreases, the circuit continues to operate and tracking the maximum power point, except that by changing the value of  $A_{V_S}$ , the average of MPPT efficiency also changes due to changes in the common mode level of the input of the comparator Comp1 and non-ideal comparator characteristics such as intrinsic delay and offset voltage. According to the simulation results, for a 50% reduction in the voltage amplitude  $A_{V_S}$ , the average of MPPT efficiency is reduced only about 13%. In addition, the proposed circuit efficiency ( $\eta_{circuit}$ ) versus  $A_{V_S}$  is also depicted in Fig. 14. As can be

 
 Table 1 Power consumption of different sections of the proposed circuit

Main part	Sub-circuit	Power consumption (nW)	
AC/DC converter with impedance matching capability	S&H	4.3	
	Pulse width domain signal processing	1444.2	
	Variable ramp/clk	1289	
	H-bridge Transistors	4794	
Voltage regulator	Schmitt trigger	682	
	TG	796	
Tracking circuit	50 Hz clk generator	2.1	
	AVG	0.223	
	Logic circuit	10.77	
Total power		9022.6	



**Fig. 12** Proposed circuit efficiency ( $\eta_{circuit}$ ), average of MPPT efficiency ( $\eta_{\text{MPPTAvg}}$ ) and average of the amplitude voltage change in each step ( $V_{amp_{step}}$ ) versus temperature

seen, by changing the value of  $A_{V_S}$ , the efficiency of the proposed circuit also changes due to the change in the input power level. By increasing the value of  $A_{V_S}$ , which corresponds to the increase in the input power level, the power consumption of the proposed circuit can be ignored and the efficiency improves. As shown in Fig. 15, with the increase of the input power level ( $P_{in}$ ), the efficiency of the circuit and average of MPPT efficiency increase.

Since different energy harvesting coils have different inductor values, to investigate the effect of the inductor value on the performance of the proposed circuit, simulations were performed for  $L_S = 50$ , 100, 300, 3000mH. As can be seen in Fig. 16, for very small inductor values, the MPPT efficiency decreases due to the increase of the inductor current ripple. On the other hand, for very large inductor values, if the inductance effect is not compensated with proper capacitance, the MPPT efficiency will decrease due to the phase shift between the current and the voltage of the energy harvesting coil. In Fig. 16, the circuit efficiency ( $\eta_{circuit}$ ), the



**Fig. 13** Average of MPPT efficiency  $(\eta_{MPPT}_{Avg})$ , oscillation range of the  $V_{amp}$  voltage  $(V_{amp}_{acc})$ , and changing steps of  $V_{amp}$  voltage  $(V_{amp}_{step})$  versus different values of C<sub>amp</sub> capacitor



**Fig. 14** Average of MPPT efficiency ( $\eta_{MPPTAvg}$ ) and circuit efficiency ( $\eta_{circuit}$ ) versus input AC voltage amplitude ( $A_{VS}$ )

average of MPPT efficiency  $(\eta_{MPPT_{Avg}})$  and the inductor current ripple  $I_{S_{ripple}}$  versus different values of  $L_S$  and along with the ripple percentage are shown.



**Fig. 15** Average of MPPT efficiency  $(\eta_{MPPTAvg})$  and circuit efficiency  $(\eta_{circuit})$  versus input power  $(P_{in})$ 



**Fig. 16** Average of MPPT efficiency  $(\eta_{MPPTAyg})$ , circuit efficiency  $(\eta_{circuit})$  and inductor current ripple  $(I_{Sripple})$  versus different values of inductor  $L_S$ 



**Fig. 17** Average of MPPT efficiency ( $\eta_{MPPTAvg}$ ), and circuit efficiency ( $\eta_{circuit}$ ) versus different values of supply voltage (vdd)

To investigate the effect of supply voltage (vdd) on the performance of the proposed circuit, the simulation has been done for different values of the supply voltage vdd. As can be seen in Fig. 17, for a wide range of vdd voltage, the circuit efficiency and the average of MPPT efficiency remain above 87% and 85%, respectively, which indicates the robustness of the proposed circuit to changes in supply voltage.

Table 2 compares the different energy harvesting systems with the energy harvesting system from magnetic field around the power transmission overhead lines proposed here.

#### 4.2 Measurement results

Here, the measurement results of a prototype of the proposed energy harvesting system are presented. The constructed system consists of the energy-harvesting analog section and the interface circuit. For the energy harvesting section, an aircore coil is used, which is an enameled copper wire with a diameter of 0.4 mm wrapped around a ring for 1100 turns as shown in Fig. 18 (a). The interface circuit also includes AC/DC converter with impedance matching capability along with the signal generator using discrete elements (MOSFET array chips) designed and built on the printed circuit board (PCB), which is shown in Fig. 18b. A heater device drawing current has been used to provide the magnetic field similar to what is generated by overhead power lines in the laboratory environment. The magnetic field around the heater supply wire is used to induce voltage in the coil. Figure 18c shows the experimental setup including heater, coil, interface circuit and measurement equipment. According to the results, the input power to the circuit for an open circuit RMS coil voltage of  $V_{oc_{rms}} = 1.6V$ , and vdd = 2V, is equal to  $P_{in} = 520 \mu W$  and the efficiency of the circuit and the efficiency of the maximum power transferring in the matching conditions (excluding the power of the digital circuit) reach about 80% and 85%, respectively. In Table 3, a comparison has been made between the fabricated prototype and other similar works. The digital section is not included in the evaluation as eventually in a custom IC implementation the power dissipation corresponding to the digital part is negligible compared to power contribution of other sections in this work. As it can be seen, the proposed circuit has an acceptable efficiency despite the fact that it is made of discrete elements. By full-custom design and fabrication of the proposed system as an integrated circuit, the parasitic capacitors and subsequently power consumption of the circuit will be reduced considerably and as a result the efficiency and performance of the circuit can be improved and brought closer to what is observed in the simulation results.

## **5** Conclusion

In this paper, a low power and integrated interface circuit for energy harvesting from the magnetic field at far distance from the power transmission overhead lines were presented. In the proposed circuit, in addition to converting the AC voltage to DC voltage by a modified PWM method with Table 2 Comparing the simulation results of the proposed circuit with other similar works

Work	[37]	[33]	[38]	[39]	[40]	This work
	2019 Simulated	2020 Simulated	2017 Simulated	2016 Simulated	2012 Simulated	Simulated
Source	RF/Piezo/Solar	TEGa/BFCb/Solar	Solar	TEG	TEG/Solar	EM
Technology	0.18 µm CMOS	0.18 µm CMOS	0.18 μm CMOS	0.18 µm CMOS	0.18 μm CMOS	0.18 µm CMOS
Fully integrated	Yes (except inductor, capacitor)	Yes (except inductor)	Yes (except capacitors)	Yes (except inductors, capacitors)	Yes (except inductor, capacitors)	Yes
Input voltage range	$> 70 \text{ mV}@R_{\rm s} = 160 \text{ k}\Omega$	0.03–1 V	NA	$> 40 \text{ mV}@R_{s} = 6.2 \Omega$	0.03–0.3 V (startup @300 mV)	$> 0.5 \text{ V}@R_{\text{s}} = 1$ k $\Omega$
Output voltage regulation	Yes	Yes	Yes	Yes	Yes	Yes
Output voltage	1 V	1.83 V	1 V	1—3 V	1.8 V	1—2.2 V
Input power	<ol> <li>1.8 μW (using auxiliary energy harvester)</li> </ol>	602 µW	1.2 mW	266 μW	$214 \mu W$	119 μW
Circuit efficiency	88.2% (not including rectifier)	95.5% @ $R_{\rm s} = 100$ $\Omega$	82.4% @ 1.2 mW	$48\% @ V_{in} = 40 \text{ mV}$	$84\% @ V_{in} = 80 \text{ mV}$	92.4%
MPPT/matching efficiency	NA	NA	NA	NA	NA	95%@1.8 V 97%@1.2 V

<sup>a</sup>Thermoelectric generator

<sup>b</sup>Biofuel cell

impedance adjustment capabilities, a low power circuit is designed to execute an MPPT algorithm by checking the voltage ripple frequency and providing feedback to the low power impedance matching circuit. The components of the proposed circuit, the operation and details of each section were presented and designed using 0.18  $\mu$ m standard CMOS technology. Based on various simulations performed, the proposed energy harvesting system has a good performance in different environmental and circuit conditions, such as different temperatures, different input voltages (A<sub>VS</sub>), different supply voltages (vdd) and different energy harvesting coils. The proposed circuit consumes about 9  $\mu$ W at 1.8 V supply voltage and the average of MPPT efficiency ( $\eta_{MPPT_{Avg}}$ ), the circuit efficiency ( $\eta_{circuit}$ ), and the total efficiency ( $\eta_{total} = \eta_{MPPT_{Avg}}\eta_{circuit}$ ) are 95%, 92.4%, and 88%, respectively. Since the required power of the proposed circuit is supplied by the output capacitor, the proposed structure can be considered as a self-powered structure that can operate only with the power received from a magnetic pick-up coil. In addition to the simulations, a prototype of the proposed circuit was designed and fabricated using discrete elements, and the experimental results of the measurements show the correct and appropriate operation of the circuit.











Table 3 Comparison of the proposed system experimental results with other energy harvesting systems

Work	[41] 2016	[ <b>29</b> ] 2020	[27] 2018	[ <b>28</b> ] 2019	[25] 2017	This work
Source	Universal	EM	EM	Piezo	EM	EM
Technology	VIS 0.15 μm BCD	0.6 μm CMOS	0.18 μm CMOS	0.25 μm BiCMOS	0.35 µm CMOS	Discrete
Input voltage range	0.06–5 V	> 2 V	> 0.15 V	3.5 V	> 0.57 V	$> 1.3 \text{ V}@R_{s} = 0.4$ k $\Omega$
Output voltage	1.2–2.5 V	2–4.5 V	1.8 V	4.2 V	4.2 V	2–3 V
Input power	1 mW	65 mW	1.1 mW	34 µW	400 µW	520 μW
Circuit efficiency	50%	95.5%	71%	77%	95% (Not including voltage regulator)	80% (not including digital circuit)
MPPT/matching efficiency	82% @ 1 mW	95.8% @ 3 V	NA	NA	91%	85%@2 V 90%@2.43 V

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