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ORIGINAL PAPER

A new nine-level switched-capacitor-based multilevel inverter with low voltage stress and self-balancing

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Abstract
This study introduces a nine-level multilevel (MLI) inverter based on the switched-capacitor method. Not only does the suggested inverter ensure that the switches' maximum voltage stress is lower than the incoming voltage, but it also includes a voltage double boost capacity. As a result, it is indeed appropriate for high-voltage tasks. The suggested inverter has horizontal extension strategies that assist it to reach a higher level of output with voltage boost. This nine-level inverter could be made with two capacitors owing to a benefit of low voltage stress and devices with cheap power consumption. Furthermore, the self-balancing capability of capacitor voltage helps reduce control circuit complexity. The topology, working principles, modulation approach and the evaluation of the inverter's capacitor are presented. The proposed inverter's superiority is explored by comparing it to recently suggested hybrid and switched-capacitor multilevel inverters. Finally, a nine-level prototype is built to verify the theoretical analysis' accuracy as well as the suggested inverter's feasibility and efficiency.

Keywords Multilevel inverter · Switched capacitor · Low voltage stress · Self-balancing · Extension

1 Introduction

Multilevel inverters (MLIs) are key components in power electronics circuits because of their large power capability, lower operating voltage stress, low cost, design with low harmonics, modularity and stability.

1.1 Motivation and incitement

The topology that combines the neutral point clamp (NPC) and flying capacitor (FC) is one of the appealing solutions to reach a better level of output and enhance extensibility [1, 2]. In addition, the cascaded H-bridge (CHB) inverter has been tweaked to cut down on the number of power switches. These enhancements broaden the range of MLIs available. They all share the benefit of keeping all semiconductor switches' voltage stress to the dc input. These inverters cannot enhance voltage. Furthermore, NPC inverters still struggle with voltage balancing of capacitors. The presence of flying capacitors necessitates the use of more complicated control circuits. To meet the load demand and output diverse voltage levels, the inverters [2] utilize unique switch arrangements to interconnect multiple dc power supplies in series. It is possible to produce various dc voltage ratios, which improves their flexibility. On the other hand, their switches have maximum voltage stress (MVS) from two dc voltage supplies. Additionally, they lack voltage boosting capabilities and just have a single topology horizontal/vertical extension technique.

The switched-capacitor approach is a great method to address the issues outlined above [3] and [4]. There's no need for a more sophisticated signal circuit in switched-capacitor-based multilevel inverters. This may enhance low source dc voltages to high ac voltages by linking the pre-charged capacitors together. The benefits of such inverters include their compact size, great power density, weightless and minimal harmonic elements [2] and [5].

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1.2 Literature review

Several SCMLIs have indeed been suggested throughout the open literature [6] and [7]. The SCMLIs are described in [8–11] can keep capacitor voltages balanced. Furthermore, they are distinguished by the use of only a dc power supply capable of boosting the voltage. On the other hand, utilizing H-bridges to accomplish voltage orientation transformation will constrain their application since H-bridge raises the MVS of the switches while also increasing the capital cost. The H-bridge was eliminated without impacting the voltage orientation conversion [12]. However, some switches must sustain the output voltage's peak value, preventing their use in high-voltage applications. Although the architecture presented in [13–15] decreases the MVS of switches, the MVS of switches remains double that of the dc supply voltage. The suggested topologies in [16–18] can effectively decrease the switches' voltage stress. However, it has a greater number of switches. The suggested inverters in [19–22] use appropriate components to limit the MVS of switches from the power supply voltage. However, in the configurations presented in [19–21, 23, 24] there is room for improvement by using fewer capacitors.

1.3 Contribution and paper organization

The multilevel inverter based on the switched-capacitor approach has indeed been developed in this study to alleviate the disadvantages of the previously mentioned inverters in terms of requiring many components, excessive MVS of power switches and absence of voltage gain and voltage self-balancing in capacitors. The suggested inverter may improve the input voltage and achieve voltage self-balancing in capacitors when compared to existing MLIs. Moreover, inverter switches have an MVS that is restricted to lower than the power supply voltage. In comparison with low-voltage-stress SCMLIs, the suggested MLI uses fewer components. Furthermore, the suggested inverter is better in terms of its flexibility and capacity to provide inductive loads. Among the good aspects that make the suggested inverter, an appealing solution for low- and high-photovoltaic (PV) power generation applications is its low voltage stress.

2 Suggested multilevel inverter

2.1 Circuit arrangement

The topologies suggested in [19–22] have a common feature that one dc voltage source and two T-type voltage-dividing switched capacitors to accomplish a seven-level inverter. The two T-type capacitors are employed to develop the voltage step of $V_{dc}/2$, reducing the output waveforms' step voltage to a value less than V_{dc}, which can efficiently minimize the output voltage's total harmonic distortion (THD). However, SCs are not fully used because they are primarily used to divide the voltage and it is not possible to power the load by connecting it in series with the dc power source. As a consequence, such configurations require extra capacitors to create multilevel outputs.

A new nine-level switched-capacitor inverter has been developed in this study to cut down on the number of capacitors and so optimize the usage of the two capacitors as illustrated in Fig. 1b. The proposed topology consists of one dc power source, 11 switches and two capacitors. In this design, the two switched capacitors are used not only to produce the voltage level of $V_{dc}/2$ and also to operate as switched capacitors (SC), obviating the requirement for extra capacitors. Furthermore, the suggested topology is a rebuild of the topology presented in Fig. 1a [25]. The recent topology presented in Fig. 1a develops the seven level only using 10 switches. On the other hand, the proposed architecture generates the nine level while adding one switch. Moreover, the switched-capacitor arrangement ensures boost ability while allowing for a voltage gain of two with the assistance of the half H-bridge to convert the voltage polarity on the load. This feature results in a significant reduction in the MVS of switches as shown in Fig. 1. The suggested inverter can produce nine different levels of output: $\pm 2V_{dc}$, $\pm 3V_{dc}/2$, $\pm V_{dc}$, $\pm V_{dc}/2$ and ± 0.

2.2 Operating principle

The operation of a nine-level inverter is described in this section. Various output voltage steps are produced by switching the off and on positions of each switch. All of the operational positions for the various modes are listed in Table 1.

The numbers 0 and 1 denote the off and on positions of the corresponding switches. The positions of the capacitors are indicated by the symbols "CH," "DS," and "NC" which stand for charging, discharging and no change, respectively.

The current paths and direction in each working mode are depicted in Fig. 2. In addition, charging loop current (I_{ch}) resistive load loop current (I_o) and inductive load loop current (I_L) directions are presented to show the inductive load handling capability of the proposed inverter. It should be noted that the operating modes from 0 to V_{dc} have three current routes and boosting modes $3V_{dc}/2$ and V_{dc}allow two current routes. The first route is that the capacitors are charged in series by the input voltage. The capacitor could power the load in the second path. Finally, the third path proves that the proposed inverter is capable of powering inductive loads.

To charge the capacitors C_1 and C_2, switches S_5, S_6 and S_9 are continuously turned on at levels zero, one and two.

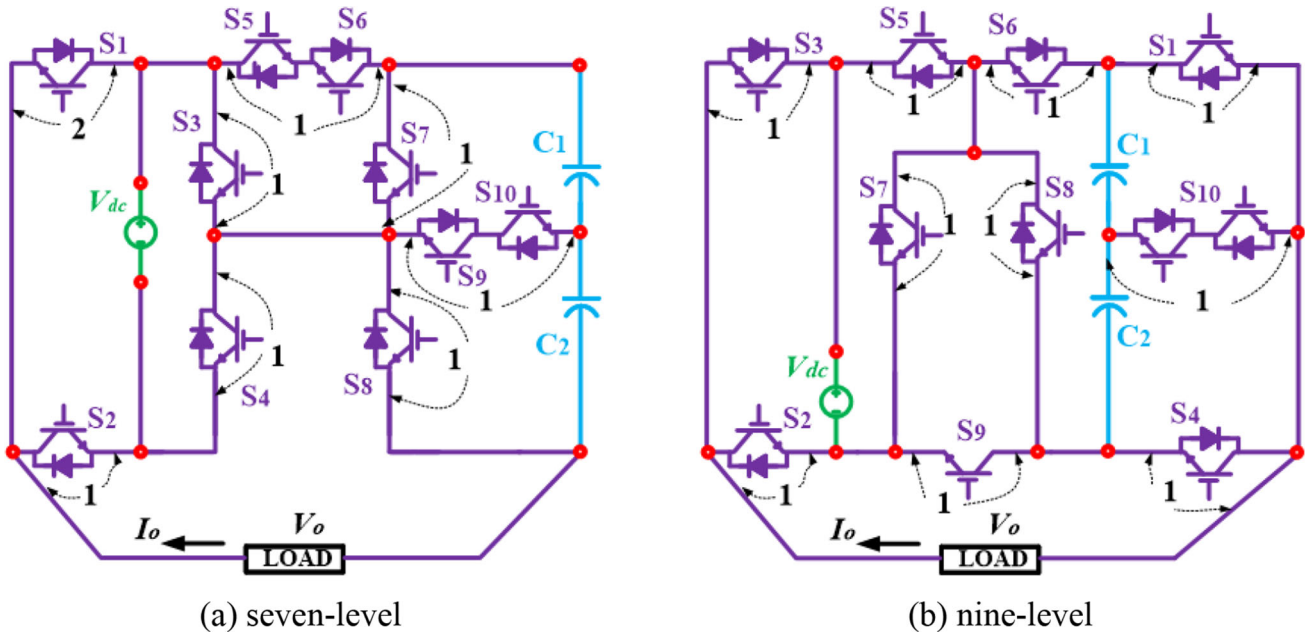


Fig. 1 Multilevel inverter with low voltage stress in per unit. **a** Recent topology, **b** suggested topology

Table 1 Switching patterns and state of capacitors

Voltage levels	Switches in half H-bridge circuit				Switches						Capacitors	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	C_1	C_2
$+2V_{dc}$	1	1	0	0	1	0	0	1	0	0	DS	DS
$+3V_{dc}/2$	0	1	0	0	1	0	0	1	0	1	NC	DS
$+V_{dc}$	1	1	0	0	1	1	0	0	1	0	CH	CH
$+V_{dc}/2$	0	1	0	0	1	1	0	0	1	1	CH	CH
+0	0	1	0	1	1	1	0	0	1	0	CH	CH
−0	0	1	0	1	1	1	0	0	1	0	CH	CH
$-V_{dc}/2$	0	0	1	0	1	1	0	0	1	1	CH	CH
$-V_{dc}$	0	0	1	1	1	1	0	0	1	0	CH	CH
$-3V_{dc}/2$	0	0	1	0	0	1	1	0	0	1	DS	NC
$-2V_{dc}$	0	0	1	1	0	1	1	0	0	0	DS	DS

CH Charging; *DS* Discharging; *NC* NO change

During this time, only three switches rather than four compare to recent topology [25] required a high-current rating. To complete the power loss estimate, Table 2 shows the current stresses of all semiconductor switches on each level. Here, I_{ch} is capacitors inrush current and I_o is the sum of load current. The proposed inverter's main advantage in terms of cost reduction is that only three switches are used to circulate the capacitor current in this circuit.

2.3 Modulation strategy

There are three types of pulse width modulation (PWM): carrier wave PWM, selective harmonic eliminated PWM (SHE-PWM) and space-vector PWM (SV-PWM). The SHE-PWM can minimize the switching frequency, lowering switching losses and increasing the dc voltage usage. However, it is difficult to execute. The SV-PWM approach is appropriate for inverters with three to five voltage steps. This is not suited for inverters that deliver more than five voltage steps due to its intricacy.

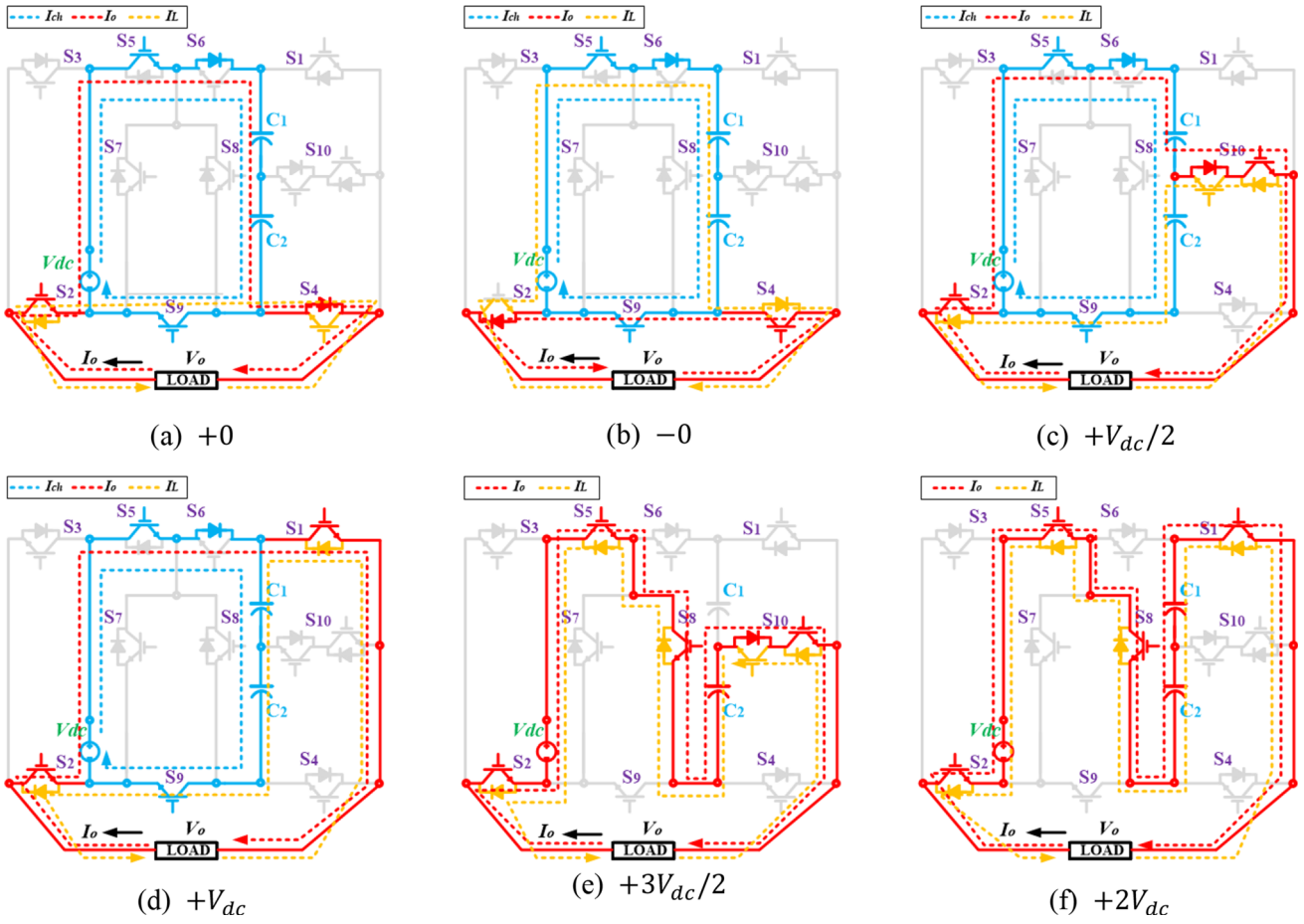


Fig. 2 Various modes of action and current direction

Table 2 Current stress of all semiconductor switches

Voltage levels	Switches in half H-bridge circuit				Switches						Capacitors	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	C_1	C_2
$+2V_{dc}$	I_o	I_o	0	0	I_o	0	0	I_o	0	0	DS	DS
$+3V_{dc}/2$	0	I_o	0	0	I_o	0	0	I_o	0	I_o	NC	DS
$+V_{dc}$	I_o	I_o	0	0	I	I	0	0	I	0	CH	CH
$+V_{dc}/2$	0	I_o	0	0	I	I	0	0	I	I_o	CH	CH
+0	0	I_o	0	I_o	I	I	0	0	I	0	CH	CH
−0	0	I_o	0	I_o	I	I	0	0	I	0	CH	CH
$-V_{dc}/2$	0	0	I_o	0	I	I	0	0	I	I_o	CH	CH
$-V_{dc}$	0	0	I_o	I_o	I	I	0	0	I	0	CH	CH
$-3V_{dc}/2$	0	0	I_o	0	0	I_o	I_o	0	0	I_o	DS	NC
$-2V_{dc}$	0	0	I_o	I_o	0	I_o	I_o	0	0	0	DS	DS

$I = I_o + I_{ch}$

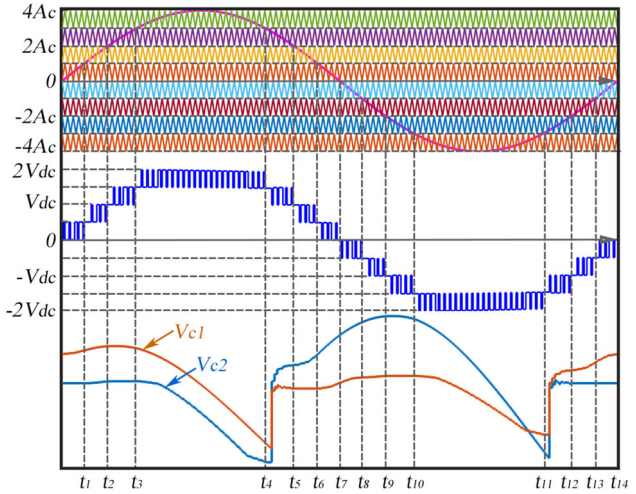


Fig. 3 Modulation strategy and capacitor voltage in one cycle fundamental frequency

In this study, the phase disposition PWM (PD-PWM) is used to create the controlling signals for all switching devices form of carrier signal PWM. This approach has the advantage of being simple to implement, decreasing the intricacy of the driver circuit significantly. To create pulses in a nine-level inverter, eight triangular carriers plus and a sinusoidal modulation wave are needed. Various logic combinations of these pulses are governed by the off and on positions of every switch. Figure 3 shows a block representation of the PD-PWM. The magnitude (A_c) and frequency (f_c) of the eight triangular carriers are identical, but their offsets vary. The sinusoidal modulation wave has a magnitude of A_{ref} and a frequency of f_o.

The modulation index is calculated by the magnitude of the carrier and reference waveforms. As a result, the modulation index M_{i} can be written by

$$M_i = \frac{A_{\text{ref}}}{4A_c} \tag{1}$$

when M_i varies, and the suggested inverter can alter its output appropriately. Table 2 shows the link between various M_i values and output levels.

2.4 Design of voltage balancing capacitors

In switched-capacitor-based MLIs, capacitors serve a critical role in power distribution. Their voltage fluctuations should be kept to a manageable level. Capacitor voltage ripple is related to its capacitance, the weight of the load and the time it takes to discharge it. Reduced voltage ripple may enhance output voltage quality, minimize ripple loss and increase inverter efficiency.

It is required to understand a capacitor's maximum discharge quantity to calculate its capacitance. Figure 3 shows that whenever the output voltage is $(3V_{\text{dc}}/2)$ and $2V_{\text{dc}}$, the capacitor C_2 is discharged. As a result, C_2's maximum discharge quantity is equal to the total of C_2's discharge quantities throughout the three t_2–t_3, t_3–t_4 and t_4–t_5 periods. The instants t_i ($i = 1, 2, 3, 4, 5$) are the points at which the sine and triangle waves intersect and they can be determined using the following equations:

$$t_1 = \frac{\arcsin\left(\frac{1}{4Mi}\right)}{2\pi f_o}, \tag{2}$$

$$t_2 = \frac{\arcsin\left(\frac{1}{2Mi}\right)}{2\pi f_o}, \tag{3}$$

$$t_3 = \frac{\arcsin\left(\frac{3}{4Mi}\right)}{2\pi f_o}, \tag{4}$$

$$t_4 = \frac{\pi - \arcsin\left(\frac{3}{4Mi}\right)}{2\pi f_o} \tag{5}$$

$$t_5 = \frac{\pi - \arcsin\left(\frac{1}{2Mi}\right)}{2\pi f_o} \tag{6}$$

$$t_6 = \frac{\pi - \arcsin\left(\frac{1}{4Mi}\right)}{2\pi f_o}, \tag{7}$$

$$t_7 = \frac{\pi}{2\pi f_o} \tag{8}$$

In 1 (2)–(8), M denotes the modulation index (in this case, $M_i = 0.9$) and f_o is the output frequency. The capacitor's discharge amount from t_1 to t_3 can be computed using the following formula:

$$\Delta Q_1 = \int_{t_2}^{t_3} I_o \sin(2\pi f_o t) d_t \tag{9}$$

where ΔQ_1 is the discharge amount over the time interval t_2 to t_3 and I_o denotes the output current. The discharge amount ΔQ_2 during the period t_3 to t_4 can be calculated using the same method:

$$\Delta Q_2 = \int_{t_3}^{t_4} I_o \sin(2\pi f_o t) d_t \tag{10}$$

The parameters in (9) are identical to those in (10). The capacitor's operational status is the same during t_2 to t_3 and t_4–t_5, and the discharge quantity is also identified during the two intervals. As a result, the maximum amount of C_2 that can be discharged is equal to

$$\Delta Q_{C2} = 2\Delta Q_1 + \Delta Q_2 \tag{11}$$

The capacitance may be calculated using the following formula, suppose k is the factor indicating the highest permissible ripple voltage:

$$C_2 \geq \frac{\Delta Q_{C2}}{kV_{C2}}, \tag{12}$$

where V_{C2} is the rated voltage of the capacitor of C_2.

Voltage ripples of two capacitors are the same when the symmetrical properties of the operating states of C_1 and C_2 in the positive and negative half-cycles are considered. Thus, C_2 is used as an example. The greatest continuous discharge quantity of C_2 is ΔQ_{C2} as may be observed from (11). As a result, the voltage ripple of C_2 could be calculated as:

$$\Delta V_{C2} \geq \frac{\Delta Q_{C2}}{C_2}, \tag{13}$$

where ΔV_{C2} is the voltage ripple of capacitor C_2. As shown in (11) by selecting the appropriate capacitance, the ripple can be kept within a tolerable range.

3 Power losses analysis

Three types of losses are considered in switched-capacitor inverters which contain the capacitor ripple losses (P_{rip}), conduction losses (P_{con}) and switching losses (P_{sw}).

3.1 Capacitor ripple losses

The voltage fluctuation of the capacitors produces (P_{rip}). Owing to the symmetrical functioning states of the two capacitors, C_2 is still used as an example. The voltage ripple of C_2 is ΔV_{C2} as indicated in (13); hence, the P can be computed as follows:

$$P_{\text{rip}} = f_o C_2 \Delta V_{C_2}^2 \tag{14}$$

Further computation can be made as follows:

$$P_{\text{rip}} = f_o \frac{Q_{C2}^2}{C_2}. \tag{15}$$

3.2 Conduction losses

The parasitic characteristics of devices are responsible for inverter conduction losses, such as the switch's on-state resistance (r_s) and each capacitor's equivalent series resistance (R_c).

The equivalent circuit for load supply is shown in Fig. 5. In Fig. 4, r_{eq}, R_o and V_o are equivalent parasitic resistance, load resistance and output voltage, respectively. Table 3 shows the

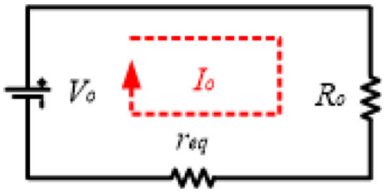


Fig. 4 Load supply equivalent circuit

Table 3 Three working modes' equivalent parameters

Level	V_o	r_{eq}
Zero	0	$4r_s$
One	$V_{\text{dc}}/2$	$3r_s$
Two	V_{dc}	$4r_s$
Three	$3V_{\text{dc}}/2$	$R_c + 4r_s$
Four	$2V_{\text{dc}}$	$2R_c + 4r_s$

corresponding parameters in the four operating modes of the positive half cycle.

The output voltage level varies between 0 and $V_{\text{dc}}/2$ in the period of [0, t_1] as shown in Fig. 3. As a result, the power losses period [0, t_1] can be computed using the formula:

$$P_{0\&0.5V\text{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times \left[(3r_s) \frac{A_{\text{ref}} \sin(2\pi f_o t)}{A_c} + 4r_s \left(1 - \frac{A_{\text{ref}} \sin(2\pi f_o t)}{A_c} \right) \right] dt \tag{16}$$

In the same approach, the power losses of the additional three operating modes can be calculated.

$$P_{0.5\&V\text{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times \left[(4r_s) \frac{A_{\text{ref}} \sin(2\pi f_o t) - A_c}{A_c} + 3r_s \left(1 - \frac{A_{\text{ref}} \sin(2\pi f_o t) - A_c}{A_c} \right) \right] dt. \tag{17}$$

$$P_{V\text{dc}\&1.5V\text{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times \left[(R_c + 4r_s) \frac{A_{\text{ref}} sin(2\pi f_o t) - A_c}{A_c} + 4r_s \left(1 - \frac{A_{\text{ref}} \sin(2\pi f_o t) - A_c}{A_c} \right) \right] dt. \tag{18}$$

Table 4 MVS of each switch in the inverter proposed

Switches	$S_1 - S_9$	S_{10}
MVS	V_{dc}	$\frac{V_{\mathrm{dc}}}{2} + \frac{V_{\mathrm{dc}}}{2}$

$$P_{1.5V\mathrm{dc}\&2V\mathrm{dc}} = \int_0^{t_1} [I_o \sin(2\pi f_o t)]^2 \times \left[\begin{array}{c} (2R_c + 4r_s)\frac{A_{\mathrm{ref}}\sin(2\pi f_o t) - A_c}{A_c} + (R_c + 4r_s) \\ \left(1 - \frac{A_{\mathrm{ref}}\sin(2\pi f_o t) - A_c}{A_c}\right) \end{array} \right] dt. \tag{19}$$

As a result, the P_{con} can be written as:

$$P_{\mathrm{con}} = 5(P_{0\&0.5V\mathrm{dc}} + P_{0.5\&V\mathrm{dc}} + P_{V\mathrm{dc}\&1.5V\mathrm{dc}} + P_{1.5V\mathrm{dc}\&2V\mathrm{dc}}) \tag{20}$$

3.3 Switching losses

The discharging and charging operations of the parasitic capacitor C_s in the switches can be used to quantify switching losses. The parasitic capacitor is supposed to have a linear capacitance. The parasitic capacitor's voltage is progressively charged to V_s when the switch is turned off, where V_s is the MVS of the switches, and V_s is reported in Table 4 for each switch.

As a result, the P_{sw} can be determined using the following formula:

$$P_{\mathrm{sw}} = C_s V_s^2 f_s, \tag{21}$$

where f_s is the switching frequency of the switches, which may be found in the following formula

$$f_s = N_s f_o, \tag{22}$$

N_s is the number of switching transitions in a single period of the reference waveform.

The switches are periodically turned on or off in the appropriate periods, as shown in Fig. 3. If the switch operates for the entire span, the N of every switch could be calculated approximately as the ratio of f_c and f_o. On the other hand, the suggested inverter switches will operate at specific intervals.

As a result, each switch's N_s can be determined:

$$N_s = \frac{t_s f_c}{T_s f_o}, \tag{23}$$

where t_s denote the switch's functioning duration and Figs. 2 and 3 can be used to get it. T_s is the duration of a single cycle. As a result, P can be determined using the following formula:

$$P_{\mathrm{sw}} = 50 \sum_{i=1}^{14} C_{si} V_{si}^2 t_{si} f_c. \tag{24}$$

In summary, the proposed inverter's efficiency can be determined as follows:

$$\eta = \frac{P_o}{P_o + P_{\mathrm{rip}} + P_{\mathrm{con}} + P_{\mathrm{sw}}}, \tag{25}$$

where η and P_o denote the proposed inverter's efficiency and output power.

The above losses can be calculated mathematically at varying output powers. It is important to remember that r_s, R_c, f_c, f_o and C_s are taken into account at 4 mΩ, 50 mΩ, 50 Hz, 5 kHz and 400 pF, respectively, for the loss estimates. Figure 5a depicts the proposed nine-level inverter's theoretical efficiency. The three forms of losses can be calculated using a 120 V_{dc} supply and a 60 Ω + 100 mH load as shown in Fig. 5b follows: $P_{\mathrm{rip}} = 0.43$ W, $P_{\mathrm{con}} = 0.12$ W and $P_{\mathrm{sw}} = 0.3$ W. The proportion of the three categories of losses is shown in Fig. 5c.

4 Horizontal extension topology

The suggested nine level can be structurally extended to provide a higher number of voltage levels. Figure 6 shows the horizontal extension topology.

The cells extend to the first cell, then to the second and so on until the Nth cell is reached. Except for the half H-bridge and switch S_{10}, every cell in the horizontal extension (HE) has the same structure up to the Nth cell. In the 1st cell, the switches are named S_{11}, S_{61}, S_{71}, $S_{81}$and S_{91} and capacitors C_{11} and C_{21}. Similarly, for the 2nd cell, the switches are S_{52}, S_{62}, S_{72}, S_{82} and S_{92} and capacitors C_{11} and C_{21}. Such arrangement can be expanded up to Nth cell. Here the capacitors are linked parallel and thus boost the voltage levels of an inverter. To bring boosting the operation of HE topology, the steps mentioned below are used.

For double boosting, Nth cell's capacitors are discharged while the remaining cell's capacitors, i.e., [1^{st} *to* $(N-1)$th] are charging. For triple boosting, Nth and $(N-1)$th cell's capacitors are discharged while other cell's [1st *to* $(N-2)$th] capacitors are charged at the same time and continuously. Similarly, the capacitors are discharged gradually from higher-order to lower-order cells to increase voltage levels step by step. Table 4 portrays the proposed HE switching sequence corresponding to the circuit structure depicted in Fig. 6. Further, Table 5 formulates the states of the capacitors such as charging, discharging and "NO" change to show the

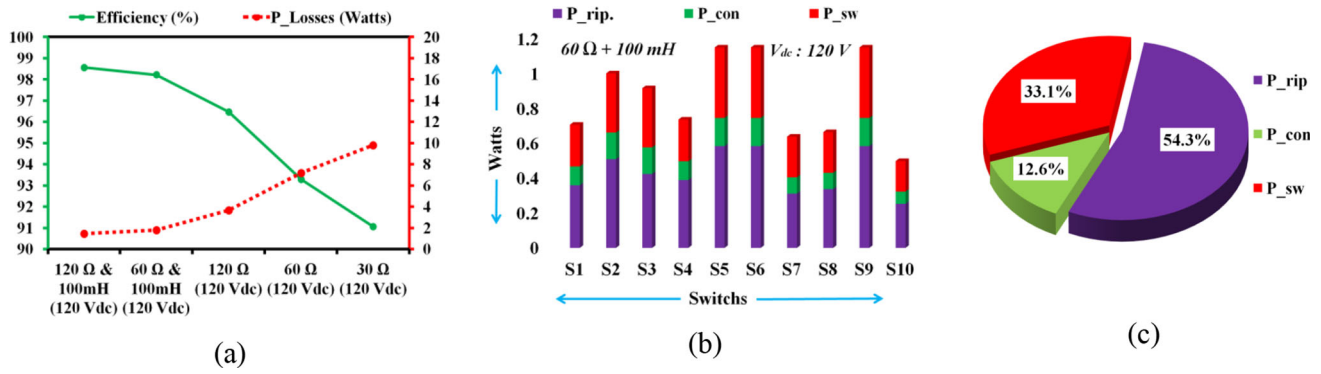


Fig. 5 Theoretical efficiency and losses on 60Ω + 100 mH load. **a** Efficiency at various power. **b** Ripple, conduction and switching losses. **c** Three types of losses

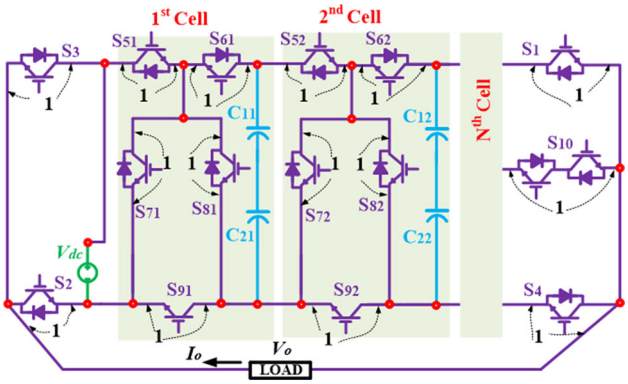


Fig. 6 Horizontal extension of the proposed topology

boost voltage. In addition, the generalized Eqs. (26)–(31) are given to construct the proposed nine-level S^3CMLI (HE).

$$N_{\mathrm{IS}} = 4n + 2(\mathrm{Included}S_9) \tag{26}$$

$$N_{\mathrm{DC}} = 4n + 1(\mathrm{Included}S_9) \tag{27}$$

$$N_{\mathrm{VL}} = 4(n+1) \tag{28}$$

$$N_C = 2(n-1) \tag{29}$$

$$V_{\mathrm{MOV}} = nV_{\mathrm{dc}} \tag{30}$$

$$V_{\mathrm{dc}} : V_o = 1 : n \tag{31}$$

where N_{IS} represents the number of power electronics switches, N_{DC} represents the number of driver circuits, $\mathrm{N_{VL}}$ represents the number of voltage levels, N_C represents the number of flying capacitors, V_{MOV} represents maximum output voltage and n represents the maximum voltage gain generated by the N^{th} cell with a single source. At this point, the inverter must satisfy the condition $n \geq 2$.

5 Comparison of the proposed topology with others

Table 5 shows the comparison of the proposed topology. Here N_{IS} is the number of power electronic switches, N_{VL} is the number of different voltage levels, Nv_{dc} is the number of input, $N_C$is the number of flying capacitors, N_{SC} is the number of the switches in the conduction path, $V_C(V)$ is voltage across the capacitors, $V_{\mathrm{TS}}(V)$ is total standing voltage of the inverter, $V_{\mathrm{BV}}(V)$ is maximum blocking voltage on switches, N_{CD} is number of active devices including diodes, $V_{\mathrm{MOV}}(V)$ is maximum output voltage, $N_{\mathrm{comp.}}(N_{\mathrm{IS}} + N_D)$ is the number of components, $N_{\mathrm{ch}}$is the number of devices in the charging loop and $S = V_{\mathrm{TS}}(V)/V_{\mathrm{MOV}}(V)$, the ratio of the number of times discharging and charging—DC/C minimum value).

5.1 Comparison of the number of active devices (N_{CD}) and standing voltage per unit (S)

For the nine-level output, the proposed topology takes ten switches that are less than the configurations described in the references [3–5, 11, 14, 22, 23].

Table 6 shows that the number of conduction switches in the suggested topology is lower than any of the other topologies. As a result, conduction losses are minimized due to the lesser switch count. Furthermore, with a gain of two, the nine-level architecture utilizes just two capacitors. However, the topologies described in the references [5, 9, 14] employ three capacitors to provide the same voltage gain. Due to these reduced active switches, the power consumption is less, and therefore, the cost of switches becomes low when compared to other topologies. It is one of the notable advantages of the suggested topologies. As compared to other circuits, the nine-level topology is the best in overall efficiency, low voltage stress on the switch and the least amount of loss.

Another significant parameter for switched-capacitor-based topologies is the number of devices in the charging

Table 5 Common switching pattern of the horizontal extension topology

Voltage levels	Switches in H-half bridge circuit	"ON" state switches						States of capacitors	
	S_1, S_2, S_3, S_4	S_{51}, S_{52}	S_{61}, S_{62}	S_{71}, S_{72}	S_{81}, S_{82}	S_9	S_{10}	C_{11}, C_{12}	C_{21}, C_{22}
$+(n+1)V_{dc}$	S_1,S_2	–	–	–	S_{81}, S_{82}, …S_{8n}	–	–	C_{11d}, C_{12d}, …C_{1nd}	C_{21d}, C_{22d}, …C_{2nd}
…	…	…	…	…	…	…	…	…	…
$+3V_{dc}$	S_1,S_2	S_{51}, … $S_{5(n-2)}$	S_{61}, … $S_{6(n-2)}$	–	$S_{8(n-1)}$, S_{8n}	S_{91}, … $S_{9(n-2)}$	–	C_{11}, C_{12}, …$C_{1(n-1)d}$, C_{1nd}	C_{21}, C_{22}, …$C_{2(n-1)d}$, C_{2nd}
$+5V_{dc}/2$	S_2	S_{51}, … $S_{5(n-2)}$	S_{61}, … $S_{6(n-2)}$	–	$S_{8(n-1)}$, S_{8n}	S_{91}, … $S_{9(n-2)}$	S_{10}	C_{11}, C_{12}, …$C_{1(n-1)d}$, C_{1n-}	C_{21}, C_{22}, …$C_{2(n-1)d}$, C_{2nd}
$+2V_{dc}$	S_1,S_2	S_{51}, … $S_{5(n-1)}$	S_{61}, … $S_{6(n-1)}$	–	S_{8n}	S_{91}, … $S_{9(n-1)}$	–	C_{11}, C_{12}, …C_{1nd}	C_{21}, C_{22}, …C_{2nd}
$+3V_{dc}/2$	S_2	S_{51}, $S_{5(n-1)}$	S_{61}, … $S_{6(n-1)}$	–	S_{8n}	S_{91}, … $S_{9(n-1)}$	S_{10}	C_{11}, C_{12}, …C_{1n-}	C_{21}, C_{22}, …C_{2nd}
$+V_{dc}$	S_1,S_2	$S_{51}S_{52}$, …S_{5n}	S_{61}, S_{62}, …S_{6n}	–	–	S_{91},S_{92}, …S_{9n}	–	C_{11}, C_{12}, …C_{1n}	C_{21}, C_{22}, …C_{2n}
$+V_{dc}/2$	S_2	$S_{51}S_{52}$, …S_{5n}	S_{61}, S_{62}, …S_{6n}	–	–	S_{91}, S_{92}, …S_{9n}	S_{10}	C_{11}, C_{12}, …C_{1n}	C_{21}, C_{22}, …C_{2n}
0	S_2, S_4	$S_{51}S_{52}$, …S_{5n}	S_{61}, S_{62}, …S_{6n}	–	–	S_{91}, S_{92}, …S_{9n}	—	C_{11}, C_{12}, …C_{1n}	C_{21}, C_{22}, …C_{2n}
$-V_{dc}/2$	S_3	$S_{51}S_{52}$, …S_{5n}	S_{61}, S_{62}, …S_{6n}	–	–	S_{91},S_{92}, …S_{9n}	S_{10}	C_{11}, C_{12}, …C_{1n}	C_{21}, C_{22}, …C_{2n}
…	…	…	…	…	…	…	…	…	…
$-(n+1)V_{dc}$	S_3,S_4	–	–	S_{71}, S_{72}, …S_{7n}	–	–	–	C_{11d},C_{12d}, …C_{1nd}	C_{21d},C_{22d}, …C_{2nd}

– -: "OFF" state; C_{1x} and C_{2x}: state of charging; C_{1xd} and C_{2xd}: state of discharging; C_{1x-} and C_{2x-}: state of "NO" Change where $x = 1, 2 \ldots n$

Table 6 Comparison of the number of active devices (N_{CD}) and standing voltages per unit of topologies

Ref	N_{VL}	N_{IS}	N_D	Nv_{dc}	N_C	V_C	V_{BV}	N_{CD}	S	GA	DC/C
[3]	9	10	3	1	4	$V_{dc}/2$	V_{dc}	7	5.0	1	3
[4]	9	12	0	1	3	V_{dc}	$2V_{dc}$	6	6	4	3
[5]	9	12	0	1	3	$V_{dc}/2$	V_{dc}	6	5.5	2	1
[14]	9	12	0	1	4	$V_{dc}/4$	V_{dc}	6	5.5	1	4
[9]	9	10	1	1	2	$V_{dc}/2$	$2V_{dc}$	6	5.7	2	3
[17]	9	9	3	1	3	V_{dc}	$2V_{dc}$	6	6.0	4	3
[11]	9	11	0	1	3	$V_{dc}/2$	$2V_{dc}$	7	5.0	2	2
[18]	9	10	0	1	4	V_{dc}	$4V_{dc}$	5	6.2	4	1
[22]	9	12	0	1	2	$V_{dc}/2$	V_{dc}	7	5.5	2	1
[23]	9	11	0	1	2	$V_{dc}/2$	V_{dc}	6	5.5	2	1
[25]	9	8	2	1	3	$V_{dc}/2$		5	5.5	2	2
Prop. Topology	9	11	0	1	2	$V_{dc}/2$	$2V_{dc}$	4	5.0	2	2
P_(HE)	13	14	0	1	4	$V_{dc}/2$	$2V_{dc}$	5	5.0	3	2

NA Not Available; *Prop*. Proposed; *P_ (HE)* Horizontal Extension; GA Gain

Table 7 Comparison of the cost function (CF) for nine-level inverter

Ref	$N_{\text{comp.}}$ ($N_{IS} + N_D$)	N_C	N_{ch}	S	N_{SC}					$\text{CF}_{(\text{Nine})}$(value of α, β)	
					± 1	± 2	± 3	± 4	N_{SC} (avg)	0.5, 0.5	1.0, 1.0
[4]	12	3	3	6	6	6	6	6	6.0	24.0	30.0
[5]	13	3	4	5.5	5	6	5	6	5.5	25.5	31.0
[14]	12	4	4	5.5	3	6	4	5	4.2	24.8	29.7
[9]	12	2	5	5.75	4	5	3	4	4.0	23.9	28.8
[17]	12	3	3	6.0	6	5	5	6	5.5	23.7	29.5
[11]	11	3	4	5.0	4	6	5	5	5.0	23.0	28.0
[22]	12	2	2	5.5	5	5	4	4	4.5	21.0	26.0
[23]	11	2	5	5.5	6	6	6	5	5.9	23.7	29.8
[25]	10	3	4	5.5	5	5	5	5	5.0	22.3	27.5
Prop. Topology	11	2	3	5.0	4	4	4	4	4.0	20.5	25.0

Table 8 Comparison with voltage levels and low-voltage-stress SCMLIs

Items	[14]	[20]	[21]	[22]	[9]	[25]	Proposed
Levels	7	7	7	7	11	7	11
Switches	10	10	10	10	11	10	11
Diodes	0	0	0	1	0	0	0
Capacitors	4	3	4	3	3	2	2
MVS	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Voltage boosting	No	No	No	No	Yes	Yes	Yes
Q_m	$6Q_m$	$5Q_m$	Q_m	$5Q_m$	$4Q_m$	$4Q_m$	$4Q_m$

loop (N_{ch}). To manage the capacitor's charging current, the devices in the charging loop must have a greater current rating.

The proposed topology has only two higher-current-rated devices that are needed, whereas the topologies presented in the all references, except [5], require a greater number of devices in the charging loop. The number of switches in the conduction path (N_{SC}) indicates the total number of conduction switches at each voltage level. The ratio of total standing voltage to the maximum output voltage (S) is also lower in comparison with other MLI except [11]; however, this design needs a higher number of components and capacitors.

5.2 Comparison of cost function (*CF*)

The cost function is utilized to calculate the overall inverter cost. It is depends on the count of switches, capacitor, switches in the capacitor charging loop, conduction switches in each level and voltage stress per level on the inverter.

A cost function $\text{CF}_{(\text{Nine})}$ has been specified by Eq. (32) for further analysis.

$$\text{CF}_{(\text{Nine})} = N_{\text{comp.}} + N_C + N_{\text{ch}} + \alpha S + \beta N_{\text{SC}}(\text{avg}) \tag{32}$$

Table 7 shows the multilevel inverter's projected cost function (CF). In addition, CF is calculated for various combinations of α and β values. Here, α and β are the weight coefficients of S and $N_{\text{SC}}(\text{avg})$, respectively. When compared to the other described inverter, the proposed topology has a lower $\text{CF}_{(\text{Nine})}$ value. Further, the suggested topology has the fewest numbers of conducting switches at each level compared to other topologies.

5.3 Comparison with voltage levels and low-voltage-stress SCMLIs

Table 8 compares the suggested inverter to the hybrid MLIs that was recently suggested. The comparison was made assuming that almost all inverters have the same MVS across each switch.

Table 9 Comparison of the cost function for 13-level inverter

Ref	N_{VL}	N_{IS}	N_{DR}	N_D	N_C	V_{TS}	T_{CV}	$CF_{(13\_Level)}$	GA
[14]	13	13	13	2	3	32	6	5.3	6
[6]	13	13	13	2	3	31	5	5.2	6
[7]	13	14	14	1	3	33	4	5.3	6
[17]	13	10	3	4	4	33	6	4.6	6
[18]	13	13	13	2	3	33	5	5.3	6
[24]	13	12	12	0	4	18	8	4.2	3
P_(HE)	13	16	14	0	3*	16	3	4.0	3

3* = (1 + 2)—1st cell's two capacitors connected in series consider as single capacitor. GA—gain

These hybrid inverters can keep the voltage burden on the switches to a minimum, which is a quality of the suggested inverter as well. In comparison with the suggested inverter, the hybrid MLIs use additional capacitors except for recent topology however, that recent topology has seven levels only.

Furthermore, the majority of them cannot raise the input voltage. The suggested inverter is better concerning maximum discharge capacity and the number of capacitors, as shown by the Q_m of these inverters. As a result, the suggested inverter has the benefit of having a lower capacitance. Table 7 shows that the suggested inverter addresses the aforementioned flaws and provides superior overall performance.

5.4 Comparison of cost function (CF) for 13-level inverter

The extension of the proposed topology operates with six active switches to produce the triple boost 13-level voltages with the total standing voltage of sixteen. The proposed topology has low voltage stress compared to other topologies shown in Table 8. A cost function $CF_{(13\_Level)}$ has been specified by Eq. (33).

$$CF_{(13\_Level)} = (N_{IS} + N_{DR} + N_D + N_C + V_{TS} + T_{CV})/13 \tag{33}$$

where N_{DR}—number of driver circuits and T_{CV}—total capacitors voltage.

Table 9 shows the cost factor $CF_{(13\_Level)}$ for a 13-level inverter is low when compared to other topologies. In addition, the total capacitor voltage (T_{CV}) is low for the extension topology of the proposed topology.

Table 10 Simulation parameters

Parameters	Values
Input DC supply (V_{dc})	120 V
frequency (f_o)	50 Hz
Carrier frequency (f_c)	2.5 kHz
Capacitor (C_1, C_2)	3400 μF, 4700 μF
Loads	60Ω + 100 mH

Table 11 Experimental parameters

Parameters	Values
Input DC supply (V_{dc})	120 V
frequency (f_o)	50 Hz
Switching frequency	2.5 kHz
Capacitor (C_1, C_2)	3400 μF and 4700 μF, r_c = 0.124 Ω
Loads	60Ω + 100 mH, 120Ω
Conduction resistance of switches $S_1 - S_4$; S_7&S_8	r_H and r_f = 0.032 Ω
Conduction resistance of switches S_9, S_6&S_9	r_s = 0.0092 Ω
Conduction resistance of switches S_{10}	r_l = 0.0422 Ω

6 Simulation verification and experimental validation

6.1 Simulations

To test the performance of the proposed inverter, a simulation of a nine-level inverter is created in MATLAB/Simulink. Table 11 lists the parameters used in the simulations. The simulation results are depicted in Fig. 7 that the inverter generates PWM waves with nine levels and the current lags the voltage.

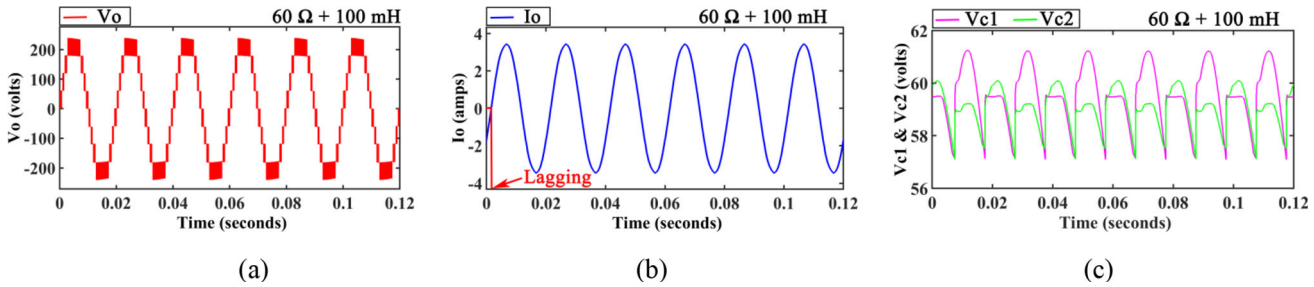


Fig. 7 Simulation results for output **a** voltage, **b** current and **c** capacitor voltage

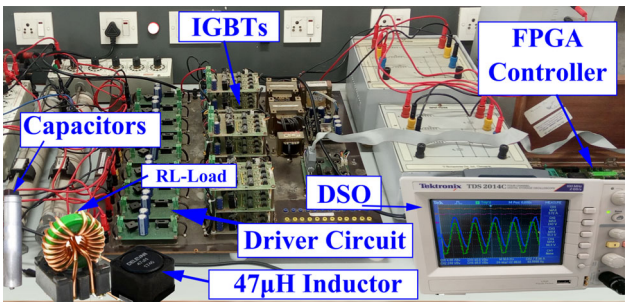


Fig. 8 Experimental apparatus

Table 12 Relation between output levels and modulation index M_i

M_i	Output level
$0 < M_i < 1/4$	3
$1/4 < M_i < 1/2$	5
$1/2 < M_i < 3/4$	7
$3/4 < M_i < 1$	9

6.2 Steady-state analysis

To show the suggested inverter's viability, a nine-level prototype was developed to test its steady-state and dynamic performance. The parameters of the prototype Fig. 8 as well as the experimental apparatus are listed in Table 11. The voltage and current waveforms are analyzed as well as the voltage waveforms of the two capacitors and the voltage stress of switches.

The voltage and current waveforms are analyzed as well as the voltage waveforms of the two capacitors and the voltage stress of switches. An experiment was done in an RL load (60Ω + 100) to assess the suggested inverter's steady-state effectiveness.

The waveforms of output voltage, current and capacitor voltage are shown in Fig. 9a under 50 Hz. Each stage has a voltage of 60 V with a maximum output voltage of 240 V. The boost gain of two is reached since the input source voltage is 120 V.

Figure 9a and b depicts the steady-state capacitor voltages. The two capacitors appear to be self-balancing through modest voltage ripples. It is compatible with the capacitor's voltage balancing analysis. Under the same RL—load conditions, increase the frequency value to 200 Hz. Figure 9b depicts the results. The output reduced magnitude current lags behind the voltage, demonstrating the capacity to supply inductive loads under high frequency.

Figure 10 depicts the voltage stress on the switches. A benefit of the proposed inverter is that the MVS of the switches is restricted to the input power voltage V_{dc}. A total of 11 switches are utilized in the proposed nine-level inverter. The voltage stress of S_1 to S_9 is V_{dc} and $V_{dc}/2$ of S_{10}(back to back connected).

The current stress of the power switches was tested, and the results are presented in Fig. 11

Because of the capacitors' small voltage changes, all switch current stress is kept to a minimum.

The switches in the capacitor charging circuit are subjected to a maximum current stress of about 4.3 A

6.3 Dynamic analysis

An effective inverter should be flexible to changing operating conditions such as load fluctuations, input voltage fluctuations, modulation wave frequency and amplitude fluctuations and so on. The inverter's performance in dynamic conditions was further evaluated in the following trials. Figure 15 depicts the output voltage as the modulation wave's amplitude changes. The output voltage changes from nine to seven levels when M_i is changed from 1 to 0.75, as shown in Fig. 12a. The transient procedures are completed quickly, demonstrating the suggested inverter's high dynamic performance. The experimental results are likewise in conformity with the findings of Table 3's analysis.

The proposed inverter can adjust appropriately when the output frequency of the modulation wave varies. As the frequency changes, Fig. 12b illustrates the output voltage, current and capacitor voltage. It is noticed in circumstances where the inverter could transit appropriately with a quick transient reaction (50–200 Hz).

Figure 13a depicts the experimental findings under the situation of a quick shift in load. The load changes from RL load ($60\Omega + 100\ mH$) to a resistance load (120Ω). The output shows that when the load fluctuates, the inverter operates admirably. Capacitors C_1 and C_2 charges and discharges when the dc source voltage changes from 120 V to 100 V processes, which may simulate the solar cell's input voltage sudden variations. The inverter functions healthy with the sudden shift in its input voltage, as shown in Fig. 13b. The test results reveal that the inverter has the strong dynamic response in adjusting to changes in the input voltage and can swiftly establish a new steady state.

6.4 Efficiency analysis

The efficiency against different load conditions at various supply voltages is shown in Fig. 14. Furthermore, the efficiency rises as the input voltage rises when the load power remains constant, as shown in Fig. 14. This is due to the fact that the load current will drop, resulting in lower power losses.

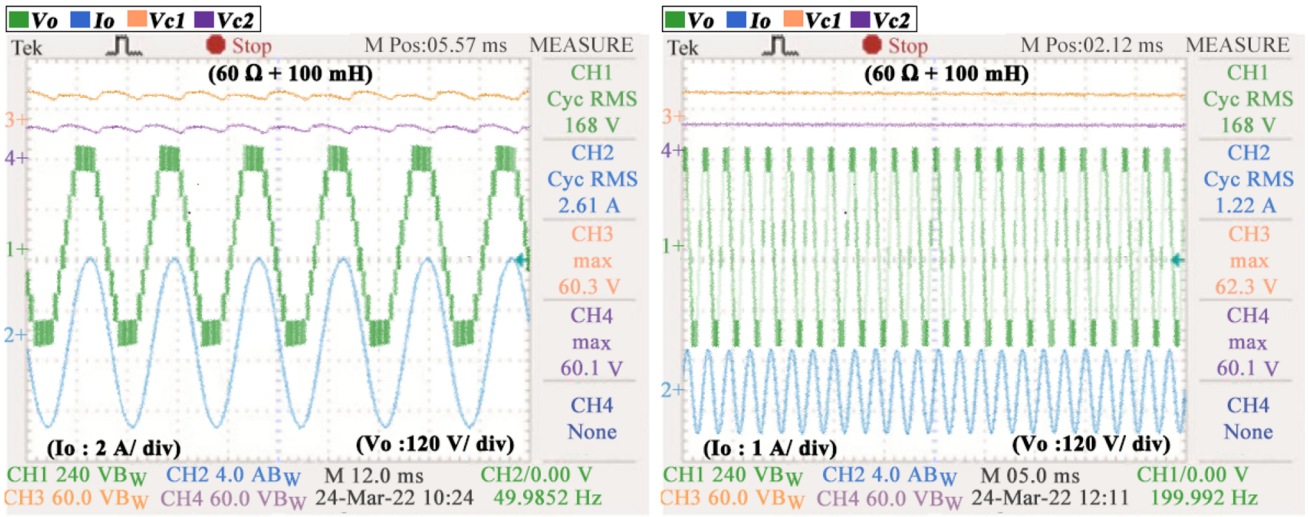


Fig. 9 Steady-state experiment waveforms of output voltage, current and capacitor voltage. **a** Load $60\Omega + 100\ mH$ under 50 Hz. **b** Load $60\Omega + 100\ mH$ under 200 Hz

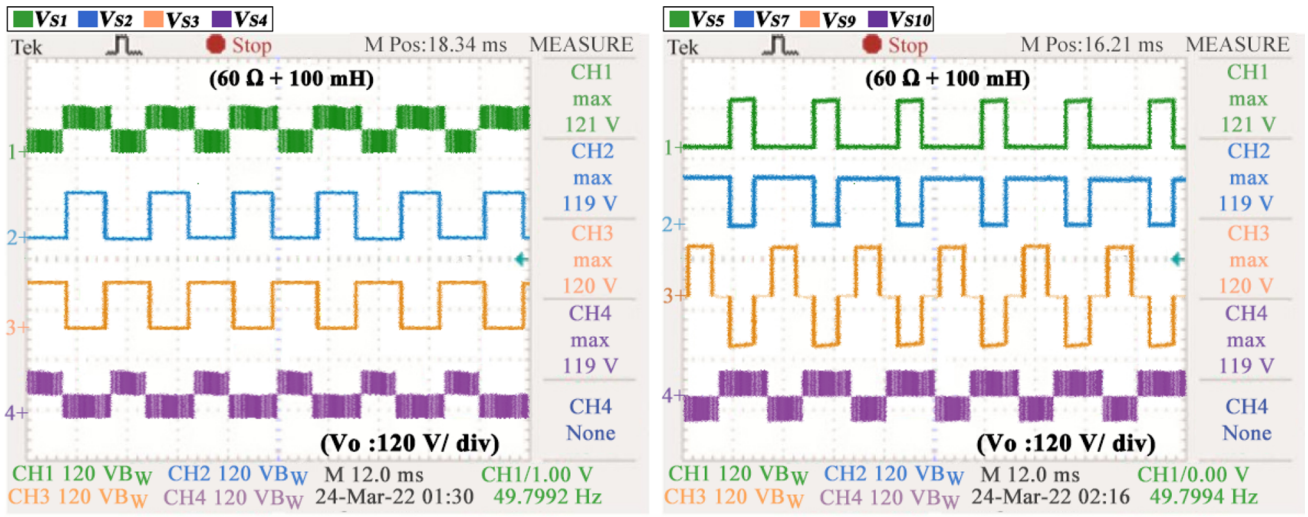


Fig. 10 Voltage stress on switches. **a** S_1, S_2, S_3, S_4, **b** S_5, S_7, S_9, S_{10}

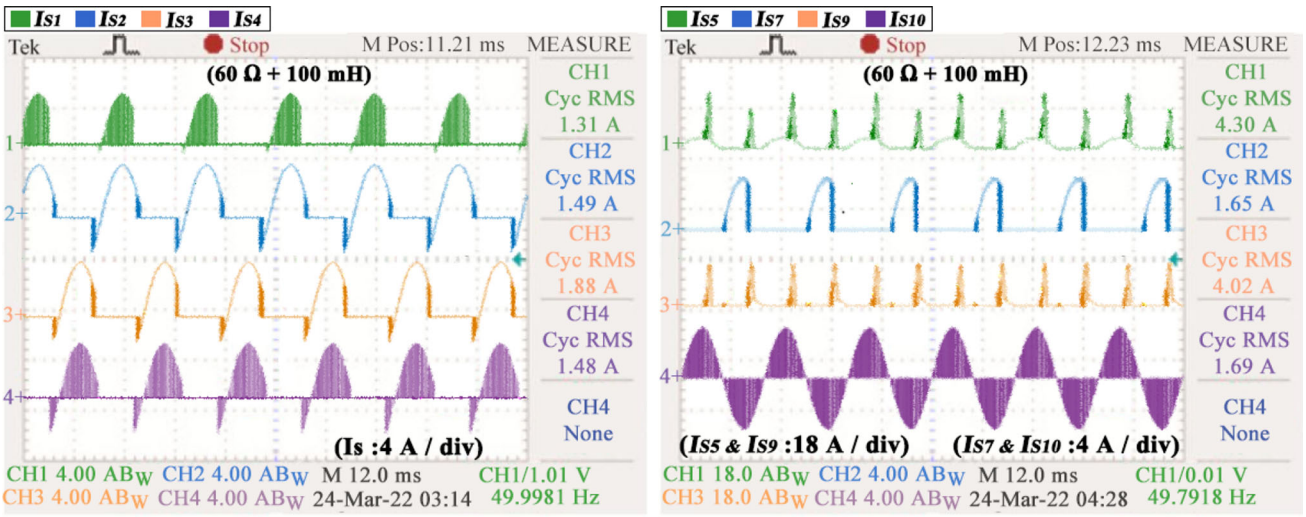


Fig. 11 Current stress on switches. **a** S_1, S_2, S_3, S_4, **b** S_5, S_7, S_9, S_{10}

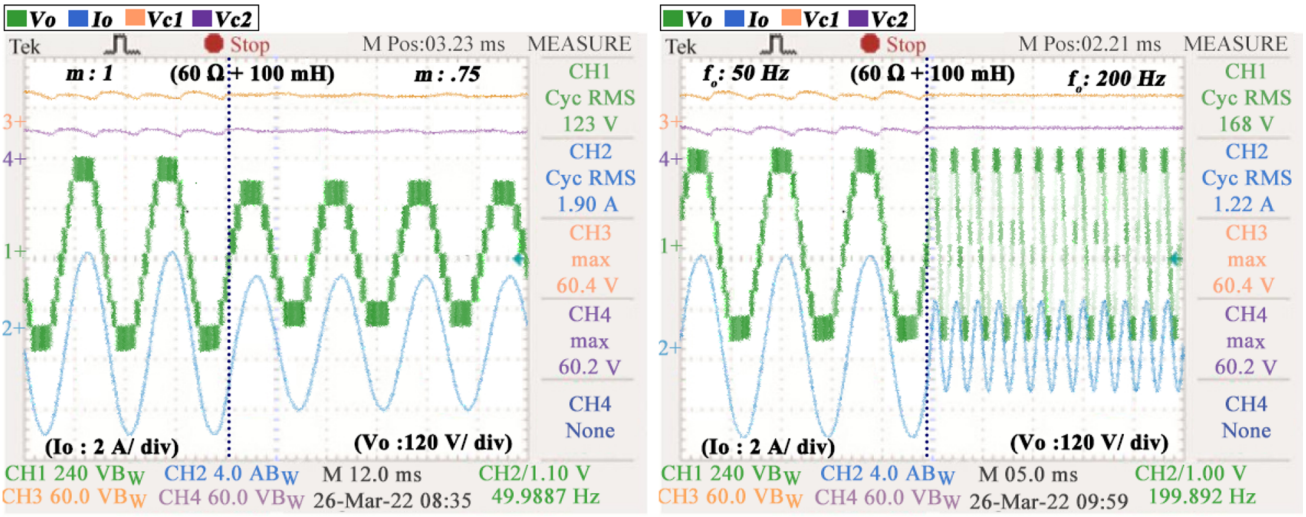
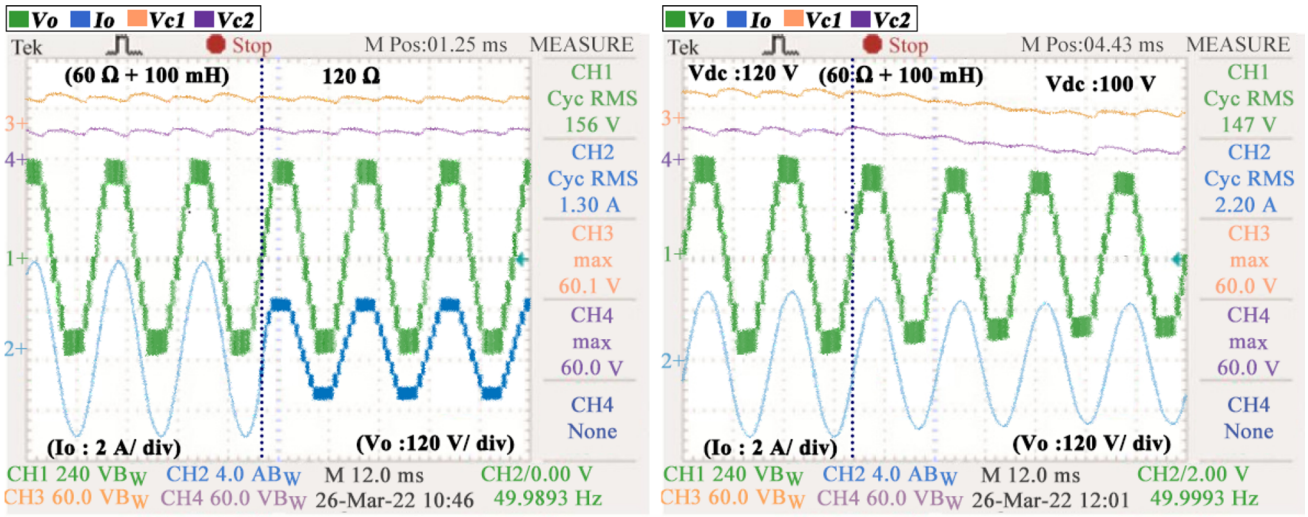


Fig. 12 Dynamic experiment waveforms of output voltage, current and capacitor voltage. **a** Modulation index $M_i\,(or)m$ changes. **b** Output frequency changes

6.5 Discussion

Through simulation verification and experimental validation, the suggested inverter's output voltage boosting, capacitors self-balancing and capacity to provide inductive loads were explored. The experimental results demonstrate that with a 120 V input signal, the output voltage magnitude is 240 V, resulting in a voltage boost of two. The experiment also shows that the capacitor voltages can balance themselves. Furthermore, the capacity to deliver the inductive load is proved through experiments with 60 Ω and 100 mH loads. The suggested inverter has a low MVS when compared to other SCMLIs: All switches' voltage stress does not surpass the input dc voltage. Furthermore, when the inverter is turned on, the working circumstances may vary, for example rapid variations in the resistive/inductive load, input voltage, as well as the magnitude and output frequency of the sinusoidal wave modulation. These situations are also evaluated by dynamic tests, which demonstrate that the suggested inverter can react to dynamics and swiftly stabilize in a new functional state.



(a) (b)

Fig. 13 Dynamic response of output voltage, current and capacitor voltage. **a** Load changes. **b** DC voltage changes

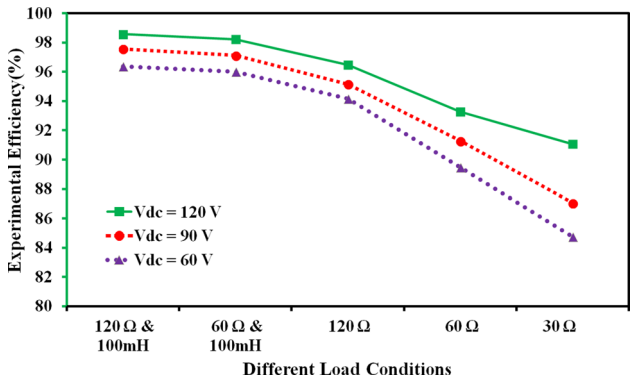


Fig. 14 Efficiency against different load conditions

7 Conclusion

This research proposes a new switched-capacitor multilevel inverter with reduced voltage stress and capacitor voltage self-balancing capability. Only two capacitors are necessary to achieve a nine-level output without impacting the switch count.

This topology has the following outcomes and characteristics: (1) Compared to traditional SCMLIs, the proposed inverter's maximum voltage stress of the switches can be limited to less than the input dc voltage. One of the good aspects that result in the suggested inverter being an appealing solution for medium- and high-voltage photovoltaic (PV) power generation applications is its low voltage stress. (2) A voltage boost gain of two can also be achieved thanks to the low voltage stress. (3) To attain a larger voltage boost gain and higher output level, topology extension approaches have been presented, which are superior in their flexible extensibility and ability to feed inductive loads. (4) The suggested inverter's capacitor voltages can be self-balanced, reducing its management complexity. (5) In each working mode, the bidirectional energy loop ensures the capacity to supply the inductive load.

A nine-level experimental prototype has been used to validate the proposed inverter's properties. The inverter exhibits good performance in both steady-state and dynamic settings, according to the experimental results.

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