



Amelioration of power quality in a solar PV fed grid-connected system using optimization-based selective harmonic elimination

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Abstract

The paper investigates a solar PV fed single phase modular multilevel inverter (MMI) and a modular converter for obtaining constant DC from the PV panels. The proposed inverter structure operates with symmetric and asymmetric DC sources. Switch reduction, harmonic reduction and grid synchronization are the performance parameters considered in the proposed work. To improve the power quality at the output side of the inverter, Selective Harmonic Elimination Technique (SHE) is used. Three different optimization techniques such as genetic algorithm, particle swarm optimization, and, bee colony optimization are implemented to calculate the triggering angles for the switches of MMI. Among the three optimization techniques the particle swarm optimization (PSO) technique gives the best result with reduced THD. Later as an application point of view the proposed MMI is connected to the grid. A closed loop control system having an outer voltage control loop and the inner current control loop is implemented for the Grid Connected System. The proposed topology and the modulation technique is simulated with MATLAB/Simulink. The hardware implementation is carried out with Field Programmable Gate Array (FPGA)-based processor to generate the switching sequences based on the proposed methodologies. The THD value of grid current using the cascaded controller is 2.03%. From the results it is evident that the PSO-based SHE method with the cascaded controller injects sinusoidal current to the grid with less THD and maintains the grid current in phase with the grid voltage at near to unity power factor.

Keywords Modular multilevel inverter · Selective harmonic elimination · Total harmonic distortion

1 Introduction

The demand for electricity is steadily increasing due to the increase in inhabitants and industrial development. Energy generated from natural sources such as coal or gas is not consistent with today's energy demand. Since coal (fossil fuel) is cheaply available, an enormous quantity of electrical energy is generated from fossil fuels. Fossil fuels cause significant damage to the environment by liberating carbon

dioxide and mercury during energy conversion, which leads to global warming [1]. Global warming is estimated to raise the earth's surface temperature from 14 to 18 °C by the end of this century as a result of the greenhouse effect. The power generated by conventional systems needs to be passed on to the end-user on a long-term basic basis, requiring costly, complex infrastructure and exposing the entire system to higher energy loss and safety risks.

In view of fossil fuel price inflation and diminishing public acceptance of these energy sources, photovoltaic (PV) technology [2] has become a truly sensible alternative. The PV has the advantage of converting sunlight directly into electricity and is also well suited for most geographical regions. The solar power system is usually the best choice for most suburban and rural applications as it requires less maintenance, provides noise-less operations due to no moving parts, and occupies less space as rooftops can be used to install solar photovoltaic plates. The PV installations [3] are increasing rapidly, with novel control strategies for suitable operation. The output of RES can be controlled with the ben-

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efits of advanced power electronic converters. The power electronic devices are interfaced with RES for reducing cost, increasing reliability, high efficiency, and power stability. Researchers have focused on renewable energy resources for decades, and numerous power inverters are built to interconnect these technologies into the distribution grid. High voltage power electronic circuits are required in the transmission lines to ensure the delivery of power and power quality. Therefore, power electronic inverters are responsible for performing these conversion tasks efficiently. The growth of global energy demand has led to the emergence of novel topologies of semiconductors and power converters which are capable of supplying all the required power. There is still an ongoing competition to produce semiconductors which can withstand higher voltage and current for efficient systems. Moreover, there has been heavy competition between the use of high-voltage semiconductor devices in traditional power converter topologies with medium voltage devices in modern converter topologies.

In traditional Multilevel inverter (MLI) [4] the switches are being increased to produce high voltages across the output terminals with less harmonic content. Each switch of a traditional MLI needs a gate driver circuit, safety circuit, and heat sink. This makes the traditional MLI costly and bulky. As a result, attempts were made in recent years to reduce the switching devices, and several modular topologies were obtained. In general, MMI (Modular Multilevel Inverter) topologies are classified into two classes, Symmetrical MMI (SMMI) and Asymmetrical MMI (AMMI). The word symmetric means that the magnitude of all the DC inputs used in a circuit are similar. The word asymmetric means that the magnitude of all the DC inputs used in a circuit are unequal. The authors in [5] offered a novel structure of MLI, which produces 27-level of output voltage using 16 switches and 5 DC sources. Fundamental frequency switching strategy is implemented for firing the switches of the 27-level MLI. The authors in [6] dealt with a multicell MLI. It consists of 8 unilateral switches, one bilateral switch and 3 DC sources to generate a 15-level of the output. It consists of a voltage tripler circuit. Nearest Level Control (NLC) modulation technique is implemented for switching the proposed inverter. The authors in [7] developed a MLI with reduced device count. The basic unit of the suggested configuration generates 13 output level with 3 DC power supplies and 8 power switches. A detailed description of the suggested structure to show the advantages of the suggested converter towards the other developed MLI topologies has been carried out. The authors in [8] designed a 7-level inverter with three-H bridges, two bidirectional switches, two capacitors, and one DC source. The proposed structure does not require any auxiliary circuit to produce negative levels. The voltage stress is equally distributed among the switches. SPWM method is implemented for triggering the power switches of the sug-

gested topology. The authors in [9] suggested the MLI using switched capacitor (SC), which generates 13-level using 14 power switches and 6 DC sources. No additional circuit is needed to produce negative voltage levels in the designed structure.

The proposed topology produces the lowest cost function when compared with other capacitor switched MLIs. A novel seven-level MLI with 8 switches and two FC is proposed in [10]. The number of switching elements is reduced in this special arrangement. A simple modulation method is implemented for the suggested structure to reduce the cost and complexity of the control system. The authors in [11] developed a 7-level MLI with nine switching devices. The author built the structure from a switched capacitor and a hybrid MLI structure. The proposed structure does not use H-bridge for producing negative voltage levels. The proposed structure is efficient and costs less. The authors in [12] introduced a 9-level SMLI with 10 power switches and 5 DC sources. The strategy employed is modular and does not include H-bridge for generation of negative levels. SHEPWM technique is used to provide pulses to the proposed MLI. The modulation strategies are used to generate pulses for the switches in the power converter to produce the preferred voltage or current. All the modulation strategies are designed to generate a synthesized staircase wave shape of the voltage on the basis of the reference signal with various voltage and current amplitudes, frequency, and fundamental elements of the steady sinusoidal waveform. Implementing modulation strategies achieve a lower THD with better power quality and also retain controlled DC-link voltages and the RMS output voltage.

To suppress the harmonics produced by the multilevel inverter many modulation schemes were introduced by the researchers in the past few years. Implementing high switching frequency modulation technique for MLI damages the switches by producing thermal loss. Therefore, low switching frequency modulation technique is mostly preferred for harmonic elimination in MLI. In low switching frequency modulation technique, the selective harmonic eliminating pulse-width modulation (SHEPWM) suits best for eliminating the low-order harmonics from inverter output voltage. The authors in [13] implemented the SHE-PWM technique to control the circulating current in the modular multilevel converter. The control technique adjusts the DC component of the circulating current and the stored energy to its reference value. Seventeen switching angles are generated by the PWM technique to optimize the circulating current and harmonics. In [14] the authors presented a 7-level reduced switch multilevel inverter. The author implemented the SPWM and SHE PWM techniques to the proposed structure. By implementing the SPWM technique and SHE PWM technique the THD obtained is 10.02% and 8.35%. From the results obtained it is evident that the SHE PWM technique

reduces the harmonics in the system. In [15] a new solution to substantially limit the harmonics is implemented using the SHE PWM technique. The transcendental optimization equations are translated into algebraic equations with Chebyshev polynomials. The approach proposed is to generalize the Chudnovsky algorithm, requiring rather than removing the modulation of the chosen harmonics. In comparison, the method used to extract the roots of the polynomial enables the algorithm to be applied in real-time applications. The authors in [16] presented the SHE optimization approach in CHB MLIs using Teaching–Learning-Based Optimization (TLBOs). The main aim of SHE is to remove harmonic contents by computing the nonlinear equations and the equations are computed using the TLBO algorithm. The third and fifth harmonics are totally removed from the output using the SHE-TLBO technique. The reduced switch MLIs particularly in renewable energy applications, including photovoltaic systems, have immense potential to enhance the efficiency and reduce the harmonics of grid connected system [17]. There have recently been several researchers that recommend reduced MLI switch topologies for a PV grid system [18]. Based on the literature it is found that all the works are carried for low voltage systems. Moreover, some inverters have more switches and a greater content of THD.

The main contributions of the paper are as follows:

- **Switch Reduction:** The proposed research work explores with the solar fed single phase Modular Multilevel Inverter (MMI) and control challenges, such as increasing the number of voltage levels, power quality issues, reducing the number of semiconductor switches and achieving higher efficiency.
- **Harmonic Reduction:** The performance improvement of a MMI is improved using the Selective Harmonic Elimination (SHE) method. Optimization methods such as particle swarm optimization (PSO), genetic algorithm (GA), and bee optimization (BO) are used to compute the complex equations of SHE.
- **Grid Synchronization:** To implement the cascaded control with optimization technique for Grid integration, since conventional controllers have slower response to the transients.

This paper is organized as follows: Sect. 2 illustrates the configuration of the proposed system; Sect. 3 presents the design of the modular converter; Sect. 4 presents the control method for the grid connected MMI; Sects. 5 and 6 describes the simulation and experimental results with discussions and Sect. 7 gives the conclusions of the proposed method.

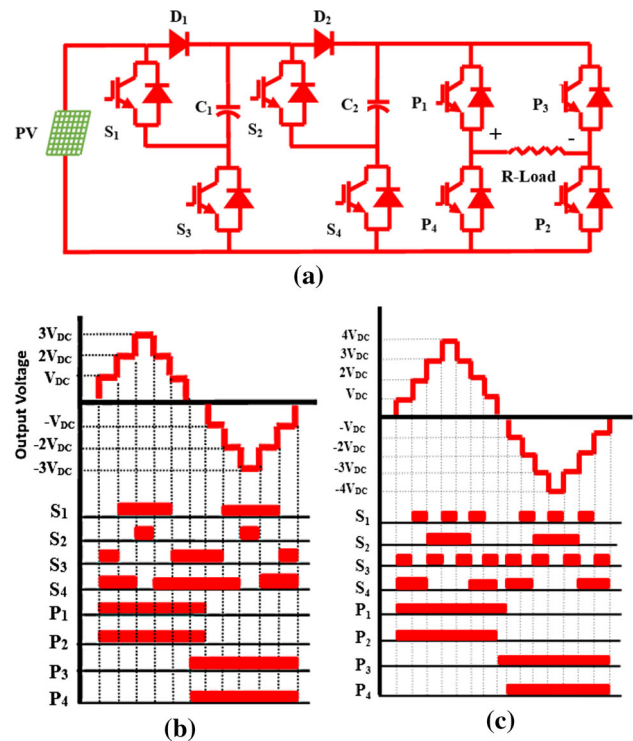


Fig. 1 a Generalized structure b Symmetric 7-level MMI c Asymmetric 9-level MMI

2 Proposed system design

Multilevel power conversion technology originally arises from the need to reduce the total harmonic distortion in the inverter's output. Later, it is introduced functionally to satisfy the need for high-voltage DC bus-driven inverters. The switching devices of conventional inverters experience high voltage stress or lack sufficient voltage rating to produce high voltages. The stress on each switching component can be reduced proportionally by using multilevel structures. As a result, a high voltage DC bus can be handled easily without the use of heavy step-up or step-down transformers. Hence, MLI can be used without the bulky transformers in grid-connected renewable energy applications. The proposed structure uses a single photovoltaic panel, two capacitors and eight switches to produce the desired output voltage. Figure 1 presents the structure of the proposed system with its corresponding waveforms in both symmetric and asymmetric modes. The proposed system can be operated with symmetric and Asymmetric DC sources. The proposed structure can produce seven level of output when the DC sources are symmetrical (1:1:1) and when the DC sources are asymmetrical (1:1:2) the proposed inverter can produce nine level of output.

The output waveforms of 7-level and 9-level inverter is presented in Fig. 1. Table 1 presents the parameters of the proposed system. Table 2 presents the Switching sequence of

Table 1 Parameters of the proposed System

Parameters	Based on number of levels(N_L)		Based on number of units (n)	
	Symmetric	Asymmetric	Symmetric	Asymmetric
Number of levels	N_L	N_L	$7n$	$9n$
Number of Switches	$N_L + 1$	$N_L - 1$	$8n$	$8n$
Number of Diodes	$N_L + 3$	$N_L + 1$	$10n$	$10n$
Number of Driver Circuits	$N_L + 1$	$N_L - 1$	$8n$	$8n$
Number of Capacitors	$N_L - 5$	$N_L - 7$	$2n$	$2n$
Number of DC sources	$N_L - 6$	$N_L - 8$	n	n

Table 2 Switching sequence of the proposed symmetric multilevel inverter

Level generation				Polarity generation				Capacitor		Output voltage
S_1	S_2	S_3	S_4	P_1	P_2	P_3	P_4	C_1	C_2	V_{out}
×	×	✓	✓	✓	✓	×	×	↑	↑	V_{DC}
✓	×	×	✓	✓	✓	×	×	↓	↑	$2V_{DC}$
✓	✓	×	×	✓	✓	×	×	↓	↓	$3V_{DC}$
×	×	✓	✓	×	✓	×	✓	↑	↑	$0V_{DC}$
×	×	✓	✓	✓	×	✓	×	↑	↑	$0V_{DC}$
×	×	✓	✓	×	×	✓	✓	↑	↑	$-1V_{DC}$
✓	×	×	✓	×	×	✓	✓	↓	↑	$-2V_{DC}$
✓	✓	×	×	×	×	✓	✓	↓	↓	$-3V_{DC}$

✓-ON, ×-OFF, ↑-Capacitor Charging, ↓-Capacitor Discharging

the proposed system using symmetric DC sources. Figure 2 presents the modes of operation of the proposed system.

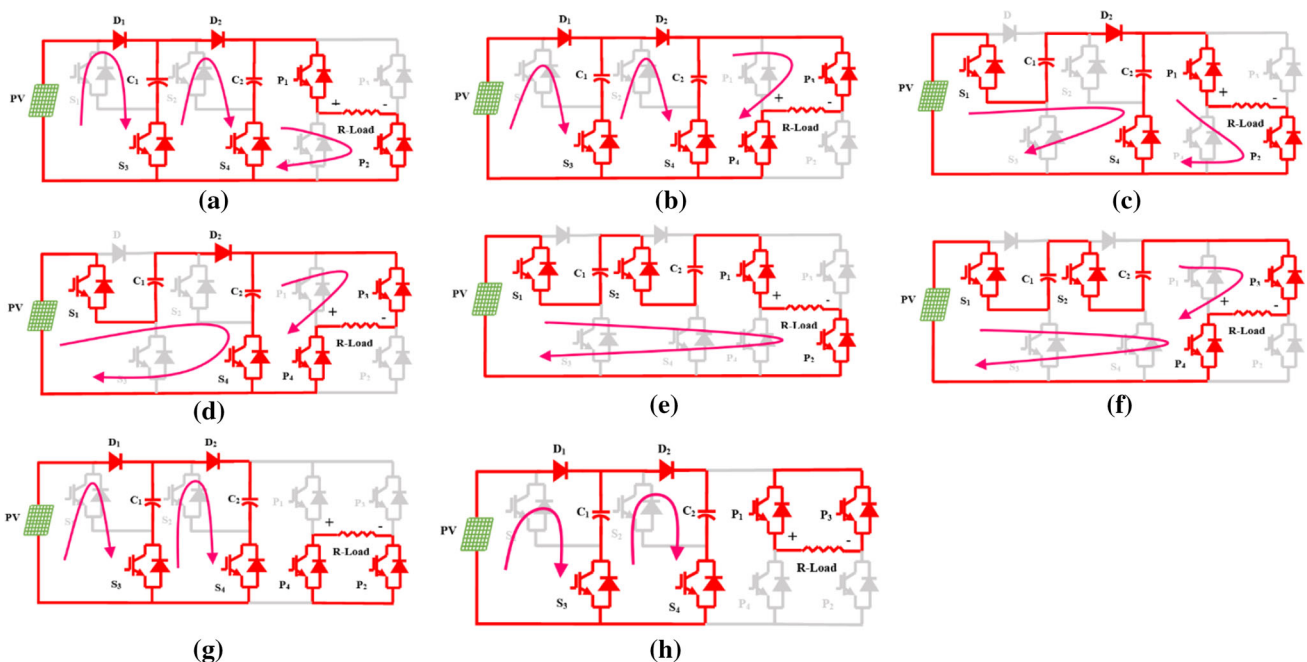


Fig. 2 Modes of operation of the proposed Symmetric Multilevel Inverter

Figure 2a presents the mode 1 operation of the proposed system. In mode1 $+V_{DC}$ is generated at the output voltage by triggering the switches P_1 and P_2 . During the triggering process along with the switches P_1 , P_2 the switches S_3 and S_4 are also triggered for making the capacitors C_1 and C_2 to charge. Similarly in mode 2, the negative level $-V_{DC}$ is obtained by triggering the switches, P_3 and P_4 . Figure 2b presents the mode 2 ($-V_{DC}$) operation of the proposed system.

During the generation of negative voltage level the switches S_3 and S_4 are also triggered for making the capacitors C_1 and C_2 to charge. Figure 2c presents the mode 3 ($+2V_{DC}$) operation of the proposed system. To achieve an output of $+V_{DC}$, the switches S_1 , P_1 , P_2 are triggered. During the generation of $+2V_{DC}$, the capacitor C_1 discharges through diode D_1 and by triggering the switch S_4 capacitor C_2 is charged. Similarly, the negative level $-2V_{DC}$ is obtained by triggering the switches, P_3 and P_4 . Figure 2d

Table 3 Switching sequence of the proposed asymmetric multilevel inverter

Level generation				Polarity generation				Capacitor		Output voltage
S_1	S_2	S_3	S_4	P_1	P_2	P_3	P_4	C_1	C_2	V_{out}
×	×	✓	✓	✓	✓	×	×	↑	↑	$1V_{DC}$
✓	×	×	✓	✓	✓	×	×	↓	↑	$2V_{DC}$
×	✓	✓	×	✓	✓	×	×	↑	↓	$3V_{DC}$
✓	✓	×	×	✓	✓	×	×	↓	↓	$4V_{DC}$
×	×	✓	✓	×	✓	×	✓	↑	↑	$0V_{DC}$
×	×	✓	✓	✓	×	✓	×	↑	↑	$0V_{DC}$
✓	×	×	✓	×	×	✓	✓	↓	↑	$-2V_{DC}$
×	✓	✓	×	×	×	✓	✓	↑	↓	$-3V_{DC}$
✓	✓	×	×	×	×	✓	✓	↓	↓	$-4V_{DC}$

✓-ON, ×-OFF, ↑-Capacitor Charging, ↓-Capacitor Discharging

presents the mode 4 ($-2V_{DC}$) operation of the proposed system.

Figure 2e presents the mode 5 ($+3V_{DC}$) operation of the proposed system. To achieve an output of $+3V_{DC}$, the switches S_1, S_2, P_1, P_2 are triggered. During the generation of $+3V_{DC}$, the capacitor C_1, C_2 discharges. Similarly the negative level $-3V_{DC}$ is obtained by triggering the switches, S_1, S_2, P_3 and P_4 . Figure 2f presents the mode 6 ($-3V_{DC}$) operation of the proposed system. Figures 2g, f presents the generation of zeroth level (mode 7).

In the proposed structure if the DC inputs are fed with asymmetric DC sources an asymmetric MLI is obtained. The developed structure is designed with minimum switch count by removing the use of bidirectional switches and clamping diodes. In addition, the proposed converter has no effect of diode reverse recovery times and uses simple gate driver circuit due to absence of bidirectional switches. During the generation of both the positive and negative levels, only four switches are in conduction, therefore the conduction losses of the proposed system are very less. Table 3 presents the switching sequence of the proposed asymmetric multilevel inverter. Figure 3a presents the mode 1 operation of the proposed asymmetric MLI. In mode1 $+V_{DC}$ is generated at the output voltage by triggering the switches P_1 and P_2 . During the triggering process along with the swithes P_1, P_2 the switches S_3 and S_4 are also triggered for making the capacitors C_1 and C_2 to charge. Similarly in mode 2, the negative level $-V_{DC}$ is obtained by triggering the switches, P_3 and P_4 . Figure 3b presents the mode 2 operation of the proposed system. During the generation of negative voltage level the switches S_3 and S_4 are also triggered for making the capacitors C_1 and C_2 to charge.

Figure 3c presents the mode 3 ($+2V_{DC}$) operation of the proposed system. To achieve an output of $+V_{DC}$, the switches S_1, P_1, P_2 are triggered. During the generation of $+2V_{DC}$, the

capacitor C_1 discharges through diode D_1 and by triggering the switch S_4 capacitor C_2 is charged. Similarly the negative level $-2V_{DC}$ is obtained by triggering the switches, S_1, P_3 and P_4 . Figure 3d presents the mode 4 ($-2V_{DC}$) operation of the proposed system.

Figure 3e presents the mode 5 ($+3V_{DC}$) operation of the proposed system. To achieve an output of $+3V_{DC}$, the switches S_2, P_1, P_2 is triggered. During the generation of $+3V_{DC}$, the capacitor C_1 , is charged by switching S_3 and C_2 discharges. Similarly the negative level $-3V_{DC}$ is obtained by triggering the switches, S_2, P_3 and P_4 . Figure 3f presents the mode 6 ($-3V_{DC}$) operation of the proposed system. Figure 3g presents the mode 7 ($+4V_{DC}$) operation of the proposed system. To achieve an output of $+4V_{DC}$, the switches S_1, S_2, P_1, P_2 are triggered. During the generation of $+4V_{DC}$, the capacitor C_1, C_2 discharges. Similarly the negative level $-4V_{DC}$ is obtained by triggering the switches, S_1, S_2, P_3 and P_4 . Figure 3h presents the mode 8 ($-4V_{DC}$) operation of the proposed system. Figures 3i and j presents the generation of zeroth level (mode 9). In order to validate the proposed topology in terms of required number of power electronic components, it should be compared with the other multilevel inverter topologies. Table 4 presents the comparison of the asymmetric 9-level inverter with other 9-level topologies.

3 Design of DC–DC converter

The use of generic DC–DC converters produces a greater amount of voltage ripples in the system. Therefore, high gain.

DC–DC converters gain more importance in voltage conversion systems. Designing a high gain DC–DC converter [30, 31] have some drawbacks such as reduced efficiency and higher stress on the switches of the converter. Moreover, high gain DC–DC converters require more number of components for conversion purpose. An impedance converter is implemented to obtain higher gain with fewer switches. Γ -source and Y-Source converters are some examples of impedance source converters.

These converters have drawbacks like increased voltage stress on the switches and regulation extent of duty cycle is limited. Therefore, to overcome the drawbacks of conventional and impedance source converters, a high gain DC–DC converter with coupled inductor having lower turns ratio is designed. Figure 4 presents the modular DC–DC converter. The proposed converter contains, three capacitors (c_a, c_b, c_c), two diodes (D_a, D_b), coupled inductor (three windings), Inductor and a power semiconductor switch (T). The three windings of the coupled inductor have a turns ratio of (N_a, N_b, N_c). Since the power semiconductor switch is implemented on the low voltage side of the converter, the stress on the switch is very less. The modular converter uses the Perturb and observe algorithm (P&O) for extracting

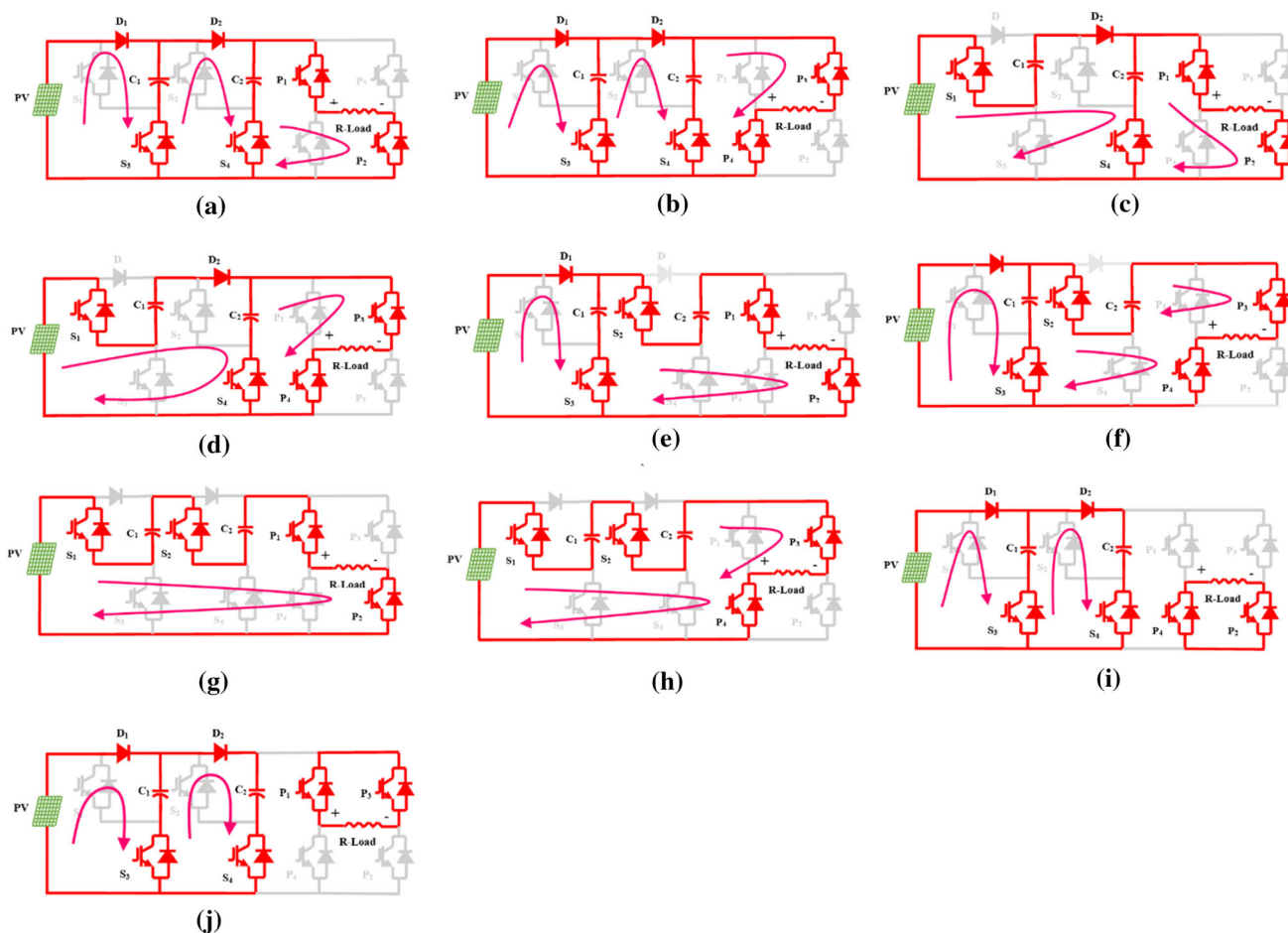


Fig. 3 Modes of operation of the proposed Asymmetric Multilevel Inverter

Table 4 Comparison of the Asymmetric Multilevel Inverter Topologies with Other 9-Level Topologies

Topology	N _{Level}	N _{DC}	N _{switch}	N _{Capacitor}	N _{Diode}
NPC	9	1	16	0	56
FC	9	1	16	28	0
CHB	9	4	16	0	0
[19]	9	2	12	3	0
[20]	9	4	10	0	3
[11]	9	2	12	3	0
[21]	9	2	12	3	0
[22]	9	2	14	2	0
[23]	9	2	10	2	0
[24]	9	4	12	0	0
[25]	9	4	12	0	16
[26]	9	4	11	0	0
[27]	9	1	11	2	0
[28]	9	4	12	0	0
[29]	9	5	10	0	0
Proposed	9	2	8	0	8

maximum power from the PV panel. There are two stages of operation for the proposed modular converter. Figure 5a presents the first stage of operation of the proposed converter. During the first stage of operation the switch T is turned on. Whenever the switch T is turned on, the input voltage makes the inductor (L) to charge and the current in the inductor rises linearly. During this stage the diodes D_a and D_b are reverse biased and the capacitor c_c feeds power to the load. Figure 5b presents the stage 2 operation of the modular converter. When the switch (T) is turned off, the energy stored in the inductor (L) is fed to the load through the impedance network. The voltage across the coupled inductors with turns ratio N_a, N_b, N_c is given in Eq. 1.

$$\left. \begin{aligned} V_{Na} &= V_{Lm} \\ V_{Nb} &= \frac{N_b}{N_a} V_{Lm} \\ V_{Nc} &= \frac{N_c}{N_a} V_{Lm} \end{aligned} \right\} \quad (1)$$

where V_{Na}, V_{Nb}, V_{Nc}, V_{Lm} are the voltage across the coupled inductances N_a, N_b, N_c and the magnetizing inductance L_m.

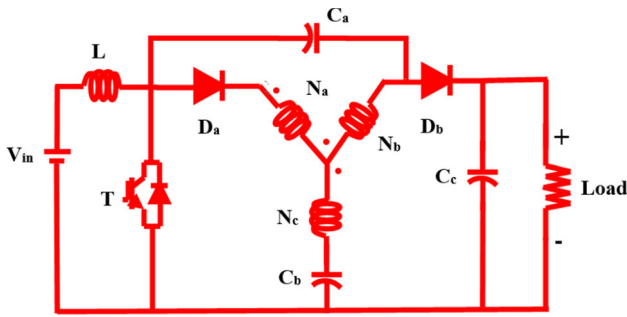


Fig. 4 Modular DC-DC converter

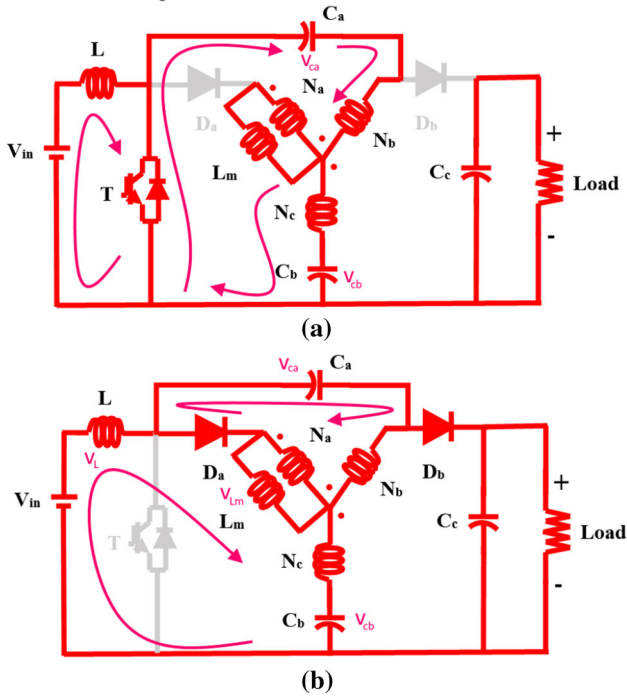


Fig. 5 a Stage 1 during Ton b Stage 2 during Toff

Applying the kirchoffs voltage law to the circuit presented in 5a,

$$V_L - V_{in} = 0 \tag{2}$$

$$-V_{ca} - V_{Nb} + V_{Nc} + V_{cb} = 0 \tag{3}$$

where V_{in} denotes the supply voltage, V_L is the inductance voltage, V_{ca} and V_{cb} presents the voltage across the capacitors c_a and c_b .

Substituting the values of 1 in 2 gives the voltage of the magnetizing inductance.

$$V_{Lm} = \frac{N_a}{N_b - N_c} (V_{cb} - V_{ca}) \tag{4}$$

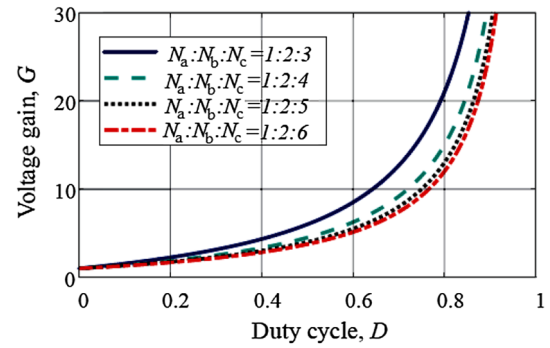


Fig. 6 Variation of voltage gain with change in duty cycle

Applying the Kirchoff’s voltage law to the circuit presented in 5b,

$$-V_L + V_{in} + V_{ca} - V_0 = 0 \tag{5}$$

$$-V_{ca} - V_{Nb} - V_{Na} = 0 \tag{6}$$

substituting equation 1 in 6

$$V_{Lm} = -V_{ca} * \frac{N_a}{N_b + N_a} \tag{7}$$

Implementing the principle of voltage second to the inductor L and the magnetizing inductance L_m , Eqs. 2, 4, 5 and 7 can be written as

$$DV_{in} + (1 - D)(V_{in} + V_{ca} - V_0) = 0 \tag{8}$$

$$= D \left(\frac{N_a(V_{cb} - V_{ca})}{N_c - N_b} \right) + (1 - D) \left(-\frac{N_a}{N_a + N_c} * V_{ca} \right) \tag{9}$$

$$V_{cb} = V_{in} + V_{ca} = \left(\frac{1 + KD}{1 - D} \right) V_{in} \tag{10}$$

$$G = \frac{V_0}{V_{in}} = \frac{1 + DK}{1 - D} \tag{11}$$

$$K = \frac{N_c + N_a}{N_c - N_b} \tag{12}$$

Equation 12 indicates that, for voltage boosting, $N_b > N_c$. Figure 6 presents the voltage gains of the proposed converter with different turns ratio and changing duty cycle.

4 Control technique for the proposed grid-connected inverter

The output of the inverter should be sinusoidal for appropriate synchronization of grid. Therefore, it is evident that the input provided to the inverter for the PV system should have lower THD, and faster dynamic response. To gain maximum power from the PV array, and inject sinusoidal current into

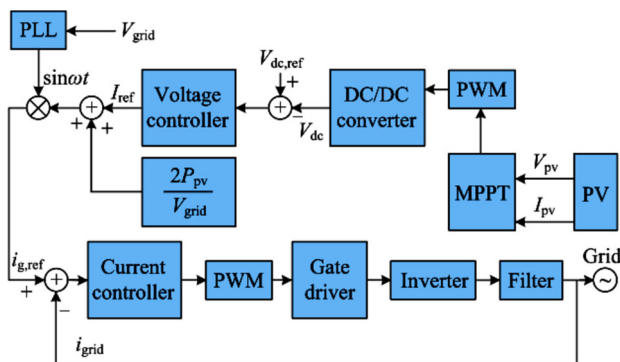


Fig. 7 Closed loop control system for the proposed system

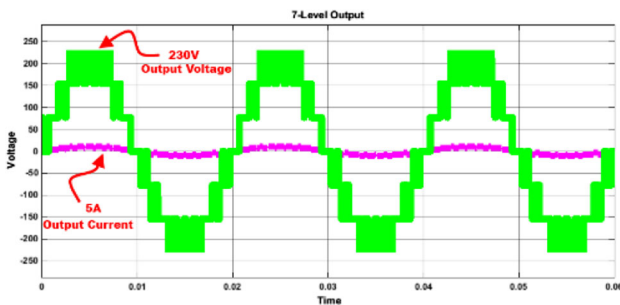
the grid, an interface between the PV array and the grid must be used for grid connected PV system (GCPVS). To satisfy these criteria, the proposed inverter is used as the interface between the PV array and the grid. The present work uses the two-stage configuration of PV system. The SHE method is used to generate pulses to the proposed inverter, thereby increasing the output power quality. The closed loop control is implemented for the proposed GCPVS. Figure 7 presents the closed loop control system of the proposed GCPVS. The voltage control loop controls the DC link voltages from the PV sources and the Current loop controls the inverter current. Power quality standards must be established throughout the grid-connected system to meet the grid interconnection.

The grid interfaced inverter are to be specifically built to validate the correct photovoltaic operation and enhance the quality of power at Point of Common Coupling (PCC). The energy extracted from the sunlight varies periodically. The solar panel has an average voltage of 12 V with a current of about 7A; it varies between 12–20 and 12 + 20% throughout the day. The developed inverter transforms this energy into the grid as per the grid requirements. One significant problem in integrating the proposed inverter with grid is the complexity of their control for synchronization. The traditional controllers are taking a longer duration to synchronize the suggested inverter with the grid. It is a challenging issue to control the varying output voltage of the inverter owing to changes in the solar radiation and synchronize the inverter with the grid. Moreover, the use of traditional control techniques in GCPVS leads to poor efficiency. Therefore, there is a need for implementing an advance control technique to solve this problem. The efficiency and THD of the inverter is also considered as an important issue in the GCPVS. The PI controller is extensively used in the closed loop control system since it is simple to implement, robust in nature and it has the ability to operate under dynamic conditions. In the control loop the conventional PI controller fails to update its gain values whenever the system is subjected to sudden changes. To improve the performance of the PI controller, the gain values are tuned using the PSO optimization method.

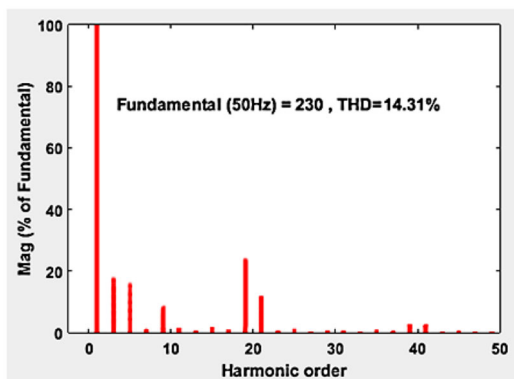
In real time, the data is extracted from the system and is given to the optimization controller, where the optimization is carried out in offline. If the optimization is carried out in online, the iteration process consumes time for giving accurate results. The entire optimization process slows down when tuning is done online. Therefore, the optimization is done in the offline thereby enhancing the performance of the grid connected system. An effective control strategy has been implemented to inject a harmonic less current with sinusoidal wave shape and maintain an in-phase relationship with the grid voltage. To achieve so, the separate DC inputs must be retained identical to their reference voltage values (V_{DC1}^* , V_{DC2}^* , V_{DC3}^*), which are considered in 1 : 1 : 3 ratio under varying irradiance condition. In the closed-loop control system the voltage controller is used to maintain a minimum DC link voltage equivalent to the constant reference voltage corresponding to the irradiation level. To regulate the overall DC voltage, the DC voltages which are taken as reference ($V_{DC1}^* + V_{DC2}^* + V_{DC3}^*$) is equated with the overall calculated DC voltages ($V_{DC1} + V_{DC2} + V_{DC3}$) and the error which is obtained as the output is transmitted via the proportional and Integral controller (PI). The PI type controllers contain gain parameters ($K_{p_{v1}}$, $K_{p_{i1}}$), which are tuned to supply maximum reference grid current (I_{max}) to the grid in the proposed GCPVS. For the GCC the Phase Lock Loop (PLL) generates a sinusoidal wave shaped reference grid current (I_g^*). A PLL is often equipped for grid synchronization. The parts in a PLL are a Phase Detector (PD), a PI-based Low Pass Filter (LF) and a voltage-controlled oscillator (VCO). The phase detector block is used to detect the phase difference between the input signal and the feedback signal. When the output of the phase detector is passed through the PI based LF block the high frequency element is removed by the low pass filter and the frequency element is obtained at the output of the LF block. During the stable condition the output signal from the LF block tends to zero. Thus the output phase signal is locked by giving the grid voltage as input. For enhancing the inverter's output current, the reference current of the grid (I_g^*) which is obtained from the product of sine component of PLL and output signal of total voltage controller block is equated to the instantaneous value of the grid current (I_g). The current error which is produced in the comparator is transmitted via the PI current type controller. The current controller gains ($K_{p_{c1}}$, $K_{p_{i1}}$) are calibrated in such a way that the grid current is maximized and becomes equivalent to the reference grid current (I_g^*). During normal operating condition, the current controller produces the reference signal (V_k^*) which can be omitted from the grid voltage (V_g) for the production of reference inverter voltage (V_{ref}). This is known as the grid tracker since the inverter's reference voltage differs based on the variations in the grid voltage. If the voltage in the grid decreases, the difference between ($V_g - V_k^*$) decreases

Table 5 Fitness function of the optimization techniques

Optimization methods	Fitness function
BCO [33]	$f = 100 * \left(\frac{V_1^* - V_1}{V_1^*}\right)^4 + \frac{1}{3} \left(50 * \frac{V_3}{V_1}\right)^2 + \frac{1}{5} \left(50 * \frac{V_5}{V_1}\right)^2 + \frac{1}{7} \left(50 * \frac{V_7}{V_1}\right)^2$
GA [33]	$f = 100 * \left(\frac{V_1^* - V_1}{V_1^*}\right)^4 + \frac{1}{3} \left(50 * \frac{V_3}{V_1}\right)^2 + \frac{1}{5} \left(50 * \frac{V_5}{V_1}\right)^2 + \frac{1}{7} \left(50 * \frac{V_7}{V_1}\right)^2$
PSO [33]	$f = 100 * \left(\frac{V_1^* - V_1}{V_1^*}\right)^4 + \frac{1}{3} \left(50 * \frac{V_3}{V_1}\right)^2 + \frac{1}{5} \left(50 * \frac{V_5}{V_1}\right)^2 + \frac{1}{7} \left(50 * \frac{V_7}{V_1}\right)^2$



(a)



(b)

Fig. 8 Simulation output of **a** 7-level inverter **b** THD

and thus the inverter reference (V_{ref}) decreases. Therefore, the basic voltage of the inverter still continues to follow the grid voltage.

4.1 Pulse width modulation for the proposed inverter

Harmonics are characterized as the integral multiples of the fundamental frequency and occur as the voltage or current distortion of the waveform. The existence of harmonics in the inverter output can contribute to overheating in neutral conductors of machines, erratic operation of circuit breakers, malfunctioning of microprocessor-based equipment, degra-

Table 6 BCO Parameters

Parameter	Value
Number of skilled bees	20
Number of scout bees	20
Number of sites selected for neighbourhood search	15
Number of elite sites	4
Stopping criteria	80iterations

Table 7 Triggering Angles for different Modulation Index and THD for BCO

Modulation Index	Switching angles (Degrees)				%THD
	β_1	β_2	β_3	β_4	
0.6	24.21	31.28	49.88	71.56	15.14
0.7	28.36	36.54	47.19	77.43	13.86
0.8	31.89	39.15	46.25	64.57	12.52
0.9	13.41	29.88	42.79	66.39	10.43

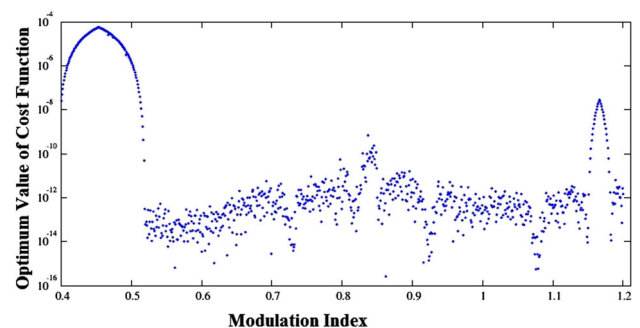
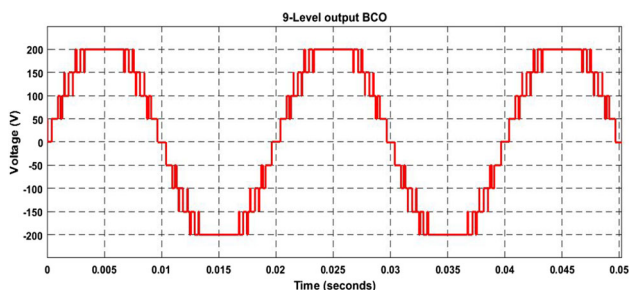
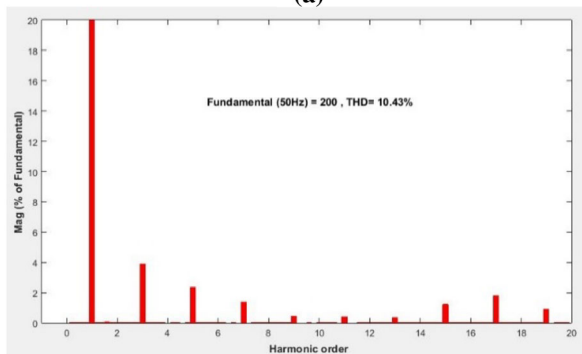


Fig. 9 Modulation Indices versus Optimum Value of Cost Function Using BCO

dation of power factor correction capacitors, and pronounced magnetic fields near switchgears and transformers. SHE method eliminates different order harmonics in the inverter voltage by choosing appropriate switching angles. These switching angles are obtained by solving a set of complex transcendental equations. The mathematical solution to nonlinear transcendental equations, including trigonomet-



(a)



(b)

Fig. 10 a 9-Level output voltage b FFT analysis of 9-Level MMI Using BCO

ric terms, are very difficult to obtain. This is a fundamental problem in this method. Applying dissimilar DC sources contributes to a variety of high-degree equations, that are difficult to be solved. This restriction is remedied by using different methods of optimization techniques such as BEE Colony Optimization (BCO), Genetic Algorithm (GA), and Particle Swarm Optimization (PSO). For the suggested technique, the objective function is developed and corresponding operations with regard to GA, PSO, and BA are conducted, to achieve the optimal triggering angles required for the inverters. The selective harmonic elimination method is very appropriate for MMIs. By implementing this method, the selected harmonics (3rd, 5th and 7th) in the output of the 9-level MMI is drastically reduced. Therefore, the use of filters at the end of the MMI is also reduced. The selected harmonics can be removed from the staircase waveform by implementing additional switching within the staircase waveform. During every half cycle of the 9-level output, the semiconductor switches are switched on and off continuously and these switching's are distributed equally over each cycle with quarter wave symmetry. In a staircase waveform if the waveform repeats the same pattern for every quarter cycle it is called quarter wave symmetry.

The harmonic components from the 9-level staircase waveform can be extracted using Fourier series. In Fourier series any periodic function can be represented by an infinite addition of harmonically related trigonometric functions. By executing the Fourier series, the 9-level waveform which is

Table 8 GA Parameters

Parameter	Value
Population size	24
Crossover rate	0.5
Mutation rate	0.234
Stopping criteria	100 iterations

Table 9 Triggering Angles for different Modulation Index and THD using GA

Modulation Index	Switching angles (Degrees)				%THD
	β_1	β_2	β_3	β_4	
0.6	26.92	36.21	49.28	63.56	13.44
0.7	23.73	39.14	48.39	60.18	11.07
0.8	19.36	30.05	45.77	68.35	9.81
0.9	12.34	28.63	39.12	57.53	7.11

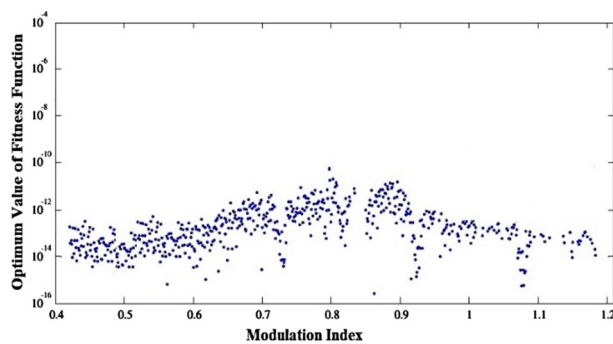


Fig. 11 Modulation Indices versus Optimum Value of Fitness Function Using GA

Table 10 PSO Parameters

Parameters	Value
S1, S2	0.3
R1, R2	0.9[0to1]
w(k)	0.9
Stopping criteria	100 iterations

non-sinusoidal in nature can be represented in equations with sine or cosine terms. Thus, by simplifying the Fourier series the fundamental and harmonic equations are derived. Therefore Eq. 13 represents the Fourier series of a periodic function in the mathematical form.

$$F(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t) + \sum_{n=1}^{\infty} B_n \sin(n\omega t) \quad (13)$$

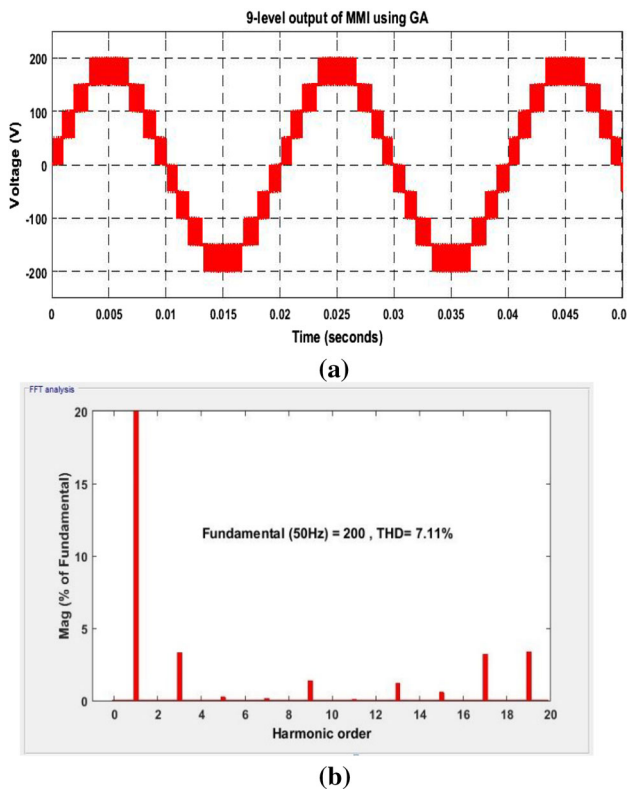


Fig. 12 a 9-Level output voltage bFFT analysis of 9-Level MMI Using GA

Table 11 Triggering Angles for different Modulation Index and THD for PSO

Modulation Index	Switching angles (Degrees)				%THD
	β_1	β_2	β_3	β_4	
0.6	13.42	39.23	55.11	70.21	8.34
0.7	12.65	35.75	58.94	72.62	7.51
0.8	11.91	33.53	60.46	76.83	6.12
0.9	10.36	31.14	64.92	82.72	5.15

where

$$A_0 = \frac{4}{\pi} \int_0^{2\pi} F(t) d\omega t \tag{14}$$

$$A_n = \frac{4}{\pi} \int_0^{2\pi} F(t) \cos n\omega t d\omega t \tag{15}$$

$$B_n = \frac{4}{\pi} \int_0^{2\pi} F(t) \sin n\omega t d\omega t \tag{16}$$

A_0 , A_n , and B_n are termed as the Fourier elements, the angular frequency is ω , ($\omega = 2\pi f$).

The half wave symmetry and the quarter wave symmetry are used to simplify the Fourier series. In a staircase waveform if each half cycle is the mirror image of the next half cycle then it is called half wave symmetry. The halfwave symmetry eliminates the even harmonics from the output waveform. The presence of even order harmonics leads to resonance in the network. In Eq. (13), due to the half wave symmetry and the quarter-wave symmetry the Fourier elements, A_0 , A_n and the integral multiples of fundamental (even harmonics) are equated to zero. Moreover, to establish the amplitude of the Fourier elements (B_n) of odd harmonics ($1/4$) th of a fundamental period is integrated. From Eq. (16),

$$B_n = \frac{4}{\pi} \int_0^{2\pi} F(t) \sin n\omega t d\omega t$$

where $F(t) = V_{out}$

$$B_n = \frac{4}{\pi} \int_0^{2\pi} V_{out} \sin n\omega t d\omega t \tag{17}$$

For all n , the Fourier series is given as

$$F(t) = \sum_{n=1}^{\infty} B_n \sin(n\omega t) \tag{18}$$

Substituting $\beta = \omega t$ in Eq. (16),

$$B_n = \frac{4}{\pi} \int_0^{2\pi} F(t) \sin n\beta d\beta \tag{19}$$

$$B_n = \frac{4V_{DC}}{\pi} \left[\int_{\beta_1}^{\frac{\pi}{2}} \sin n\beta d\beta + \int_{\beta_2}^{\frac{\pi}{2}} \sin n\beta d\beta + \int_{\beta_3}^{\frac{\pi}{2}} \sin n\beta d\beta + \int_{\beta_4}^{\frac{\pi}{2}} \sin n\beta d\beta \right] \tag{20}$$

$$B_n = \frac{4V_{DC}}{n\pi} \sum_{k=1}^R \cos(n\beta_k) \tag{21}$$

$$B_n = \frac{4V_{DC}}{n\pi} [\cos(n\beta_1) + \cos(n\beta_2) + \cos(n\beta_3) + \cos(n\beta_4)] \tag{22}$$

where n is the harmonic order, R is the number of switching angles each quarter and is also equal to number of PV sources, β_k is the k th switching angle and V_{DC} indicates the DC voltages.

To determine triggering angles β_1 , β_2 , β_3 , and β_4 , Eqs. (23) to (26) derived from Eq. (22) ought to be evaluated. Since these equations are indefinite and constitute trigonometric parameters, they are not possible to be solved with algebraic techniques. This contributes to the necessity of

optimization methods to render the triggering angles ($\beta_1, \beta_2, \beta_3, \beta_4$) for producing preferred output with reduced harmonic distortions.

The nonlinear equation of the fundamental component is written as:

$$V_1 = \frac{4V_{DC}}{\pi} [\cos(\beta_1) + \cos(\beta_2) + \cos(\beta_3) + \cos(\beta_4)] \quad (23)$$

The nonlinear equations for the odd harmonic component are written as:

$$V_3 = \frac{4V_{DC}}{3\pi} [\cos(3\beta_1) + \cos(3\beta_2) + \cos(3\beta_3) + \cos(3\beta_4)] \quad (24)$$

$$V_5 = \frac{4V_{DC}}{5\pi} [\cos(5\beta_1) + \cos(5\beta_2) + \cos(5\beta_3) + \cos(5\beta_4)] \quad (25)$$

$$V_7 = \frac{4V_{DC}}{7\pi} [\cos(7\beta_1) + \cos(7\beta_2) + \cos(7\beta_3) + \cos(7\beta_4)] \quad (26)$$

The basic voltage equation presented in Eq. (23) can be expressed in terms of M_i as follows,

$$\cos(\beta_1) + \cos(\beta_2) + \cos(\beta_3) + \cos(\beta_4) = H * M_i \quad (27)$$

To remove the third-, fifth-, and seventh-order harmonics from the output Eqs. (28) to (31) should be solved.

$$\cos(\beta_1) + \cos(\beta_2) + \cos(\beta_3) + \cos(\beta_4) - (3 * M_i) = 0 \quad (28)$$

$$\cos(3\beta_1) + \cos(3\beta_2) + \cos(3\beta_3) + \cos(3\beta_4) = 0 \quad (29)$$

various voltages that enter the inverter stages would, therefore, trigger fundamental non-regulated harmonics of higher magnitude, which must also be considered. For three-phase systems, the removal of triple harmonics is not required since such distortions are automatically removed from the line to line voltage.

4.1.1 Computation of switching angles by using optimization methods

Optimization is the method in which the optimal outcome is obtained under any different situations. It is commonly used in science and technology for various applications to optimize the targeted result. The structuring of the optimization challenge is to start with the identification of the design variables that are used during the optimization method. The next challenge is to find limitations linked to the optimization problem that represent a functional correlation between design variables and other design parameters. The formulation method is to identify the objective function as design parameters and other problem variables. The objective function can be of two types, either maximization or minimization. In this work the minimization objective function is used since the main objective of the SHE method is to minimize the harmonics. Equation (32) shows the objective function (O) of the SHE method in harmonics minimization for the 9-level MMI.

$$\text{Minimize}(O) = F(\beta_1, \beta_2, \beta_3, \beta_4) \quad (32)$$

$$\text{Subjected to } 0 \leq \beta_1 < \beta_2 < \beta_3 < \beta_4 \leq \frac{\pi}{2}.$$

The objective function (Min O) and constraints of 9-level MMI is specified in Eqs. (33) and (34).

$$\text{Min } O = \left\{ \begin{aligned} W(k) * (V_{1(p.u)} - \frac{V_1}{V_{1\text{maximum}}}) &= \frac{1}{4} (\cos(\beta_1) + \cos(\beta_2) + \cos(\beta_3) + \cos(\beta_4)) + THD_{\text{min}} \\ &= \sqrt{\frac{\pi}{4} * \frac{(\beta_2 - \beta_1) + 4(\beta_3 - \beta_2) + 9(\frac{\pi}{2} - \beta_4)}{\cos(\beta_1) + \cos(\beta_2) + \cos(\beta_3) + \cos(\beta_4)} - 1} \end{aligned} \right\} \quad (33)$$

$$\cos(5\beta_1) + \cos(5\beta_2) + \cos(5\beta_3) + \cos(5\beta_4) = 0 \quad (30)$$

Constraints

$$\cos(7\beta_1) + \cos(7\beta_2) + \cos(7\beta_3) + \cos(7\beta_4) = 0 \quad (31)$$

$$0 \leq \beta_1 < \beta_2 < \beta_3 < \beta_4 \leq \frac{\pi}{2} \quad (34)$$

$$\text{Where } M_i = \frac{\pi V_1}{V_{\text{max}}} = \frac{\pi V_1}{4 * H * V_{DC}}$$

H denotes the number of PV sources, V_{max} is the peak output voltage of MMI, V_{PV} is the input PV source of MMI.

In the suggested MMI-based PV system the PV-cell voltages vary from 36 to 48 V, and from the battery-driven energy storage network centered on MMI, the battery voltages often shift according to their state of charge (SoC). The

where $\beta_1, \beta_2, \beta_3, \beta_4$ are the switching angles, $W(k)$ is the weighting factor which is used for making the error small enough and per unit equivalent of the output peak voltage whose value is between 0 to 1. In the objective function (Min O), the first element is the absolute value of error in adjusting the fundamental component. Table 5 shows the fitness function used

Table 12 Performance Comparison of THD and Harmonic components of 9-level MMI with BCO, GA and PSO methods

Method	Modulation Index	Switching angles (Degrees)				%THD	H ₃ (%)	H ₅ (%)	H ₇ (%)
		β_1	β_2	β_3	β_4				
BCO	0.6	24.21	31.28	49.88	71.56	15.14	1.08	0.68	0.66
		26.92	36.21	49.28	63.56	13.44	0.95	0.28	0.16
		13.42	39.23	55.11	70.21	8.34	0.49	0.45	0.38
GA	0.7	28.36	36.54	47.19	77.43	13.86	0.78	0.31	0.10
		23.73	39.14	48.39	60.18	11.07	0.57	0.06	0.47
		12.65	35.75	58.94	72.62	7.51	0.39	0.46	0.05
BCO	0.8	31.89	39.15	46.25	64.57	12.52	0.68	0.26	0.00
		19.36	30.05	45.77	68.35	9.81	0.45	0.43	0.38
		11.91	33.53	60.46	76.83	6.12	0.16	0.25	0.03
BCO	0.9	13.41	29.88	42.79	66.39	10.43	0.52	0.04	0.37
		12.34	28.63	39.12	57.53	7.11	0.37	0.42	0.04
		10.36	31.14	64.92	82.72	5.15	0.05	0.01	0.37

H₃, H₅, H₇-Third, Fifth, Seventh order harmonics

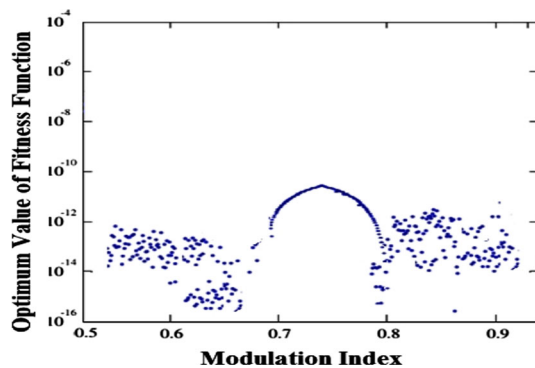


Fig. 13 Modulation Indices versus Optimum Value of Fitness Function Using PSO

by the optimization algorithms to obtain the switching angles.

The performance of the optimization technique depends upon the formulation of the fitness function. In [32] the authors discussed about the review of different optimization methods used in selective harmonic elimination technique for calculating the switching angles. From [32] it has been identified that the use of an improved or modified fitness functions is to improve the accuracy of the solution as well as reduce the convergence time. But we cannot compare the performance of the optimization algorithms with different fitness functions used for performing the same task. Therefore, Table 5 consist of same fitness function for all the three algorithms BCO, GA and PSO. All three are nature inspired algorithm. However, the GA bases itself of encoding of “genes” that multiplies, while preserving the optimal solutions, until the best optimum solution is found. The PSO technique uses an iterative process to iterate velocity and position of each particle, until the global minimum is reached. It has been noticed that the GA sometimes gets trapped at the

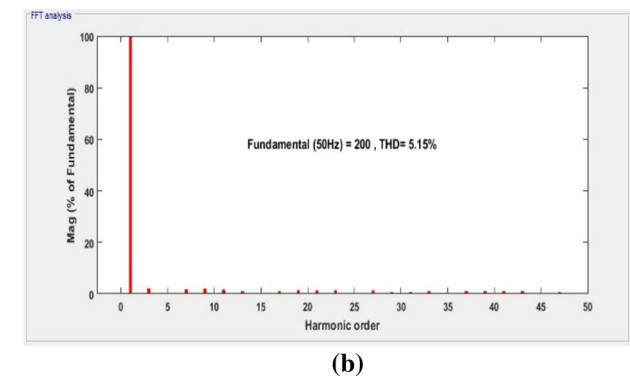
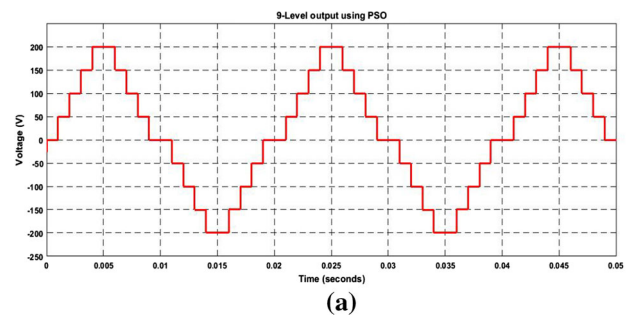


Fig. 14 a 9-Level output voltage **b** FFT analysis of 9-Level MMI Using PSO

boundaries, when there are too many constraints method has limited search space and is non-convergent. Also, there are many parameters that needs to be adjusted to reach an optimal solution. But the solution obtained using PSO method is more accurate, robust and has fast computing capability.

5 Simulation results

The 7-level symmetric multilevel inverter and 9-level asymmetric multilevel inverter are simulated in MAT-

LAB/Simulink. For experimental investigations the 9-level asymmetric multilevel inverter is considered in this work. The method which provides the least THD in simulation is implemented for the experimental setup. Each DC source of a symmetric MLI is provided with a voltage of 112 V. Since the proposed system uses three DC source, an average voltage of 336 V is obtained and the inverter provides an output of 230Vrms. Figure 8 presents the 7-level output with its THD. For simulation purpose the DC sources of the 9-level asymmetric MLI are considered as 40 V:40 V:120 V.

5.1 Bee colony optimization

Table 6 presents the variables of BCO used for the execution of the program. The BCO program is run in MATLAB and the triggering angles are obtained. Table 7 presents the triggering angles for different M_i . From Table 7, it is inferred that when the modulation index M_i is 0.9, the optimum switching angles give minimum THD of 10.43%. Figure 9 presents the fitness values of different generations. It is observed from Fig. 9 that, for various modulation indexes ranging from 0.4 to 1.2, the value of cost function in Y axis is between 10^{-12} and 10^{-14} ; hence, the efficiency of this method for solving SHE problem is evident. Figure 10 presents the output and FFT analysis of the 9-level MMI using BCO. From the FFT analysis, it is concluded that the THD obtained using BCO is 10.43%.

5.2 Genetic algorithm

For the proposed 9-level MMI, Table 8 shows the GA parameters. Table 9 shows the switching angles required to reduce the third-, fifth- and seventh-order harmonics for several ranges of modulation indices using GA. Figure 11 presents the fitness values for different modulation index. It is observed from Fig. 11 that, the fitness values fall in the range of 10^{-12} and 10^{-14} for different modulation indexes and this value gradually decreases from 0.9 to 1.2 of the modulation index value. Therefore, the best fitness values are found in the region where the modulation index is 0.9. Table 9, it is inferred that when the M_i is 0.9, the optimum switching angles give minimum THD of 7.11%. Figure 12 presents the output and FFT analysis of the 9-level MMI using GA. From the FFT analysis, it is concluded that the THD obtained using GA is 7.11%.

5.3 Particle swarm optimization

Table 10 shows the PSO parameters used for the execution of the program. Table 11 shows the switching angles required to reduce the third-, fifth- and seventh-order harmonics for several ranges of modulation indices using PSO. Figure 13 shows the relation between the fitness value and the modula-

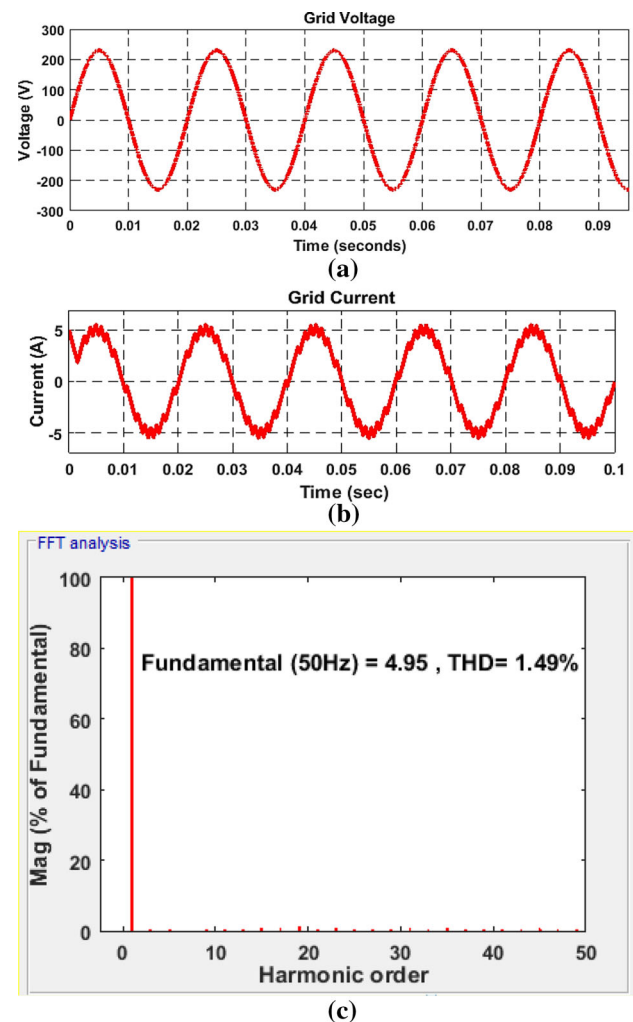


Fig. 15 a Grid voltage b Grid current c FFT analysis of Grid Current using FFA-PI controller

tion index. From Fig. 13 it is observed that the fitness value lies between 10^{-12} and 10^{-14} for the modulation index 0.1 to 0.9. It is also noted that the fitness value has a steep raise from 0.7 to 0.8 of modulation index. The best fitness values are obtained at the modulation index 0.9. Figure 14 presents the output and FFT analysis of the 9-level MMI using PSO. From the FFT analysis, it is concluded that the THD obtained using PSO is 5.15%. The output of 9-level MMI consist of H_3 , H_5 , H_7 order of harmonics. These harmonic contents have to be minimized since they are dominant and may cause damage to the system. Table 12 presents the THD values of the 9-level MMI for various modulation index values using BCO, GA and PSO optimization techniques. From Table 12 it is evident that the total THD % as well as the harmonic contents of the proposed 9-level MMI are very less for the PSO algorithm when compared with the other two techniques. Figure 15 presents the output waveforms of grid voltage, grid current and THD of the proposed system using PSO-PI controller.

Controller	Gain Parameters				%THD	
	Voltage Controller		Current Controller			
	K_{vp}	K_{vi}	K_{cp}	K_{ci}	Simulation	Experimental
PSO-PI	0.41	0.205	1.1	0.294	1.49	2.03



Fig. 16 Solar Plant of rating 1kWp

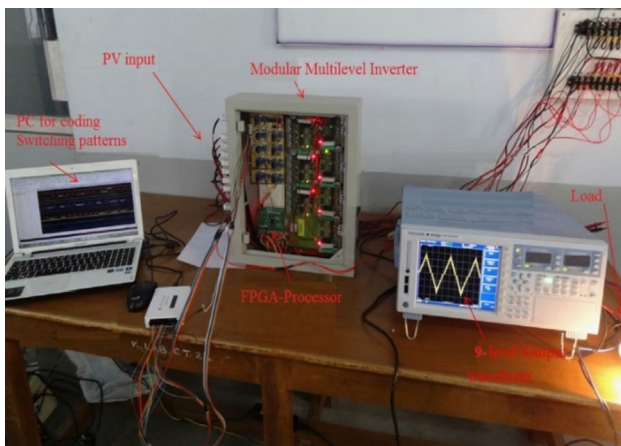
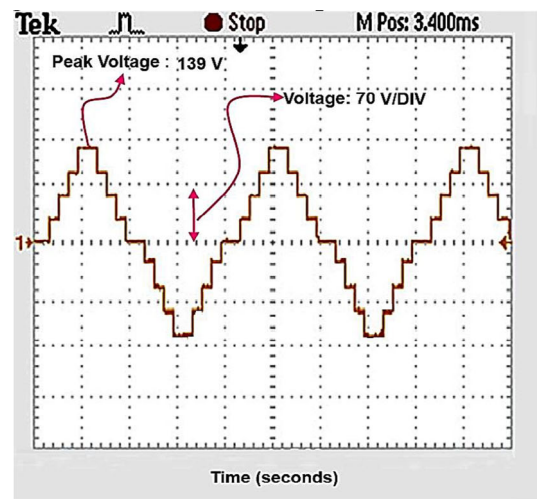


Fig. 17 Hardware set up of MMI with SHE

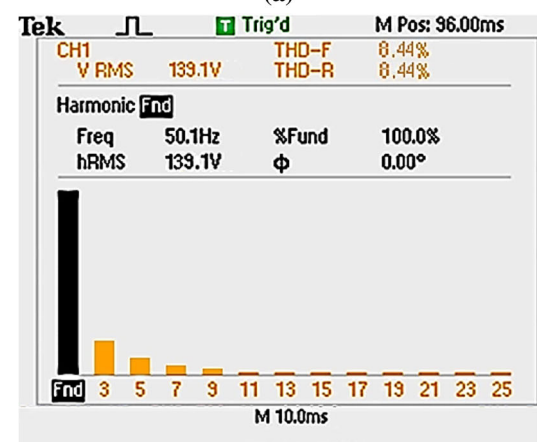
From Fig. 15 it is observed that the THD obtained using the PSO-PI controller is very less (1.49%) and satisfies the IEEE-519 standard.

6 Experimental results

For the hardware implementation, the input PV sources are obtained from the 1kWp PV plant. Figure 16 shows the setup of a 1kWp PV plant. The PSO algorithm is used in the hardware implementation for computation of switching angles. Figure 17 shows the hardware setup including the four PV sources, FPGA SPARTAN 6E processor, Digital Storage Oscilloscope (DSO), and Load. In the processor, the offline procedure is utilized where the switching angles are pre-calculated and then programmed.



(a)



(b)

Fig. 18 Experimental output of the 9-level MMI with its FFT analysis

Using the MATLAB software, the PSO code is run for generation of switching angles. These switching angles which are in.m files are converted to.vdl using the HDL coder. This conversion is necessary since the FPGA kit works with.vhd code. The processor finds the relevant switching angles and transfers it to the driver circuit which is connected to IGBT for turning it ON. Figure 18 illustrates the experimental output of the suggested 9-level MMI with its FFT analysis. The THD obtained for the 9-level MMI is 8.44%. Table 13 presents the gain parameters and % THD of the proposed system, Table 14 presents the specifications of PV fed grid connected system.

Table 15 presents the comparison of the proposed technique with other methods. To integrate the proposed inverter to the grid, the input DC voltages are scaled in the ratio of 65 V:65:195 V. The average value obtained is 335 VDC. This DC input is fed to the inverter to achieve 230Vrms at its output. Figure 19 presents the prototype of the GCPVS.

Table 13 Gain Parameters and THD Value of the proposed Grid Connected System

Controller	Gain parameters				%THD	
	Voltage controller		Current controller		Simulation	Experimental
	K_{vp}	K_{vi}	K_{cp}	K_{ci}		
PSO-PI	0.41	0.205	1.1	0.294	1.49	2.03

Table 14 Specifications of PV Fed Grid Connected System

PV FED MMI	
Nominal grid voltage (V_{rms})	230 V_{rms}
DC Voltage (V_{DC})	360 V
Switching Frequency (f_s)	1 kHz
Supply Frequency (f)	50 Hz
Inverter Filter inductance (L_i)	32 mH
Grid Filter inductance (L_g)	20 mH
Filter capacitance (C)	3.45 μ F
Grid frequency (ω)	$2\pi * 50$ rad/sec
Grid resistance (R_g)	0.05 Ω

Table 15 Comparison of the proposed technique with Other Modulation Methods

S. no.	Authors	Levels	Methodology	THD (%)
1	Panda et al. [33]	7	SHE-PSO	19.89
			SHE-FSO	14.66
			SHE-PSFSO	10.47
2	Panda and Panda [34]	7	PSO	11.81
3	Memon et al. [35]	7	APSO	12.52
4	Mahato et al. [12]	9	SHE-PWM	13.68
5	Lee et al. [8]	9	SHE-PWM	19.051
6	Saeedian et al. [36]	9	MCPWM	11.83
7	Proposed	9	SHE-PSO	8.44

MCPWM-Multicarrier PWM

Figure 20 presents the grid voltage and grid current of the proposed grid connected system in steady state condition.

From Fig. 19 it is observed that the grid voltage and grid currents are inphase. Figure 21 presents the experimental voltage and current THD of the proposed GCPVS. From Fig. 21 it is observed that the proposed systems THD is very less and it satisfies the IEEE-519 standard. Figure 22 presents the experimental output of the GCPVS under transient mode. From Fig. 22 it is observed that the proposed control system acts very fast and maintains the grid voltage and current in phase.

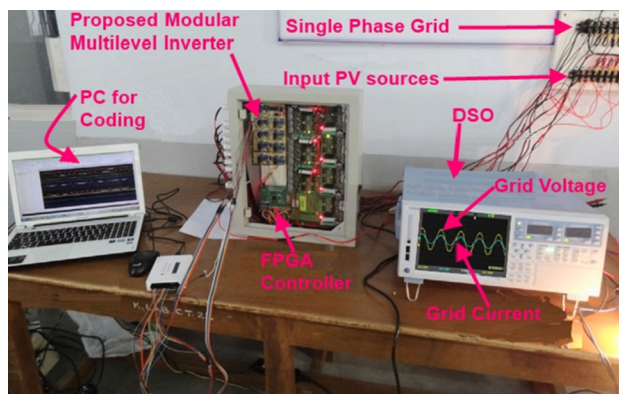


Fig. 19 Prototype model of the suggested system

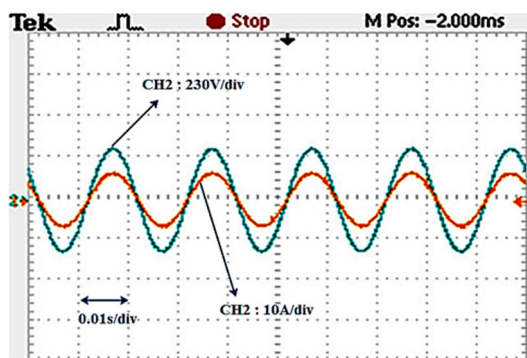


Fig. 20 Grid Voltage and Grid Current of the Prototype Under Steady State Condition

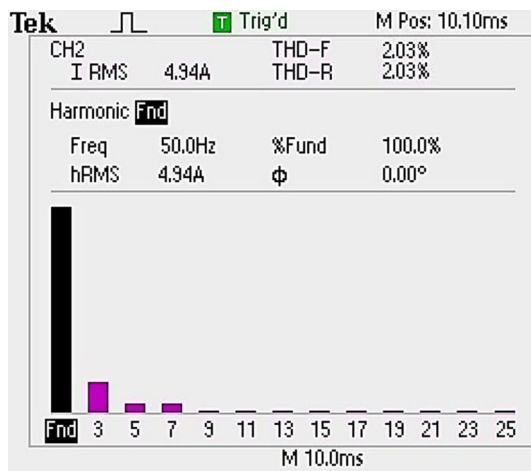


Fig. 21 Experimental THD of Grid Current

7 Conclusion

A 7-level and 9-level MMI for the elimination of certain harmonic orders (H3, H5, H7 for 9-level) is developed for power quality improvement. The selective harmonic elimination method is used with optimization methods (GA, PSO, and BCO) and the grid control system uses the PSO-PI

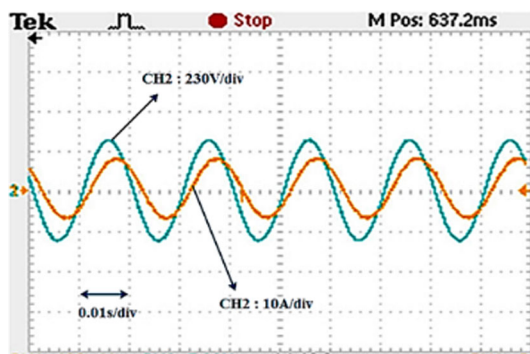


Fig. 22 Experimental Output of Grid Voltage and Grid Current Under Transient Condition

current and voltage controllers. Metaheuristic optimization algorithms are implemented to find a better output for the proposed system. Each algorithm has its own unique flow, its own tuning parameters, its own advantages and disadvantages. Moreover, a new algorithm can outperform the other algorithms based on, the computational speed, accuracy and other parameters. But it can fail to do so in another criterion. Which means that it can have adverse impact on the performance of system, as opposed to another one. The experimental investigation is carried out in the laboratory with an FPGA processor in arriving at the reduction of three possible harmonic orders for a 9-level inverter. From the results it is observed that, SHE-PSO method produces the output with less content of harmonics, which is acceptable based on the IEEE519 standards. PSO has superior performance than other methods since it has an inbuilt guidance strategy which lets the solutions to obtain a useful information from the better solutions and thereby helping them to improve their own solutions. Moreover, the results of PSO are faster convergence for the solutions. The experimental investigations for the GCPVS with cascaded controller is carried out for a 1kWp solar PV system in which the results satisfy the standards for harmonic reduction. The advantages of the proposed system include simple control, less complexity, lower THD, and avoids the usage of output transformers, and front-end rectifiers.

Declarations

Conflict of interest The authors have no conflict of interest.

Ethical approval This article does not contain any studies with human participants or animals performed by any of the authors.

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