Electrical Engineering (2022) 104:3107–3117
https://doi.org/10.1007/s00202-022-01535-2

ORIGINAL PAPER

Switched capacitors-based single-phase seven-level photovoltaic inverter with self-voltage balancing

Ritika Agarwal[1] · Krishna Kumar Gupta[1] · Shakti Singh[1]

Received: 2 June 2021 / Accepted: 1 March 2022 / Published online: 25 March 2022

Abstract

In this paper, a novel switched capacitors-based seven-level photovoltaic inverter having self-voltage boosting with reduced power switches is analyzed. It has voltage boosting capability with a possibility of 1.5 times of maximum voltage level to input DC voltage. In the proposed topology, higher voltage gain does not impose high voltage stress on any power switches. Therefore, the peak inverse voltage (PIV) of all power switches does not exceed the input source voltage. Furthermore, only a single source is enough, and voltage balancing of capacitors is not required as capacitors are balanced through the charging and discharging phenomenon. A simple modulation technique is used for generating a suitable switching pulses for the inverter. A comparative analysis is presented with other switched capacitors multilevel inverter in terms of the number of power switches, total standing voltage, PIV, and cost function. The closed-loop structure of proposed inverter is investigated with specified controlling and implemented in MATLAB/Simulink and validated through hardware-in-the-loop real-time simulation in OPAL-RT. Additionally, an experimental prototype of the proposed topology in open as well as closed loop is built and tested to validate its efficacy.

Keywords Multilevel inverter · Switched-capacitors · Voltage boosting

1 Introduction

The multilevel inverters (MLIs) has emerged as an enabling technology for the conversion of power. It has been broadly examined for its wide range of low-, medium-, and high-power applications. As inherent advantages of improved power quality, lower voltage stress, improved efficiency, and high modularity, etc., are the key factor for growth and increasing demand of MLIs in industries, electric vehicles, high-frequency AC power distribution systems, and renewable power generation [1,22,25]. Conventional types of a multilevel inverter are categorized into three following categories, i.e., neutral point clamped (NPC) [14], flying capacitor (FC) [9], and cascade H-bridge (CHB) [13]. For producing a large number of levels, NPC topology needs more diodes and power switches. Additionally, there is a problem of unbalancing capacitors voltage in NPC topology [6]. Similar to FC topology, more capacitors are used to produce more levels leading to higher cost of the system. In comparison with NPC and FC, there is no use of clamping diode in CHB, and voltage stress is also very low. Though, in CHB, numerous independent power supplies are required [5]. In a general MLI with self-balancing voltage ability, capacitor voltage can be balanced without any additional circuit [16]. FC and NPC can be deduced from this general purpose MLI but this structure requires too many power devices. Additionally, many researchers projected a variety of new and advanced topologies to create more voltage levels. In [20] and [19], researchers move toward the topology of the T-type and E-type back-to-back converter which uses uneven DC source. In [2] and [3], a cascaded multilevel inverter with a reduced number of power switches is projected. Due to the cascade structure, it uses more DC source. To overcome this problem and to produce more levels with reduction in total harmonic distortion (THD), a conventional MLI-based series of hybrid MLI with fault-tolerant capability was developed [15], [8]. In the case of active NPC, hybrid inverter combines toughness of NPC and the adaptability of FC [4]. A five-level inverter topology integrating FC with a H-bridge was developed to reduce the total standing voltage (TSV) [18]. To overcome the problem of inherent

✉ Ritika Agarwal
ritikaagarwal290@gmail.com

[1] Thapar Institute of Engineering and Technology, Patiala, Punjab, India

balancing of capacitors, switched capacitors MLI (SCMLI) topologies have gained more attention in recent years. These topologies solved the problem of unbalancing capacitor voltage and has ability to produce a higher number of voltage levels with only a single voltage source. In [10], switched capacitor topology was proposed with voltage stress equal to DC input voltage but with an increasing number of power switches and gate drivers. A two-stage structure SCMLI with front end as switched capacitors and back end as H-bridge having high voltage stress and TSV was proposed [7]. In [23], a SCMLI was proposed, limiting its application due to more power switches and gate drivers. Topologies with less power switches, having two voltage sources and large voltage stress across switches, are presented [17]. The SCMLI in [11,21,24] has low voltage stress, but cost function (CF) increases with device count.

In the literature described above, the topologies have disadvantages, namely high PIV on power switches, unbalancing of capacitors, high number of power switches, and multiple DC source. To overcome all these disadvantages, a novel SCMLI topology is presented in this paper, having the following features:

1. The voltage stress across the power switches has a maximum value of V_{DC}.
2. Ability to generate seven-level output voltage with the help of nine switches.
3. Single DC source/DC link is used for single-phase and three-phase topologies.
4. All capacitors are self-balanced by using proper switching states.
5. Low value of CF owing to reduced device count.

The paper is organized into seven sections: Section 2 outlines the description of topology and modes of operation. The modulation technique is presented in Section 3. In Section 4, the ratings of components and design of capacitors are discussed. A comparative analysis with other SCMLI to validate the advantage of the proposed topology is presented in Section 5. Simulation and experimental results of the proposed SCMLI are presented in Section 6. Lastly, closed-loop control of proposed inverter is presented in Section 7

2 Description of topology

2.1 Circuit Topology

The structure of the proposed seven-level inverter is shown in Fig. 1. It has nine power switches and four capacitors. Each power switch in this topology consists of a transistor (MOSFET) with an anti-parallel diode. The output voltage is labeled as V_{ao}. The DC link consists of two parallel-connected capacitors C_1 and C_2 whose voltages are rated at half of the DC voltage. Input voltage is obtained from the PV panel which is V_{DC}. One DC source is sufficient to produce seven level of voltages ($0, \pm 0.5V_{\mathrm{DC}}, \pm V_{\mathrm{DC}}, \pm 1.5V_{\mathrm{DC}}$).

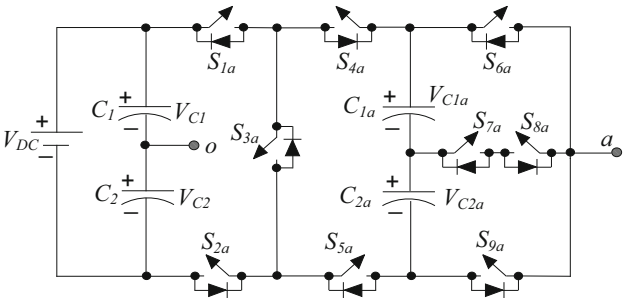

Fig. 1 Schematic circuit of proposed seven-level inverter

2.2 Modes of Operations

All the valid operating states for the proposed seven-level inverter are shown in Fig. 2. The path through which capacitors are charged is shown in red, and the load current path is shown in blue. Table 1 represents the switching states of the proposed topology in which '1' and '0' represent the ON and OFF operation of power switches in particular state. Switching states of $S_{1a} = S_{5a}$, $S_{2a} = S_{4a}$ and $S_{7a} = S_{8a}$. Capacitors states of capacitors (C_{1a}, C_{2a}) are represented by 'C' (charging state), 'D' (discharging state), and '-' (idle state). The states are described below.

1. State $\lambda_1 \& \lambda_5$: In this state, the output voltage $V_{ao} = 0$ with continuous conduction of power switches S_{1a}, S_{2a}, S_{4a}, S_{5a}, S_{7a}, and S_{8a}, while power switches S_{3a}, S_{6a}, and S_{9a} are OFF. As a result, the capacitors C_1, C_2, C_{1a}, and C_{2a} are parallel with the DC source and hence get charged to voltage $0.5V_{\mathrm{DC}}$ as shown in Fig. 2a.
2. State λ_2: In this state, with continuous conduction of power switches S_{1a}, S_{2a}, S_{4a}, S_{5a}, and S_{6a}, while power switches S_{3a}, S_{7a}, S_{8a}, and S_{9a} are OFF, the output voltage of $V_{ao} = V_{\mathrm{C1}} = 0.5V_{\mathrm{DC}}$ is obtained. As a result, the capacitors C_1, C_2, C_{1a}, and C_{2a} are parallel with the DC source and hence get charge to voltage $0.5V_{\mathrm{DC}}$ as shown in Fig. 2b.
3. State λ_3: In this state, with continuous conduction of power switches S_{1a}, S_{3a}, S_{5a}, S_{7a}, and S_{8a}, while power switches S_{2a}, S_{4a}, S_{6a}, and S_{9a} are OFF. Thus, the output voltage is $V_{ao} = V_{C1} + V_{C2a} = V_{\mathrm{DC}}$ as shown in Fig. 2c.
4. State λ_4: In this state, with continuous conduction of power switches S_{1a}, S_{3a}, S_{5a}, and S_{6a}, while power switches S_{2a}, S_{4a}, S_{7a}, S_{8a}, and S_{9a} are OFF. As a result, the output voltage is $V_{ao} = V_{C1} + V_{C1a} + V_{C2a} = 1.5V_{\mathrm{DC}}$ as shown in Fig. 2d.

Table 1 Switching states of the proposed topology

States	V_{ao}	Power switches						Capacitors	
		S_{1a}/S_{5a}	S_{2a}/S_{4a}	S_{3a}	S_{6a}	S_{7a}/S_{8a}	S_{9a}	C_{1a}	C_{2a}
λ_1, λ_5	0	1	1	0	0	1	0	C	C
λ_2	$0.5V_{dc}$	1	1	0	1	0	0	C	C
λ_3	V_{dc}	1	0	1	0	1	0	–	D
λ_4	$1.5V_{dc}$	1	0	1	1	0	0	D	D
λ_6	$-0.5V_{dc}$	1	1	0	0	0	1	C	C
λ_7	$-V_{dc}$	0	1	1	0	1	0	D	–
λ_8	$-1.5V_{dc}$	0	1	1	0	0	1	D	D

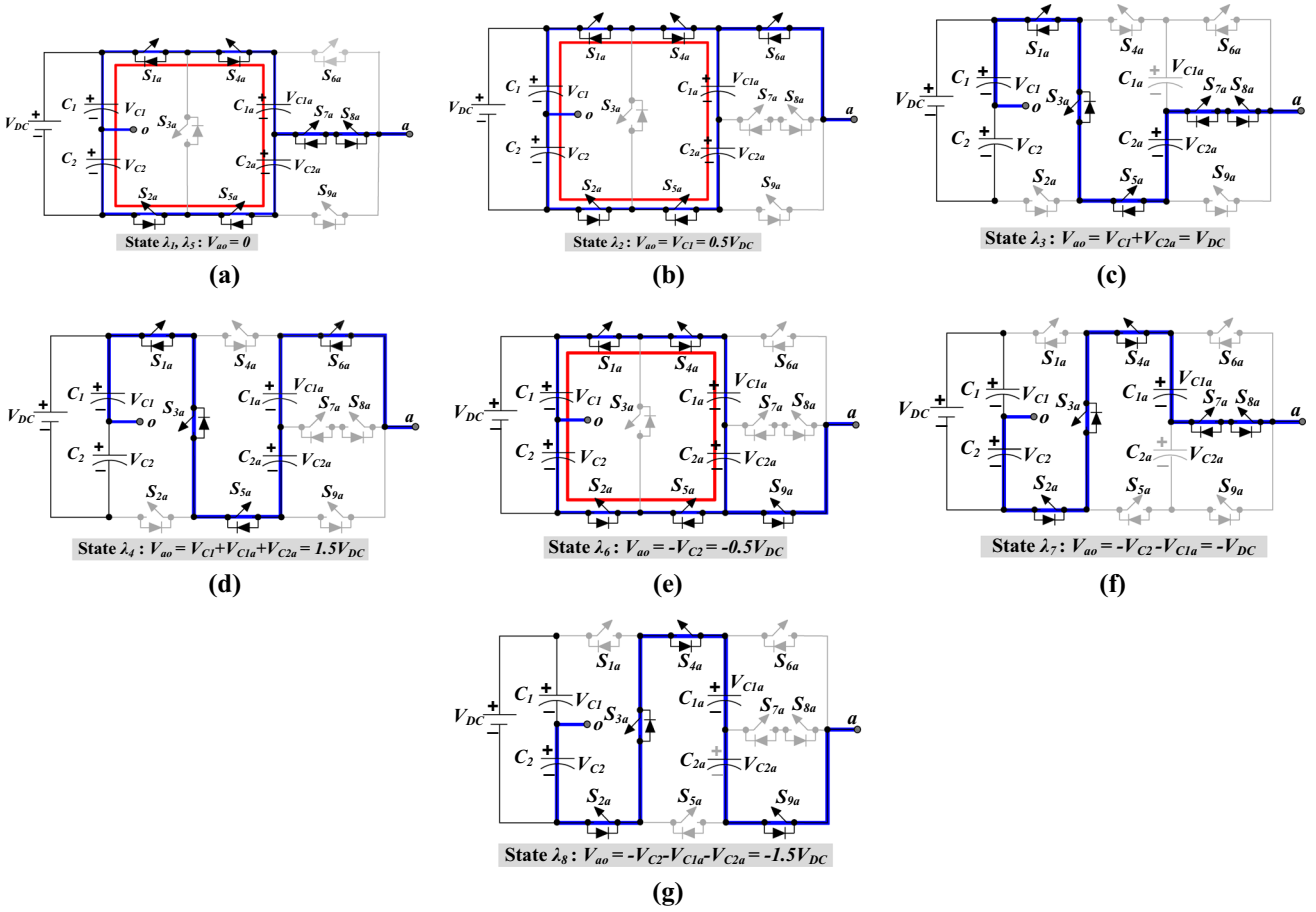

Fig. 2 Different states of the proposed seven-level inverter **a** 0, **b** $0.5V_{DC}$, **c** V_{DC}, **d** $1.5V_{DC}$, **e** $-0.5V_{DC}$, **f** $-V_{DC}$, **g** $-1.5V_{DC}$

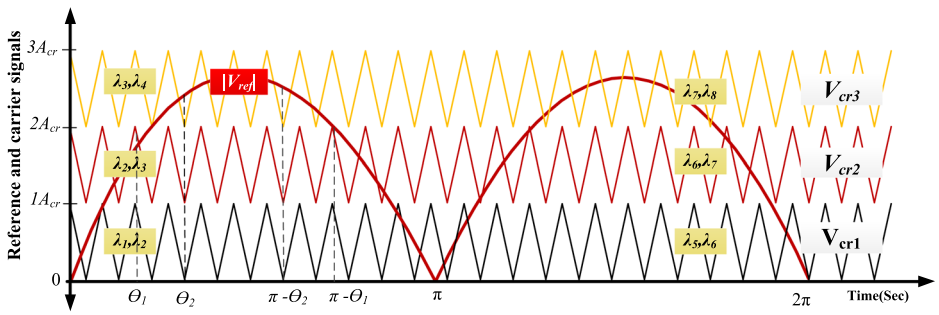

Fig. 3 Reference and carrier waveforms to modulate the proposed seven-level inverter

5. State λ_6: In this state, with continuous conduction of power switches S_{1a}, S_{2a}, S_{4a}, S_{5a}, and S_{9a}, while power switches S_{3a}, S_{6a}, S_{7a}, and S_{8a} are OFF. As a result, the output voltage is $V_{ao} = -V_{C2} = -0.5V_{\mathrm{DC}}$ as shown in Fig. 2e.
6. State λ_7: In this state, with continuous conduction of power switches S_{2a}, S_{3a}, S_{4a}, S_{7a}, and S_{8a}, while power switches S_{1a}, S_{5a}, S_{6a}, and S_{9a} are OFF. As a result, the output voltage is $V_{ao} = -V_{C2} - V_{C1a} = -V_{\mathrm{DC}}$ as shown in Fig. 2f.
7. State λ_8: In this state, with continuous conduction of power switches S_{2a}, S_{3a}, S_{4a}, and S_{9a} while power switches S_{1a}, S_{5a}, S_{6a}, S_{7a}, and S_{8a} are OFF. As a result, the output voltage is $V_{ao} = -V_{C2} - V_{C1a} - V_{C2a} = -1.5V_{\mathrm{DC}}$ as shown in Fig. 2g.

3 Modulation strategy

Various methods are used for modulation of multilevel inverters, namely high-switching-frequency methods [9] and low-switching-frequency methods. The proposed topology can be modulated with any of these methods with an appropriate alteration. This topology is modulated by using level-shifted pulse width modulation (LSPWM) technique as shown in Fig. 3. In this scheme, triangular carrier signals are used to compare with sinusoidal reference signal and resultant pulse signals are used to provide switching to the power devices corresponding to the particular voltage level. As shown in Fig. 3, three carrier waveforms $V_{\mathrm{cr}j}$ ($j = 1$ to 3) of the same frequency (f_{cr}), phase, and peak-to-peak value (A_{cr}) are used for carriers. A sinusoidal waveform (V_{ref}) having amplitude (A_{ref}) and frequency (f_{ref}) are taken as the reference signal, and its absolute value $|V_{\mathrm{ref}}|$ is compared with the carriers. Therefore, modulation index *(M)* is denoted as:

$$M = \frac{A_{\mathrm{ref}}}{3 \times A_{\mathrm{cr}}} \tag{1}$$

where A_{cr} and A_{ref} are amplitude of the carrier and reference waveform, respectively.

Various operating states are shown in Fig. 3 for the complete power cycle, i.e., during $0 \leq \omega t \leq 2\pi$. It can be seen that during $0 \leq \omega t \leq \pi$ interval, V_{cr1} is compared with $|V_{\mathrm{ref}}|$, the estimated voltage levels are $(0, 0.5V_{\mathrm{DC}})$ which are obtained by imposing gate signals for states (λ_1, λ_2). In the same way, when V_{cr2} and V_{cr3} are compared with $|V_{\mathrm{ref}}|$, the estimated levels during $0 \leq \omega t \leq \pi$ are $(0.5V_{\mathrm{DC}}, V_{\mathrm{DC}})$ and $(V_{\mathrm{DC}}, 1.5V_{\mathrm{DC}})$ which are obtained by imposing gate signals for states (λ_2, λ_3) and (λ_3, λ_4). For the other half cycle, i.e., during $\pi \leq \omega t \leq 2\pi$, the states for the negative half cycle are to be enacted and zero levels are obtained by the state λ_5. Therefore, for $\pi \leq \omega t \leq 2\pi$, when V_{cr1}, V_{cr2}, and V_{cr3} are compared with $|V_{\mathrm{ref}}|$, the estimated levels are $(0, -0.5V_{\mathrm{DC}})$, $(-0.5V_{\mathrm{DC}}, -V_{\mathrm{DC}})$ and $(-V_{\mathrm{DC}}, -1.5V_{\mathrm{DC}})$ which are obtained by imposing gate signals for states (λ_5, λ_6), (λ_6, λ_7) and (λ_7, λ_8). Based on the abovementioned description, the execution of the state-selection logic is given in Fig. 4, in which gate signals for specific states are first obtained, and finally fed to OR gates for obtaining respective firing pulses for each power switch.

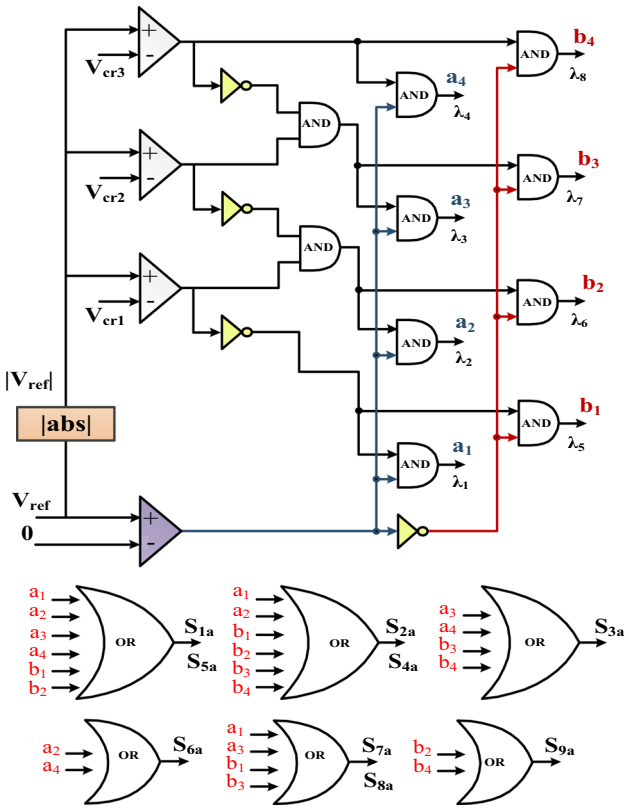

Fig. 4 Logic gates-based implementation of modulation scheme

4 Ratings of components and designing of capacitors

4.1 Voltage and Current Rating

PIV for the power switches in the proposed topology is shown in Table 2. The PIV rating of switches S_{7a} and S_{8a} is $\approx$ 34%

Table 2 PIV of power switches

PIV	Power switches
$0.5V_{\mathrm{DC}}$	S_{7a}, S_{8a}
V_{DC}	S_{1a}, S_{2a}, S_{3a}, S_{4a}, S_{5a}, S_{6a}, S_{9a}

of the operating voltage and for remaining switches, it is $\approx$ 67% of the operating voltage.

Besides, the minimum current ratings of power switches are shown in Table 3. Four power switches (S_{6a}, S_{7a}, S_{8a}, and S_{9a}) need to carry only the load current (I_{ac}), and hence they should be rated at least at the value equal to the amplitude of the load current (I_{ac}). Considering, unity factor load case with power ratings equal to P_r, I_{ac} can be calculated as:

$$I_{ac} = \frac{\sqrt{2} \times P_r}{1.5 \times M \times V_{DC}} \tag{2}$$

where M is modulation index defined in Eq. (1)

The switches S_{1a}, S_{2a}, S_{4a}, and S_{5a} need to carry two currents, the load current (I_{ac}) and the charging current (I_C) for the capacitors C_{1a} and C_{2a}, and hence it should be rated at least equal to the sum of their peak values. The path for I_C is shown in Fig. 5, and it can be calculated as:

$$I_C = \left(\frac{V_{eq}}{R_{eq}}\right) \times \exp\left(-\frac{t}{R_{eq} \times \frac{C_{1a} \times C_{2a}}{C_{1a}+C_{2a}}}\right) \tag{3}$$

where

$$\begin{aligned} V_{eq} &= V_{DC} - V_{D4a} - V_{C1a} - V_{D5a} - V_{C2a} \\ R_{eq} &= r_{D4a} + r_{D5a} + r_{S_{1a}} + r_{S_{2a}} + R_{ESR_{C1aC2a}} \end{aligned} \tag{4}$$

Therefore, V_{D4a} and V_{D5a} are the on-state voltage drops across the diodes of switches S_{4a} and S_{5a}, respectively. V_{C1a}

Table 3 Current through power switches

Current stress	Power switches
I_{ac}	S_{3a}, S_{6a}, S_{7a}, S_{8a}, S_{9a}
$I_{ac} + I_C$	S_{1a}, S_{2a}, S_{4a}, S_{5a}

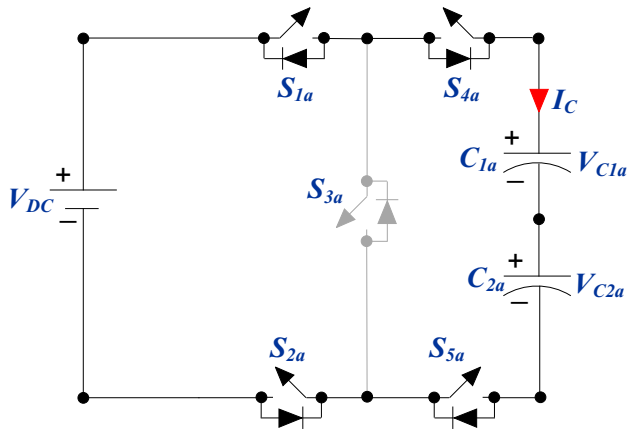

Fig. 5 Charging path for capacitors C_{1a} and C_{2a}

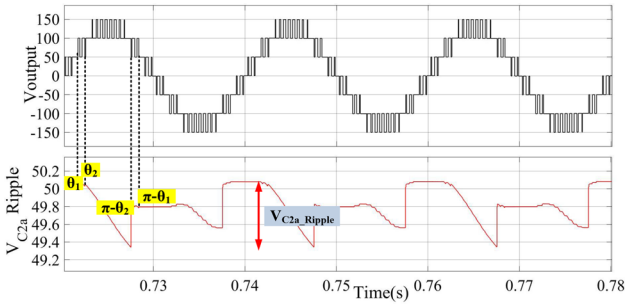

Fig. 6 Ripple voltage across capacitor C_{2a}

and V_{C2a} are the voltages across capacitors C_{1a} and C_{2a}, respectively. r_{D4a}, r_{D5a}, r_{S1a}, and r_{S2a} are the respective on-state resistances of the diode S_{4a}, the diode of S_{5a}, transistor part of S_{1a}, and transistor part of S_{2a}, and $R_{ESR_{C1aC2a}}$ is the equivalent series resistance (ESR) of the series combination of C_{1a} and C_{2a}.

4.2 Designing of Capacitors

Two capacitors C_{1a} and C_{2a} are maintained at $0.5V_{DC}$ each in the proposed inverter by using the principle of switched capacitor technique. Ripples that appear on them should not be more than 10% of the desired capacitors voltage when they discharge from supply to load [12]. The voltage ripple across the capacitors is determined by discharging time and the current across the load. The worst situation is when a load is purely resistive [7]. In capacitors C_{1a} and C_{2a}, continuous maximum discharging happens in interval θ_1 to $\pi - \theta_1$ in the positive and negative cycle when obtaining continuously output voltage levels of $+V_{DC}$, $+1.5V_{DC}$, and $-V_{DC}$, $-1.5V_{DC}$ as shown in Fig. 6. The maximum discharge for resistive load R_L can be described as:

For C_{1a},

$$\begin{aligned} \Delta Q_{C1a} &= C_{1a} \times \Delta V_{C1a} \\ &= \int_{\frac{\theta_1}{\omega}}^{\frac{\theta_2}{\omega}} \frac{V_{DC}}{R_L}\, dt + \int_{\frac{\theta_2}{\omega}}^{\frac{\pi-\theta_2}{\omega}} \frac{1.5V_{DC}}{R_L}\, dt + \int_{\frac{\pi-\theta_2}{\omega}}^{\frac{\pi-\theta_1}{\omega}} \frac{V_{DC}}{R_L}\, dt \end{aligned} \tag{5}$$

By solving this

$$\Delta Q_{C1a} = \frac{V_{DC}}{\omega \times R_L} \times (1.5\pi - 2\theta_1 - \theta_2) \tag{6}$$

And, Figure 3 shows that

$$\theta_1 = \sin^{-1}\left(\frac{1}{3M}\right) \tag{7}$$

$$\theta_2 = \sin^{-1}\left(\frac{2}{3M}\right) \tag{8}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C1a}}{0.5V_{DC}} \leq 10 \tag{9}$$

Using these equations, we have:

$$C_{1a} \geq \frac{20}{2\pi \times f \times R_L}\left[1.5\pi - 2\sin^{-1}\left(\frac{1}{3M}\right) - \sin^{-1}\left(\frac{2}{3M}\right)\right] \tag{10}$$

A similar analysis for C_{2a} would show that it is equal to C_{1a}, i.e.,

$$C_{1a} = C_{2a} \tag{11}$$

5 Comparison with other topologies

Switched capacitor-based multilevel inverter topology offers a high voltage gain and self-balancing capability, whereas conventional topology like cascade H-bridge, diode clamped and flying capacitor offers a unity voltage gain but requires multiple DC source, more number of components which leads to increase in cost function. A proposed seven-level topology is compared with other recent seven-level topologies. The components for comparison are the number of levels (N_L), number of power switches (N_S), number of gate drivers (N_{GD}), number of isolated source (N_{IS}), number of diodes (N_D), number of capacitors (N_C), PIV, TSV, and cost function (CF). Table 4 presented in this section summarized the comparative study of the proposed topology. Equal importance has been given to all the parameters, while calculating CF which is further defined as:

$$\mathrm{CF} = \left(N_S + N_{GD} + N_D + N_C + \frac{\alpha \times TSV}{\beta}\right) \times \left(\frac{N_{IS}}{N_L}\right) \tag{12}$$

where α is the weighing factor for assigning weightage to TSV in comparison with the component count and β is the voltage gain. Higher voltage gain reduces the requirement of any boosting circuit; however, it may lead to higher PIVs across the switches. As shown in Table 4, [7] has higher PIV and CF compared to the proposed topology. The topology proposed in [17] has less number of switches; however, it requires multiple DC source and power diodes. Although the topologies of [11,21,24] have a lower number of capacitors than the proposed one; however, these topologies have high TSV and high CF. From the resultant CF shown in Table 4, the proposed topology gives the less CF as compared to other topologies which implies that the proposed topology has better structural features.

6 Experimental Verification

The simulation results of the proposed seven-level inverter are taken in the MATLAB/SIMULINK to validate its practicability. In Table 5, simulation parameters are described. Modulation index M is set to 0.85. Figure 7 presents the voltage and current output waveforms with a resistive load of 500 Ω. Figure 8 presents the voltage and current output waveforms under R–L load of 50 Ω and 120 mH. The proposed topology can generate seven levels with the amplitude of output voltage being 150V, and amplitude of output current changes with respect to change in load.

Figures 9 and 10 depict the total harmonics distortion (THD) of output voltage and current under R–L load of 50 Ω and 120 mH in which it can be seen that THD of output voltage and current is 23.09% and 0.96%, respectively. Figure 11

Table 4 Comparison of proposed topology with other seven-level topologies

Components	[10]	[7]	[23]	[17]	[21]	[24]	[11]	Proposed
N_L	7	7	7	7	7	7	7	7
N_S	10	10	16	7	12	14	10	9
N_{GD}	10	10	16	7	12	14	10	9
N_{IS}	1	1	1	2	1	1	1	1
N_D	0	0	0	2	0	0	0	0
N_C	4	2	2	1	2	2	3	4
TSV	9	18	16	8.5	16	14	13.5	8
PIV	1	3	2	1.5	2	1	1	1
β	1.5	3	3	1.5	3	3	1.5	1.5
CF at $\alpha = 0.5$	3.85	3.57	5.23	5.66	4.09	4.62	3.92	3.52
at $\alpha = 1.5$	4.71	4.42	6.00	7.28	4.85	5.28	5.17	4.28

Table 5 Parameters of simulation

Parameters	Values
DC source	100 V
Capacitors (C_1, C_2, C_{1a}, C_{2a})	1600 µF
Switching frequency (f_{SW})	2000 Hz
Fundamental frequency (f)	50 Hz
Resistive load (R_L)	500 Ω

Table 6 Experimental parameters

Parameters	Values
MOSFET	SiHG47N60E
Isolated gate driver IC	Si8275
Capacitors (C_1, C_2, C_{1a}, C_{2a})	1600 µF
Controller	Opal-RT OP4510
Resistive load (R_L)	500 Ω

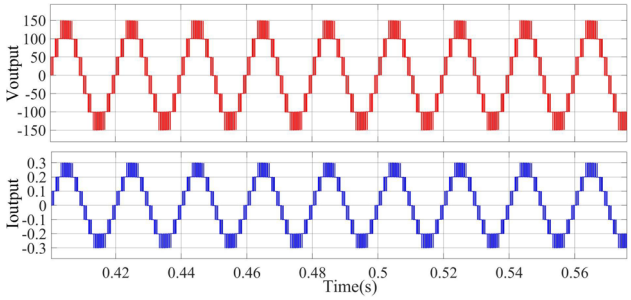

Fig. 7 Simulation waveforms of the output voltage and current with resistive load

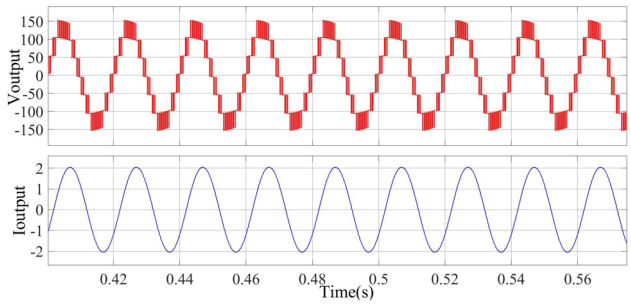

Fig. 8 Simulation waveforms of the output voltage and current with R–L load

shows the current through capacitors C_1, C_2, C_{1a}, and C_{2a} under R–L load of 50 Ω and 120 mH. Figure 12 represents a sudden change in the load. For $t < 1$ s, the load comprises resistance 50 Ω and inductance 120 mH. After $t = 1$ s load change to half the previous value of resistance 25 Ω and inductance 60 mH. Therefore, load current is changed significantly and gets double by decreasing load to half of the earlier values.

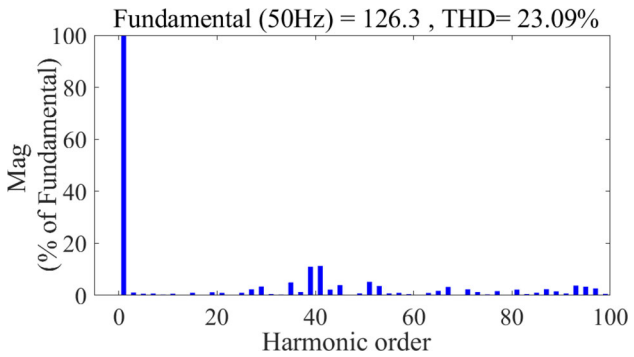

Fig. 9 Harmonic profile of the output voltage

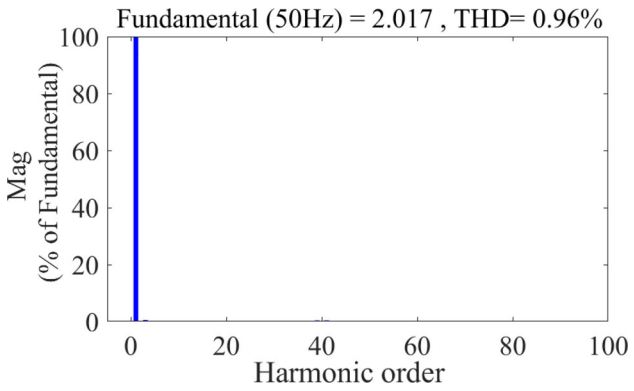

Fig. 10 Harmonic profile of the output current

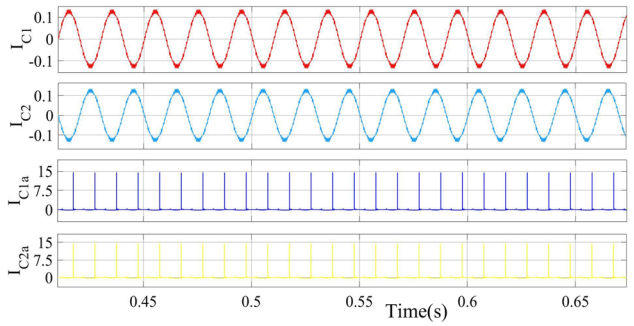

Fig. 11 Current through capacitors C_1, C_2, C_{1a}, and C_{2a}

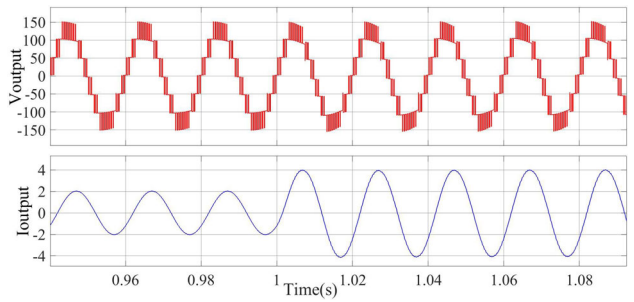

Fig. 12 Waveforms of load voltage and current for transition in load from (50 Ω, 120 mH) to (25 Ω, 60 mH)

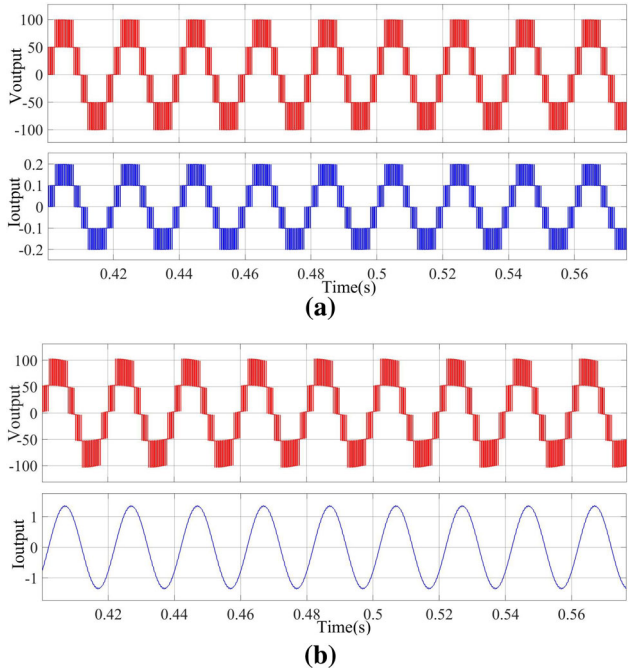

Fig. 13 Output voltage and current waveforms for modulation index of 0.55 **a** resitive load **b** R–L load

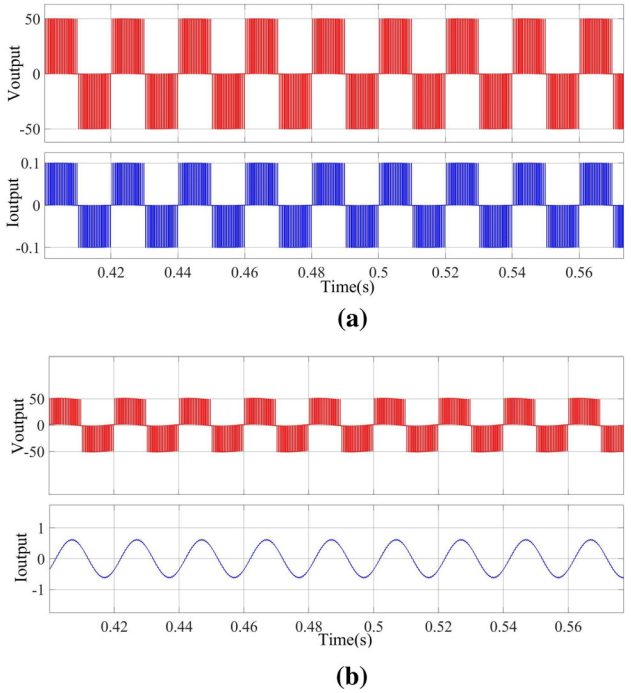

Fig. 14 Output voltage and current waveforms for modulation index of 0.25 **a** resitive load **b** R–L load

The waveforms at lower modulation indexes of 0.55 and 0.25 are shown in Figs. 13 and 14 , respectively. Figures 13a and 14a present the voltage and current output waveforms with a resistive load of 500 Ω having reduced levels with less peak value. Figures 13b and 14b present the voltage and current output waveforms under R–L load of 50 Ω and 120 mH. The waveforms for the over-modulation index of 1.25 are shown in Fig. 15. Figure 15a presents the voltage and current output waveforms with a resistive load of 500 Ω. Figure 15b presents the voltage and current output waveforms under R–L load of 50 Ω and 120 mH. Zero level is present in every value of the modulation index. At this level, all the capacitors (C_1, C_2, C_{1a}, and C_{2a}) are in parallel with the DC source which implies all the capacitors are balanced at their desired voltages.

A prototype of the proposed seven-level SCMLI is designed further to validate the analysis and simulation results. A fixed DC voltage of 100V from PV emulator is used as an input source. The device values chosen for the prototype are shown in Table 6. The experimental photograph is shown in Fig. 16. OPAL-RT (OP4510) real-time controller was used in conjunction with MATLAB/Simulink to generate the desired gate signals for the power switches. These signals are obtained for modulation index of 0.85 and fsw=2KHz. Figure 17 shows the voltage and current output waveforms under a resistive load of 500 Ω. The amplitude of output voltage and current is 150V and 0.3A, respectively. Figure 18 shows that capacitors C_1, C_2, C_{1a}, and C_{2a} gets approximately charged to 50V, and they are within the

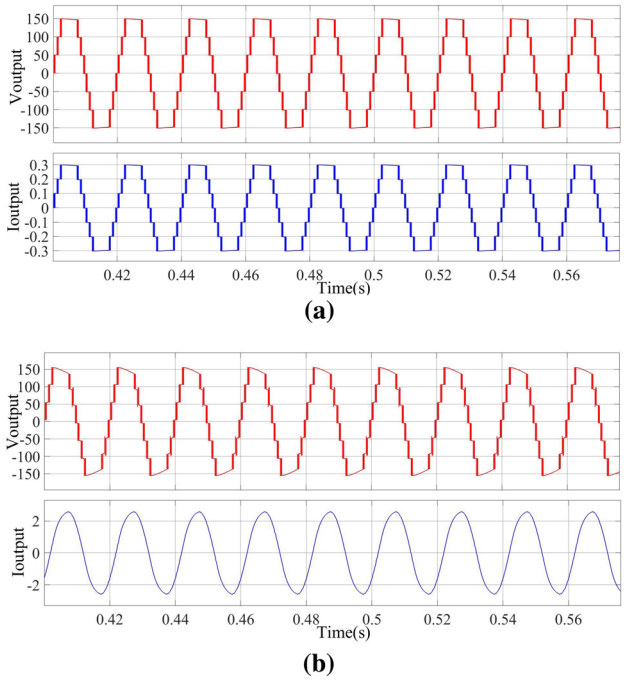

Fig. 15 Output voltage and current waveforms for modulation index of 1.25 **a** resitive load **b** R–L load

range of 10% voltage ripples. Figures 19 and 20 depict the voltage waveforms of switches S_{1a} to S_{9a}. The PIV of the bidirectional switch (S_{7a}, S_{8a}) is 50V for each, and for other switches, it is 100V. Therefore, PIV across the switches does not exceed input source. Figure 21 shows the voltage and cur-

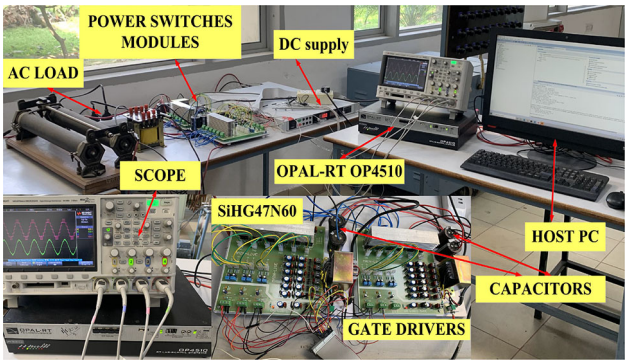

Fig. 16 Photograph of experimental setup

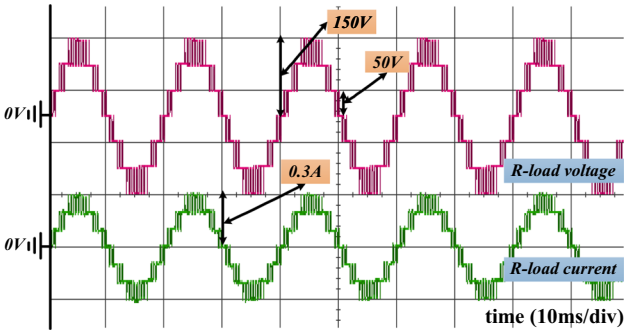

Fig. 17 Experimental waveforms of output voltage and current under resistive load

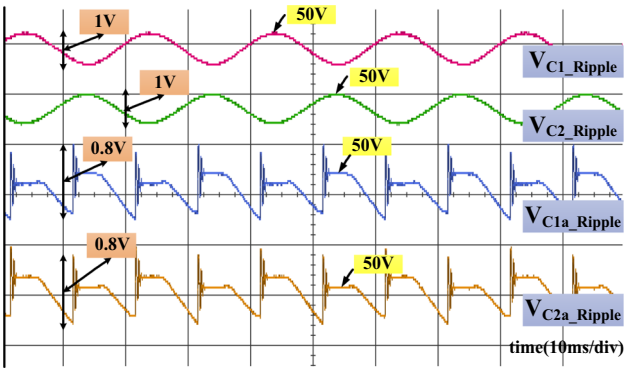

Fig. 18 Voltages across capacitors C_1, C_2, C_{1a} and C_{2a}

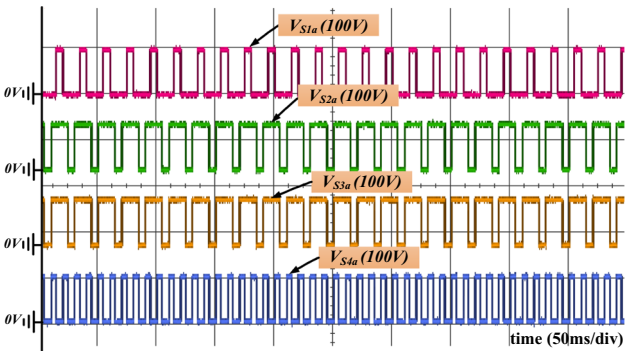

Fig. 19 Switching signals for power switches S_{1a}, S_{2a}, S_{3a} and S_{4a}

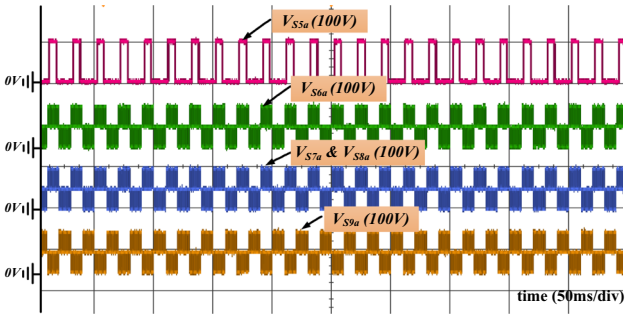

Fig. 20 Switching signals for power switches S_{1a}, S_{2a}, S_{3a} and S_{4a}

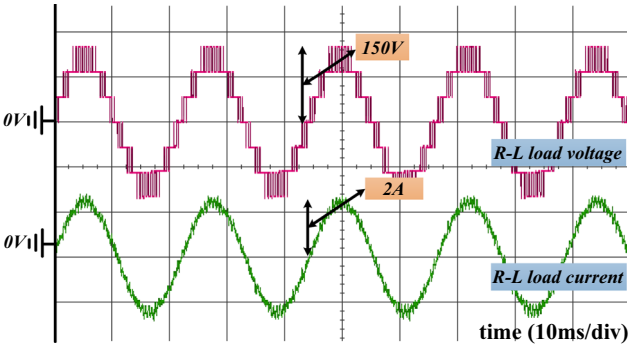

Fig. 21 Experimental waveforms of output voltage and current under R–L load

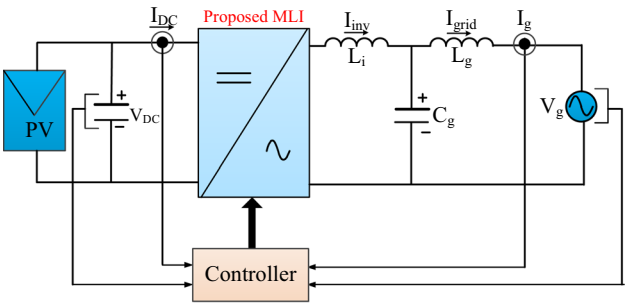

Fig. 22 Closed-loop structure of proposed inverter

rent output waveforms under R–L load of 50 Ω and 120 mH. The amplitude of output voltage and current is 150V and 2A, respectively.

7 Closed-loop control of proposed inverter

Closed-loop structure of the proposed inverter is shown in Fig. 22. The main components of this structure are PV array, proposed SC-MLI, LCL filter to improve THD, controller, and the utility grid. The controller of this structure consists of a maximum power point tracker (MPPT) algorithm using perturb and observe method, and phase-locked loop (PLL) is utilized to extract the voltage angle and generate the synchronized current reference.

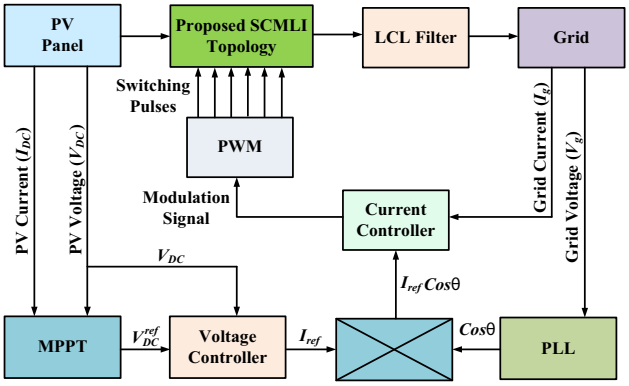

Fig. 23 Block diagram of voltage and current controller

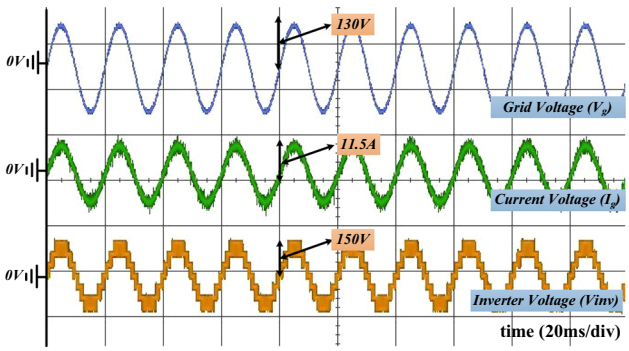

Fig. 24 Waveform of grid voltage, grid current and inverter voltage

In this work, voltage and current are controlled by the proportional integral and proportional resonant controller, respectively. In Fig. 23, components of controller are shown in which output (V_{DC}^{ref}) from MPPT block and source voltage (V_{DC}) is fed to voltage controller which produces reference signal (I_{ref}) which multiplied with signal (Cos`) from PLL block to produce reference grid current ($I_{ref}$Cos`) which further fed to current controller. It produces the desired reference signal which further processes with PWM, described in Sect. 3, and generates a switching pulse. These pulses are fed to the power switches of the proposed inverter.

The closed-loop performance characteristic is shown in Fig. 24 in which the grid voltage is in phase with grid current and hence maintains unity power factor with amplitudes 130V and 11.5A, respectively.

8 Conclusion

A novel seven-level PV inverter is described in this paper, having advantages over different SCMLI topologies. Nine switches and four capacitors are used in the proposed topology to generate seven-level with voltage stress across all switches controlled within the input voltage. The maximum attainable voltage level was 1.5 times the input voltage. The LSPWM algorithm improves the quality of its output voltage and reduces the capacitors voltage ripples simultaneously. Self-voltage balancing of capacitors and a single DC source are also some of the attractive features of the proposed inverter. By using voltage and current controller, closed-loop PV connected grid system is presented. Theoretical analyses were shown and proved by the experimental study of a single-phase prototype.

References

1. Abu-Rub H, Holtz J, Rodriguez J, Baoming G (2010) Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications. IEEE Trans Ind Electron 57(8):2581–2596. https://doi.org/10.1109/TIE.2010.2043039
2. Babaei E (2008) A cascade multilevel converter topology with reduced number of switches. IEEE Trans Power Electron 23(6):2657–2664. https://doi.org/10.1109/TPEL.2008.2005192
3. Babaei E, Alilu S, Laali S (2014) A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge. IEEE Trans Ind Electron 61(8):3932–3939. https://doi.org/10.1109/TIE.2013.2286561
4. Barbosa P, Steimer P, Steinke J, Winkelnkemper M, Celanovic N (2005) Active-neutral-point-clamped (ANPC) multilevel converter technology. In: 2005 European conference on power electronics and applications, p 10. https://doi.org/10.1109/EPE.2005.219713
5. Gupta K, Jain S (2012) Topology for multilevel inverters to attain maximum number of levels from given dc sources. IET Power Electron 5:435–446. https://doi.org/10.1049/iet-pel.2011.0178
6. He L, Cheng C (2016) A flying-capacitor-clamped five-level inverter based on bridge modular switched-capacitor topology. IEEE Trans Ind Electron 63(12):7814–7822. https://doi.org/10.1109/TIE.2016.2607155
7. Hinago Y, Koizumi H (2012) A switched-capacitor inverter using series/parallel conversion with inductive load. IEEE Trans Ind Electron 59(2):878–887. https://doi.org/10.1109/TIE.2011.2158768
8. Kumar PR, Kaarthik RS, Gopakumar K, Leon JI, Franquelo LG (2015) Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges. IEEE Trans Power Electron 30(7):3471–3478. https://doi.org/10.1109/TPEL.2014.2342882
9. Lai JS, Peng FZ (1996) Multilevel converters—a new breed of power converters. IEEE Trans Ind Appl 32(3):509–517. https://doi.org/10.1109/28.502161
10. Lee SS, Bak Y, Kim SM, Joseph A, Lee KB (2019) New family of boost switched-capacitor seven-level inverters (BSC7LI). IEEE Trans Power Electron 34(11):10471–10479. https://doi.org/10.1109/TPEL.2019.2896606
11. Lee SS, Lim CS, Siwakoti YP, Lee KB (2020) Hybrid 7-level boost active-neutral-point-clamped (H-7L-BANPC) inverter. IEEE Trans Circuits Syst II Express Briefs 67(10):2044–2048. https://doi.org/10.1109/TCSII.2019.2946860
12. Liu J, Wu J, Zeng J, Guo H (2017) A novel nine-level inverter employing one voltage source and reduced components as high-frequency AC power source. IEEE Trans Power Electron 32(4):2939–2947. https://doi.org/10.1109/TPEL.2016.2582206
13. Malinowski M, Gopakumar K, Rodriguez J, Pérez MA (2010) A survey on cascaded multilevel inverters. IEEE Trans Ind Electron 57(7):2197–2206. https://doi.org/10.1109/TIE.2009.2030767
14. Nabae A, Takahashi I, Akagi H (1981) A new neutral-point-clamped PWM inverter. IEEE Trans Ind Appl 17(5):518–523. https://doi.org/10.1109/TIA.1981.4503992

15. Nair RV, Rahul SA, Kaarthik RS, Kshirsagar A, Gopakumar K (2017) Generation of higher number of voltage levels by stacking inverters of lower multilevel structures with low voltage devices for drives. IEEE Trans Power Electron 32(1):52–59. https://doi.org/10.1109/TPEL.2016.2528286
16. Peng FZ (2001) A generalized multilevel inverter topology with self voltage balancing. IEEE Trans Ind Appl 37(2):611–618. https://doi.org/10.1109/28.913728
17. Raman SR, Cheng KWE, Ye Y (2018) Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution. IEEE Trans Power Electron 33(7):5937–5948. https://doi.org/10.1109/TPEL.2017.2742525
18. Roshankumar P, Rajeevan PP, Mathew K, Gopakumar K, Leon JI, Franquelo LG (2012) A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge. IEEE Trans Power Electron 27(8):3505–3512. https://doi.org/10.1109/TPEL.2012.2185714
19. Samadaei E, Gholamian SA, Sheikholeslami A, Adabi J (2016) An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components. IEEE Trans Ind Electron 63(11):7148–7156. https://doi.org/10.1109/TIE.2016.2520913
20. Samadaei E, Sheikholeslami A, Gholamian SA, Adabi J (2018) A square t-type (ST-type) module for asymmetrical multilevel inverters. IEEE Trans Power Electron 33(2):987–996. https://doi.org/10.1109/TPEL.2017.2675381
21. Siddique MD, Mekhilef S, Shah NM, Ali JSM, Blaabjerg F (2020) A new switched capacitor 7L inverter with triple voltage gain and low voltage stress. IEEE Trans Circuits Syst II Express Briefs 67(7):1294–1298. https://doi.org/10.1109/TCSII.2019.2932480
22. Siwakoti YP, Mahajan A, Rogers DJ, Blaabjerg F (2019) A novel seven-level active neutral-point-clamped converter with reduced active switching devices and DC-link voltage. IEEE Trans Power Electron 34(11):10492–10508. https://doi.org/10.1109/TPEL.2019.2897061
23. Sun X, Wang B, Zhou Y, Wang W, Du H, Lu Z (2016) A single dc source cascaded seven-level inverter integrating switched-capacitor techniques. IEEE Trans Ind Electron 63(11):7184–7194. https://doi.org/10.1109/TIE.2016.2557317
24. Taghvaie A, Adabi J, Rezanejad M (2018) A self-balanced step-up multilevel inverter based on switched-capacitor structure. IEEE Trans Power Electron 33(1):199–209. https://doi.org/10.1109/TPEL.2017.2669377
25. Zeng J, Lin W, Cen D, Liu J (2020) Novel k-type multilevel inverter with reduced components and self-balance. IEEE J Emerg Sel Top Power Electron 8(4):4343–4354. https://doi.org/10.1109/JESTPE.2019.2939562