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ORIGINAL PAPER

On-board power quality charger for electric vehicles with minimized switching stresses

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Abstract

This paper intends to provide a three-level CUK converter-based on-board electrical vehicle battery charger with improved power quality features. The proposed configuration includes a diode bridge rectifier followed by a DC–DC converter suitable for the universal input voltage variations (85–265 V). It offers reduced voltage stress across the switches, reduced filter size, high efficiency, and improved dynamic response. A feed-forward control scheme is implemented for the proper functioning of the proposed converter under constant current (CC) and constant voltage (CV) modes of operation. In this paper, the mathematical modeling, operational details, and components design of the PFC converter are analyzed in continuous current mode. The simulation study on a 3.2 kW, 400 V proposed converter is carried out with MATLAB Simulink toolbox, and a real-time implementation of the same specifications of the proposed system is developed to verify the simulation study. The steady-state and dynamic behavior of the converter is investigated for power quality features like total harmonics distortion and input power factor with resistive and battery loads. The onboard charger exhibits satisfactory operation in CC and CV modes to a wide range of supply voltage variations.

Keywords Diode bridge rectifier (DBR) · Power factor correction (PFC) · Total harmonics distortion (THD) · Three-level (TL) DC–DC converter · Constant current (CC) · Constant voltage (CV)

1 Introduction

Keeping in view of global warming and usages of fossil fuel, there is growing interest of car manufacturers, consumers, and researchers towards the electric vehicles (EVs)/plug-in electric vehicles (PHEVs) [1, 2]. According to battery charger location, type of usages, and power level, the battery chargers are classified as on-board chargers (level-1, level-2) and off-board chargers (level-3) [3, 4]. A single-phase 120 V/230 V ac supply is limited to about 1.92 kW used to charge level-1 battery charger and works as slow charging for overnight charging. The level-2 charging refers to an onboard/off-board charger suitable with single-phase, 230 V, 50 Hz/three-phase, 415 V, 50 Hz ac supply, operates up to 19.2 kW. To improve the fast-charging time, typically 10–30 min approximately can be achieved with the off-board (level-3) charger. The onboard charger is placed inside the vehicle that uses a suitable outlet ac supply. However, the off-board charger is located outside the vehicle at a fixed location and to direct charge the EV battery. Therefore, an off-board charger is less constrained by size and weight [5, 6].

The AC/DC power converter is a key component of the onboard battery charger which is located inside the EVs/PHEVs [7]. Most battery chargers consist of an AC–DC converter followed by a non-isolated/isolated DC–DC converter to improve the power quality. The active PFC techniques can be divided into two categories: the single-stage and the two-stage approach [7–10]. In a single-stage, a diode bridge rectifier is widely used to produce unregulated DC output. Due to the nonlinear property of the rectifier, it supplies a non-sinusoidal and high value of peak distorted current which has 70–80% low THD and low input power factor (PF)

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of the order 0.7–0.8 lagging. According to IEC 61000-3-2, it is necessary to maintain input PF above 0.9 and THD in source current below 5% [11, 12]. To satisfy the guidelines of the IEC Standard, there are several PFC converters have been proposed in the literature for power quality improvement [12]. Therefore, the single-stage approach is suitable for low-power applications. The two-stage approach is preferred where the power rating requirement is relatively high but suffers from poor efficiency.

Generally, the PFC converters are designed to operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) [13]. In DCM mode, these converters are suffering from large voltage/current stress and high switching and conduction losses. Hence, DC–DC converters with DCM mode are advantageous for low-power applications. Based on the literature review, the boost and boost derived converters like flyback converter, etc., are found to be most appropriate for DCM PFC usage [14]. On the other hand, CCM associated with low switch stress is preferred for medium and high-power applications. Contrary, the PFC converters exhibit huge efficiency variations when fed from a wide range of input supply variations (85–265 V) [15]. At low input voltage, the boost converter suffers from poor efficiency as a consequence of high conduction losses in switch and reverse recovery losses in a diode. Thus, a large heat sink is required for losses dissipation, and security in the DC–DC converter leads to low power density [16–18].

These losses can be reduced by providing a high step-up gain and lower switch stress by employing DC–DC converters at low input voltage operation. There are several topologies which include transformer-based topologies, cascaded converters, quadratic converters, coupled inductor-based converters, and voltage multipliers. These converters include power factor correction to minimize harmonic currents drawn from the supply and provide regulated DC link voltage. Therefore, these topologies are widely used in battery charging applications [19]. Alike, a Cuk DC–DC converter which is derived from the buck and boost converters can generate the output voltage higher or lesser than supply voltage with reverse polarity. It consists of an intermediate capacitor that transfers energy from source to load. It has many advantages like a wide voltage conversion ratio, smooth source and load current, low conduction losses, and capacitor energy transfer [20, 21]. Despite aforesaid advantages, it suffers from high voltage stress and high filter size, and oversized components rating. To mitigate these disadvantages, three-level converters can be used which reduce filter size as well as voltage stress across the switch. The three-level converters are very much capable of smooth battery charging applications for electric vehicles [21]. Besides, a feed-forward control scheme is employed by eliminating distortion in source current, making input impedance resistive to ensure the proper functioning of the PFC converter [22–24].

The paper is structured in six sections. The technical issues and challenges related to PFC converters are discussed in Sect. 1. The schematic layout of system configuration and operation details of the three-level PFC CUK converter is demonstrated in Sect. 2. The design of circuit components and control algorithm of the proposed converter is presented in Sect. 3 and Sect. 4, respectively. Section 5 presents simulation and experimental results with resistive and battery loads. Power quality performances have also been discussed in Sect. 5. In the end, the conclusion is summarized in Sect. 6.

2 Operation analysis of PFC converter

The general layout of a single-phase PFC power converter for a battery charging system mainly consists of a single-phase ac supply (v_s), a diode bridge rectifier (DBR), a three-level Cuk DC–DC converter, and a battery pack of an electric vehicle as shown in Fig. 1.

2.1 Topology

A three-level Cuk converter-based power factor correction (PFC) circuit is proposed in Fig. 1a. It comprises a diode bridge rectifier (DBR) and a three-level CUK converter with different loads. The three-level Cuk converter consists of an input inductor (L_1), energy transferring capacitors (C_1, C_2), output inductor (L_2), output capacitor (C_o), and power diodes (D_1, D_2). It is designed to operate in continuous conduction mode (CCM) during one switching period, i.e., for a particular switching cycle, input inductor current (i_{L1}) never becomes zero.

Figure 1b illustrates the schematic diagram of the control scheme for the PFC converter which includes constant current (CC) and constant voltage (CV) modes of operation employed during battery charging application. The selection of charging modes either CC or CV depends on the value of state of charge (SOC) of the battery. The mode selector block inside the controller circuit changes the mode of operation from CC to CV. Initially, the battery is charged in CC mode in which the current controller maintains a constant current to charge the EV battery. As soon as the SOC of the battery reaches more than 85%, the operation of the converter is shifted to CV mode. During the CV mode of operation, the voltage controller maintains the constant output voltage of the converter to charge the battery.

2.2 Modes of operation

To carry out steady-state analysis of the proposed converter, the source voltage (v_s) is assumed to be constant (V_s) over

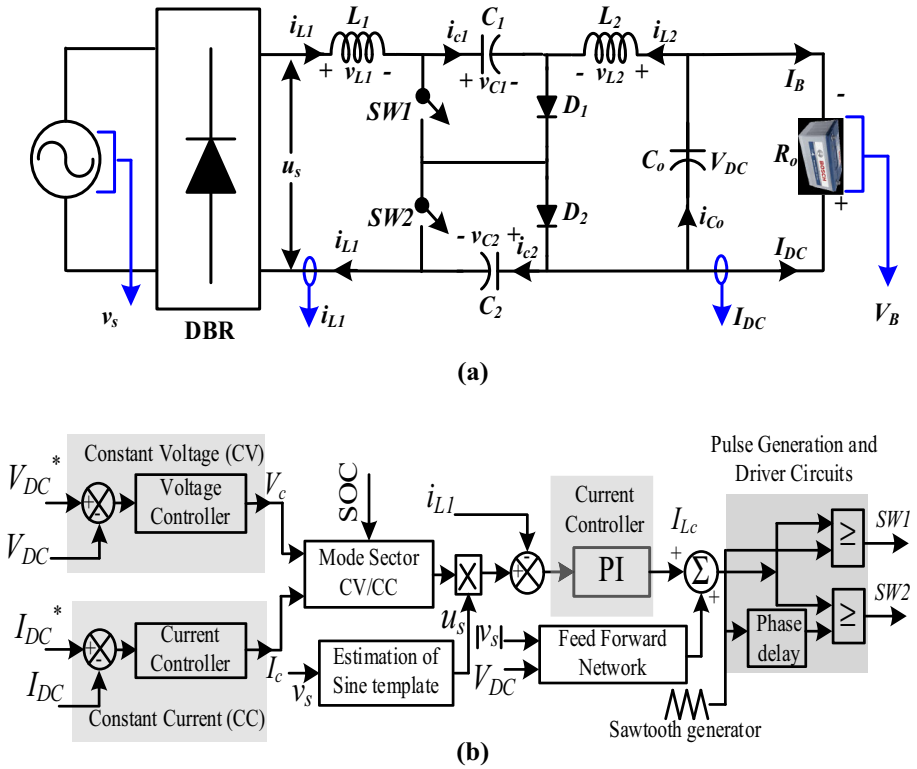


Fig. 1 Schematic diagram of TL Cuk converter with PFC operation

a particular sampling time (T_s). As supply voltage keeps on changing in each sampling time, the duty cycle (D) also keeps on varying in each sampling. For one switching period (T_s), each switch is turned on for DT_s and turns off for $(1-D)T_s$. The four operating modes are identified in each sampling period which repeats multiple times in one cycle of 50 Hz supply frequency as shown in Figs. 2 and 3. Depending upon the supply voltage (v_s), the duty ratio D of a switch may be classified as $D<0.5$ and $D>0.5$.

A. Case-1 when each switch is operated with $D<0.5$

In this case, waveforms of current and voltage of circuit parameters for one switching period are shown in Fig. 2a.

Mode-1 ($0<t\leq DT_s$): In this mode, switch SW1, diode D_2 turns on and switch SW2, diode D_1 turned off as shown in Fig. 3a. The input inductor L_1 charges through path v_s-L_1-SW1-D_2 and output inductor L_2 charges with SW1-D_2-C_O-L_2-C_1 as well as intermediated capacitors C_1, C_2 discharges. Thus, inductor currents i_{L_1} and i_{L_2} are increased and achieved their respective final values at time DT_s. The corresponding equations are following as:

$$V_{C_1}=V_{C_2}=\frac{V_s+V_{DC}}{2} \tag{1}$$

Here, the average voltage across intermediate capacitor $C_1$and C_2 is shown in Eq. (1).

$$v_{L1}=v_{L2}=\frac{V_s-V_{DC}}{2}$$
$$i_{D2}=i_{L1}+i_{L2};V_{SW2}=\frac{v_s(t)+V_{DC}}{2};V_{D1}=-\frac{v_s(t)+V_{DC}}{2} \tag{2}$$

Mode-2 ($DT_s<t\leq T_s/2$): In this mode, switches SW1, SW2 kept off and diodes (D_1, D_2) conduct as illustrated in Fig. 3d. The input inductor L_1 discharges through the path C_1-D_1-D_2-C_2-V_S-L_1 and L_2 discharges through output capacitor C_o. The current through both the inductors fall from their final values to initial values as shown in Fig. 2a. The corresponding equations are given as:

$$v_{L1}=v_{L2}=-V_{DC}$$
$$i_{D1}=i_{D2}=i_{L1}+i_{L2};V_{SW1}=V_{SW2}=\frac{V_s+V_{DC}}{2} \tag{3}$$

Mode-3($T_s/2<t\leq DT_s+T_s/2$): In this mode, diode D_2 turned off, but D_1 remains on with SW2 on and SW1 off as depicted in Fig. 3b. The currents through inductors raise from their initial values to final values same as mode-1. The corresponding equations are given as:

$$v_{L1}=v_{L2}=\frac{V_s-V_{DC}}{2}$$
$$i_{D1}=i_{L1}+i_{L2};\ V_{SW1}=\frac{V_s+V_{DC}}{2};\ V_{D2}=-\frac{V_s+V_{DC}}{2} \tag{4}$$

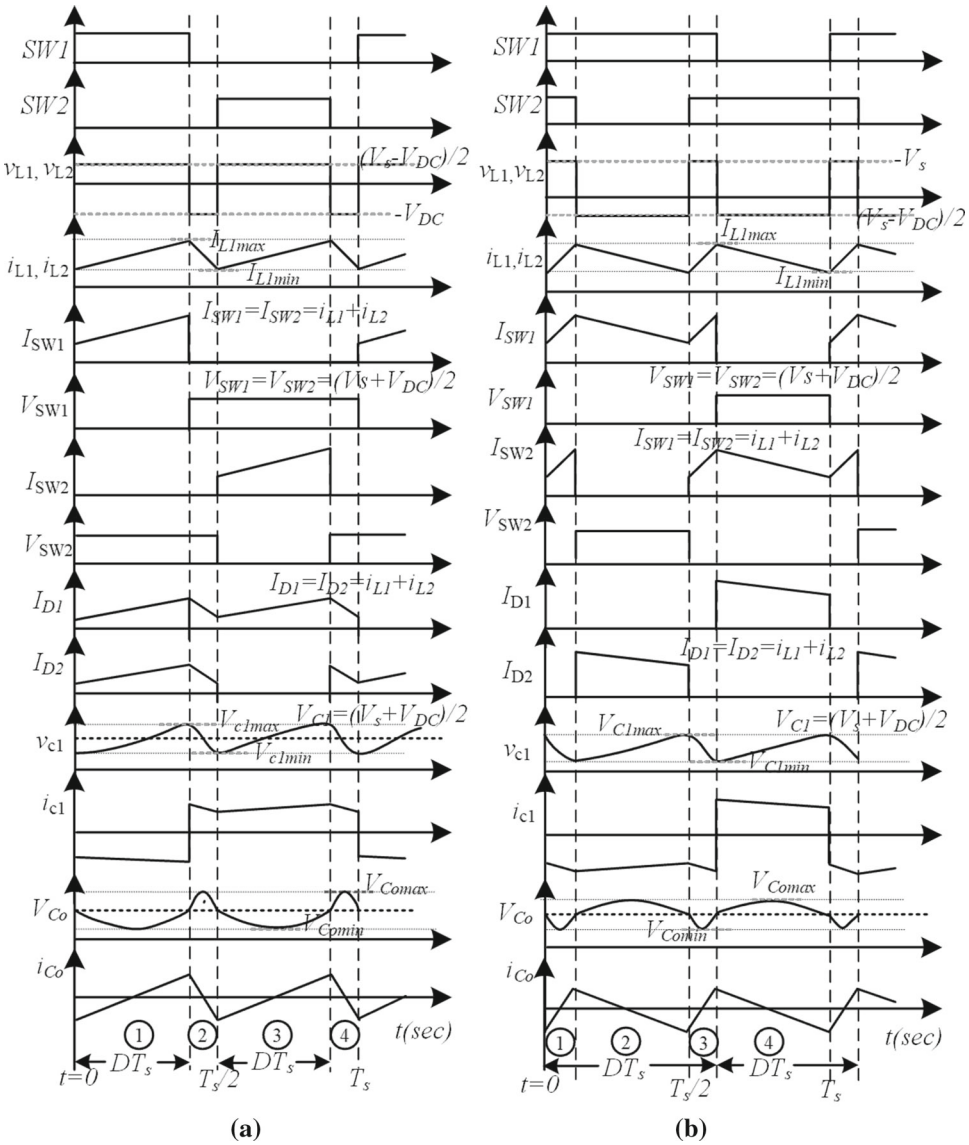


Fig. 2 Switching waveforms of voltage and current over one switching cycle with duty ratio **a** $D<0.5$ and **b** $D>0.5$

Mode-4 ($DT_s + T_s/2 < t \leq T_s$): The operation in mode-4 is the same as mode-2 switch SW1 turned off and switch SW2 kept off and diodes (D_1, D_2) both are conducting depicted in Fig. 3d.

B. Case-2 when each switch is operated with $D > 0.5$

The voltage and current waveforms of various parameters over one switching cycle are depicted in Fig. 2b. Based on the state of switches, four modes of operations over one switching are identified. In the case of a duty ratio greater than 0.5, the output voltage should be greater than the input voltage.

Mode-1 ($0< t \leq (DT_s - T_s/2)$): Initially switches SW1, SW2 turned on and diode D_1, D_2 kept off as illustrated in Fig. 3c. Input inductor L_1 is charging with input voltage v_s and output inductor L_2 is charging through C_1-SW1-SW2-C_2-C_O-L_2. Hence inductor currents i_{L1} and i_{L2} are increased and achieved their respective final values at time ($DT_s - T_s/2$). The corresponding equations are given as:

$$v_{L1} = v_{L2} = V_s$$
$$i_{SW1} = i_{SW2} = i_{L1} + i_{L2};\ V_{D1} = V_{D2} = -\frac{V_s + V_{DC}}{2} \quad (5)$$

Mode-2 ($(DT_s - T_s/2) < t \leq T_s/2$): In this mode, SW2 turned off, but SW1 remains on with D_1 off and D_2 on as depicted in Fig. 3a. The voltage across both the inductors becomes negative; hence, the currents through inductors fall from their final values to initial values because the voltage across inductors is negative. The corresponding equations are given as:

$$v_{L1} = v_{L2} = \frac{V_s - V_{DC}}{2}$$

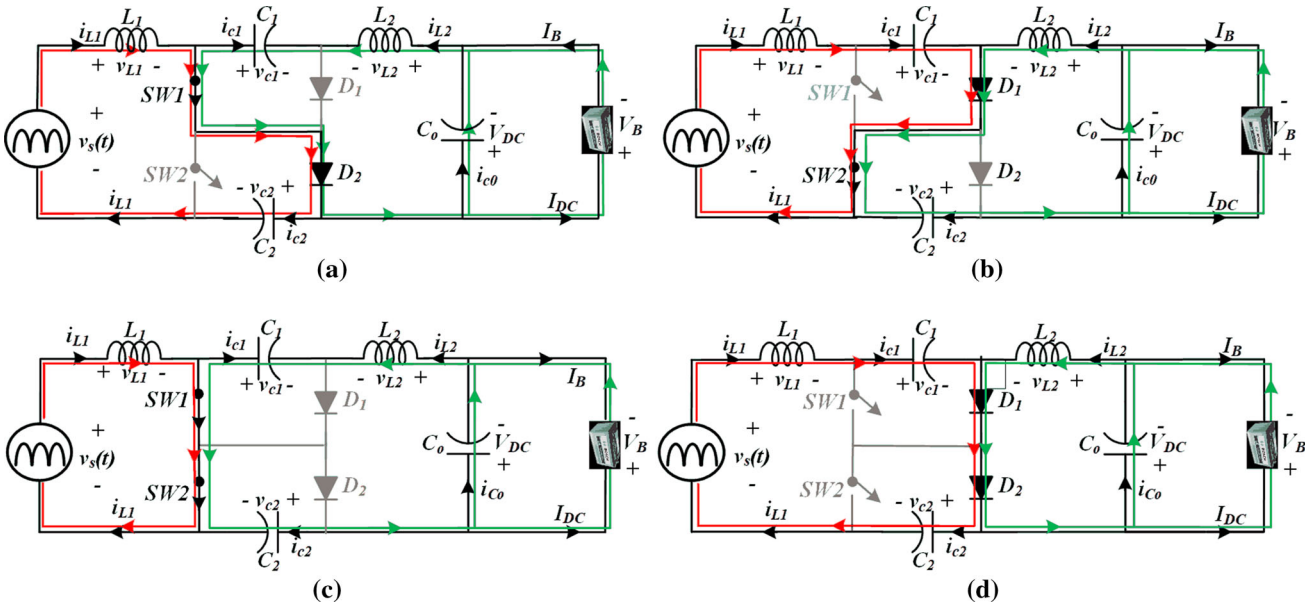


Fig. 3 Equivalent circuit depicting current paths under different operating modes over one switching cycle **a** SW1 on, **b** SW2 on, **c** Both switches SW1, SW2 are on and **d** switches SW1 and SW2 are off

$$i_{\mathrm{SW1}} = i_{D2} = i_{L1} + i_{L2}; V_{\mathrm{SW2}} = V_{D1} = \frac{V_{\mathrm{s}} + V_{\mathrm{DC}}}{2} \tag{6}$$

Mode-3 ($T_{\mathrm{s}}/2 < t \leq (T_{\mathrm{s}} - \mathrm{DT_s})$): The operation in mode-3 is same as mode-1. In case-2, for $D < 0.5$ because both switches SW1 and SW2 are conducting and diode are reversed bias depicted in Fig. 3c.

Mode-4 ($(T_{\mathrm{s}} - \mathrm{DT_s}) < t \leq T_{\mathrm{s}}$): At the time instant $t = \mathrm{DT_s}$, SW2 remains on, SW1 turns off and D_1 turns on and D_2 turns off as illustrated in Fig. 3b. The current through both the inductors (i_{L1}, i_{L2}) again decrease from their final values and related equations are given below:

$$v_{L1} = v_{L2} = \frac{V_{\mathrm{s}} - V_{\mathrm{DC}}}{2}$$
$$i_{\mathrm{SW2}} = i_{D1} = i_{L1} + i_{L2}; V_{\mathrm{SW1}} = V_{D2} = \frac{V_{\mathrm{s}} + V_{\mathrm{DC}}}{2} \tag{7}$$

3 Design of passive components of PFC converter

Based on the power ratings of the three-level converter, proper selection of passive components like inductors (L_1, L_2) and capacitors (C_1, C_2, C_{o}) is to be carried out for providing the well-maintained DC output with improved power quality features at the input side. A single-phase 240 V, 50 Hz is supplied to a DBR feeding the TL converter which is given by the equation $v_{\mathrm{s}}(t) = V_{\mathrm{m}}\mathrm{Sin}(2\pi f_{\mathrm{L}})t = 240\sqrt{2}\mathrm{Sin}(314t)$; where $V_{\mathrm{m}}, f_{\mathrm{L}}$ is the peak voltage and line frequency of supply system, respectively. The output of DBR, which is connected as the input voltage to a three-level converter, is given in Eq. (8);

$$v_{\mathrm{s}}(t) = |V_{\mathrm{m}} \sin(2\pi f_L)t| = \left|240\sqrt{2}\sin(314)t\right| \tag{8}$$

For the satisfactory operation of an inductor, the average voltage over one switching cycle should be zero. Thus, the average voltage across inductor L_1 is given as:

$$V_{L1} = \left(\frac{V_{\mathrm{s}} - V_{\mathrm{DC}}}{2}\right) \cdot \mathrm{DT_S} - V_{\mathrm{DC}}\left(\frac{T_{\mathrm{S}}}{2} - \mathrm{DT_S}\right) = 0 \tag{9}$$

After solving Eq. (9), the steady-state output voltage and the value of duty ratio D, in the terms of supply voltage and output DC voltage is given in Eq. (10):

$$V_{\mathrm{DC}} = \frac{D}{(1-D)} V_{\mathrm{s}}$$
$$D = \frac{V_{\mathrm{DC}}}{V_{\mathrm{DC}} + V_{\mathrm{s}}} \tag{10}$$

Thus, the duty ratio D is measured as 0.65 for three-level Cuk converter PFC operation.

3.1 Design of inductors (L_1, L_2)

The value of inductors (L_1, L_2) can be selected by evaluating the average inductor current. With consideration of lossless converter and CCM mode of operation, the boundary values of the inductor current are identified by using Eqs. (4) and

(10). After that designed equations for inductors for different range of duty ratio are given in Eq. (11):

$$L_1 = \frac{(1-2D)V_o}{2 \cdot \Delta i_{L1} \cdot f_s},\ L_2 = \frac{(1-2D)V_o}{2 \cdot \Delta i_{L2} \cdot f_s}; D < 0.5$$
$$L_1 = \frac{(2D-1)(1-D)V_o}{2 \cdot D \cdot \Delta i_{L1} \cdot f_s},\ L_2 = \frac{(2D-1)(1-D)V_o}{2 \cdot D \cdot \Delta i_{L2} \cdot f_s}; D > 0.5 \quad (11)$$

where ripple in input inductor current $\Delta I_{L1} = 30\%$ ripple of input current I_s, ripple in output inductor current $\Delta I_{L2} = 30\%$ ripple of input current I_o.

As the PFC converter is operated in continuous current mode, $I_{L1\min}$ should be positive. The minimum value of L_1 can be determined by keeping the minimum inductor current to zero.

$$L_{1\text{crit}} = L_{2\text{crit}} = \frac{(1-2D)(1-D)R_o}{4 \cdot D \cdot f_s}; \quad D < 0.5$$
$$L_{1\text{crit}} = L_{2\text{crit}} = \frac{(2D-1)(1-D)^2 R_o}{4 \cdot D^2 \cdot f_s}; \quad D > 0.5 \quad (12)$$

Here, $L_{1\text{crit}}$ is the minimum value of inductance, the value above which the PFC converter operated in CCM mode.

The voltage and current equations for the intermediate inductor (L_2) are the same as the input inductor (L_1) with the same boundary values. Hence design values of L_2 will be the same as L_1 in both Eqs. (11) and (12). The critical inductance (L_1, L_2) is calculated from Eq. (11) for $D > 0.5$ is 3 mH. And the selected values of L_1, L_2 in the CCM mode of operation are specified is given in "Appendix".

3.2 Design of intermediate capacitors (C_1, C_2)

Figure 3a indicates that both intermediate capacitor currents (i_{C1}, i_{C2}) are the same as current flow in an intermediate inductor (i_{L2}) for that mode hence values of C_1 and C_2 will be the same. The capacitor current i_{C1} can be represented during switching as shown in Fig. 2b. The value of capacitor C_1 can be calculated by

$$C_1 = \frac{1}{\Delta V_{C1}}\left[\int_0^{T_{ON}} i_{C1} \mathrm{d}t\right] \quad (13)$$

where ΔV_{C1} = ripple voltage across C_1, from Eqs. (1) and (13). Thus, the values of capacitors are given by Eq. (14);

$$C_1 = C_2 = \frac{(1-D) \cdot T_s}{\frac{\Delta V_{C1}}{V_o} \cdot R_o} r; \quad D < 0.5$$
$$C_1 = C_2 = \frac{(2D-1)(1-D) \cdot T_s}{2D\frac{\Delta V_{C1}}{V_o} \cdot R_o}; \quad D > 0.5 \quad (14)$$

For the duty ration, $D > 0.5$, the calculated intermediate capacitances (C_1, C_2) are 1.8 μF and the selected value for intermediate capacitors is specified in "Appendix".

3.3 Design of output capacitor (C_o)

The value of output capacitor depends upon ripple in output voltage (ΔV_{Co}). For the low value of ripple content, the designed value of capacitor is higher. The output voltage ripple (ΔV_{Co}) can be calculated by Eq. (16) and output current (i_{Co}) is given in Eq. (15).

$$i_{Co} = i_{L2} - I_o$$
$$C_o = \frac{1}{\Delta V_{Co1}}\left[\int_0^{T_{ON}} -I_o \mathrm{d}t\right] \quad (15)$$

After solving Eq. (15), the value of output capacitor is given by:

$$C_o = \frac{D \cdot T_s}{\frac{\Delta V_{Co}}{V_o} \cdot R_o}; \quad D < 0.5$$
$$C_o = \frac{(2D-1) \cdot T_s}{2 \cdot \frac{\Delta V_{Co}}{V_o} \cdot R_o}; \quad D > 0.5 \quad (16)$$

The calculated and selected value for output capacitance (C_o) is 1000 μF. The selected design components values are specified in "Appendix".

4 Control algorithm

To achieve the desired objective of ripple-free output voltage/current along with improved input power factor, the average current control technique is employed. It consists of two control loops namely inner input current control to maintain the unity power factor operation and outer control loop for maintaining the constant output voltage/current. The inner current control loop is faster and it tries to reduce error between average input current [23]. Besides, there is one feed-forward network that tries to reduce zero crossing error in supply current.

For outer control loop operation, initially, the battery will operate under CC mode and the mode selector block selects constant current (CC) mode of operation. In CC mode of operation, Battery will operate at 30% SOC and compare reference current $I^*_{DC}(k)$ with output current $I_{DC}(k)$ which generate a current error $I_e(k)$, where $I_e(k)$ at any instant 'k' is given as

$$I_e(k) = I^*_{DC}(k) - I_{DC}(k) \quad (17)$$

This current error is the input of the current PI controller, and it generates a controlling signal $I_c(k)$, which is shown in Eq. (18) are:

$$I_c(k) = I_c(k-1) + k_{ii} I_e(k) + k_{pi}\{I_e(k) - I_e(k-1)\} \quad (18)$$

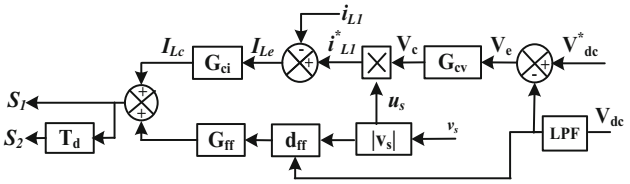


Fig. 4 Control algorithm for PFC converter

where k_{pi}, k_{ii} are the proportional and integral gain of the outer current PI controller.

In the case of an outer voltage control loop, when battery voltage reaches 85% of SOC value then mode selector block selects constant voltage (CV) mode of operation. In this control algorithm (Refer Fig. 4), the output voltage controller will be activated and compared a reference voltage $V^*_{DC}(k)$ with the output DC voltage $V_{DC}(k)$. Then, it generates a voltage error $V_e(k)$, where $V_e(k)$ at any instant 'k' is given as

$$V_e(k) = V^*_{DC}(k) - V_{DC}(k) \tag{19}$$

The voltage error $V_e(k)$ is the input of a voltage PI controller and it generates a controlling voltage signal $V_c(k)$, which is represented by

$$V_c(k) = V_c(k-1) + k_{iv}V_e(k) + k_{pv}\{V_e(k) - V_e(k-1)\} \tag{20}$$

where k_{pv}, k_{iv} are the proportional and integral gain of the outer voltage PI controller. The current reference $i^*_{L1}(k)$ is produced by multiplying $V_c(k)$ with the unit template of supply voltage as follows:

$$u_s(k) = \left|\frac{v_s(k)}{V_m}\right|; \quad i^*_{L1}(k) = u_s(k)\cdot V_c(k) = u_s(k)\cdot I_c(k) \tag{21}$$

The comparison is done between the current reference signal $i^*_{L1}(k)$ and input inductor current $i_{L1}(k)$ which produces a current error $I_{Le}(k)$, where $I_{Le}(k)$ at any instant 'k' is given as

$$I_{Le}(k) = I^*_{L1}(k) - I_{L1}(k) \tag{22}$$

This $I_{Le}(k)$ is fed to another proportional-integral (PI) controller and output of PI is generated controlled output as $I_{Lc}(k)$ which is given by Eq. (23);

$$I_{Lc}(k) = I_{Lc}(k-1) + k_{p1}\{I_{Lc}(k) - I_{Lc}(k-1)\} + k_{i1}I_{Lc}(k) \tag{23}$$

where k_{p1}, k_{i1} are proportional and integral gains of the inner current PI controller. The output of inner current PI controller $I_{Lc}(k)$ is added up with the output of feed forward network and compares with a high-frequency ramp signal of switching frequency 10 kHz. The output of this comparator is used as switching pulses for switch SW1 and for generating the switching pulses for switch SW2, same high frequency ramp signal is delayed by 180° using a transport delay. This feed-forward network is nothing but a varying duty ratio of the proposed converter. Here, G_{cv} = gain of voltage controller; G_{ci} = gain of current controller; G_{ff} = gain of feed-forward network; T_d = transport delay.

5 Results and discussions

A 3.2 kW, 400 V/8 A three-level CUK converter-based on-board charger is developed in MATLAB software for simulation study with "ode4" solver and same is done for real-time implementation with 20 μs sampling time. The developed charging system performances are shown as per converter design parameters shown in "Appendix". The steady state and dynamic performance is investigated with respect to power quality features like supply current THD, supply voltage THD and input PF with resistive and battery loads. The charging performance of the battery is examined in constant current (CC) and constant voltage (CV) modes on the basis of state of charge (%SOC). The waveform results of source voltage (v_s), source current (i_s), output voltage (V_{DC}), output current (I_{DC}), inductor currents (i_{L1}, i_{L2}), intermediate capacitor voltage (v_{C1}), voltage across switch and diode (V_{SW1}, V_{D2}), switch current (I_{SW1}), battery voltage (V_B) and battery current (I_B) are examined for resistive and battery loads shown in Fig. 5. Figure 6 shows simulation results of power quality indices like power factor and THD in supply current.

5.1 Simulation results

A developed Simulink model analysis of proposed PFC system is done for steady and dynamic state by feeding 400 V/8 A resistive load and battery load with nominal voltage of 345 V/40 AH at 230 V, 50 Hz supply voltage.

A. Steady-state analysis feeding resistive load

Figure 5a shows steady-state analysis of the PFC converter for resistive load at supply voltage of 230 V, 50 Hz for time t = 0.9 to 1.2 s. It is observed that source current waveform is purely sinusoidal and also in phase with source voltage which indicates that proposed converter is operating at unity PF. The current through input and output inductor follows output current of DBR which is displayed in continuous conduction mode. Figure 5a shows intermediate capacitor voltages (v_{C1}) is equal to summation of half of sinusoidal input voltage and constant output DC voltage. The min value of voltage of

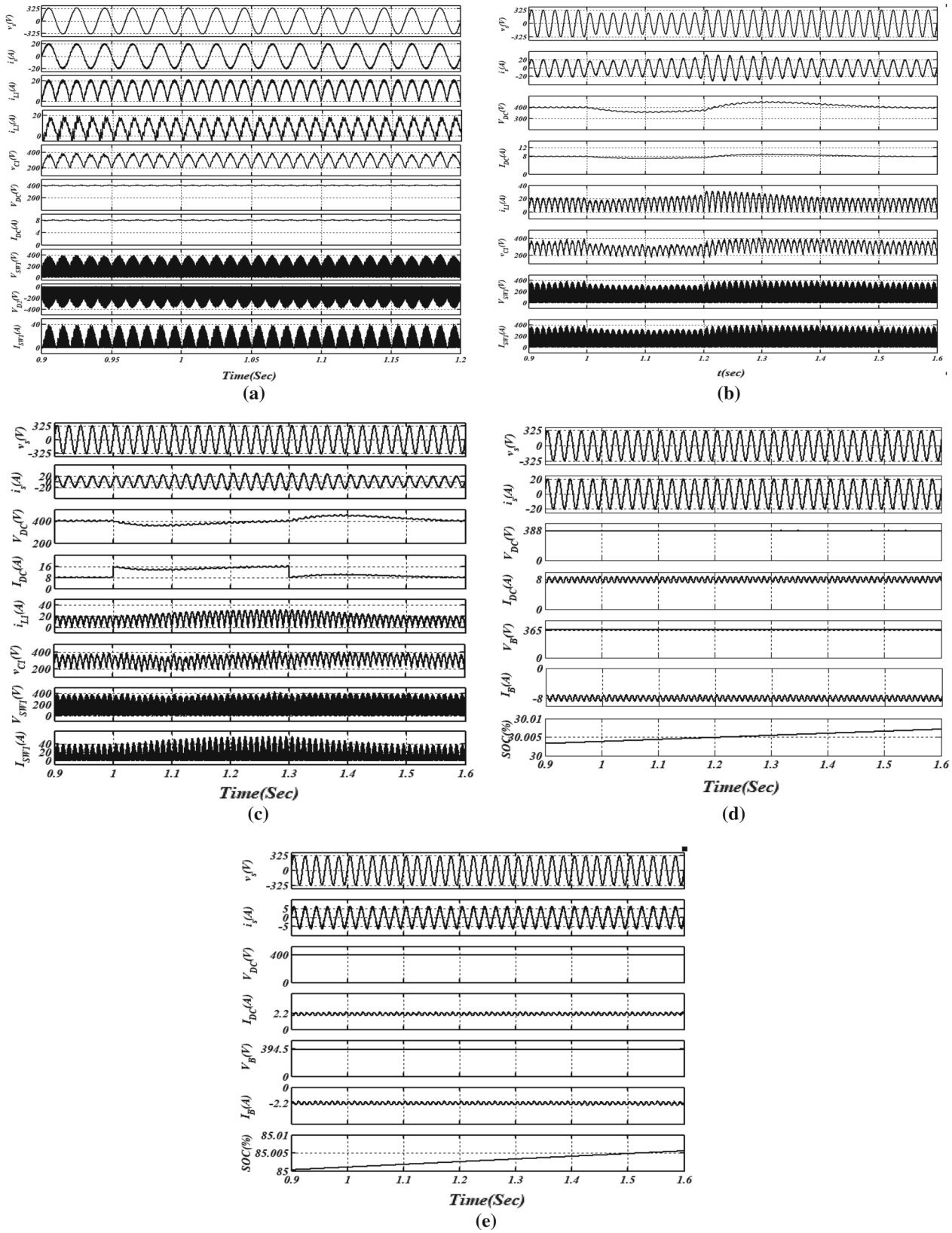


Fig. 5 Simulation results of PFC converter **a** steady-state analysis with resistive load, **b** source voltage variation, **c** load variation, **d** battery load in CV mode and e battery load in CC mode

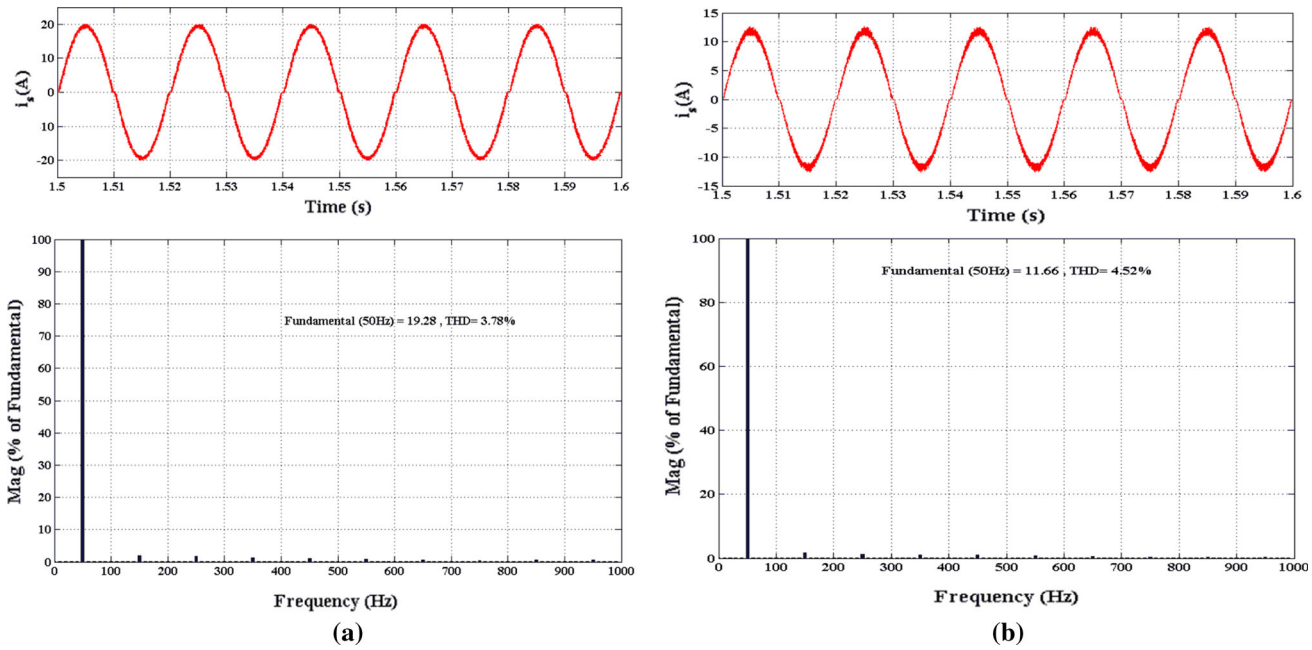


Fig. 6 Converter THD performance of input current at 3.2 kW battery load at $v_s = 230$ V **a** CC mode and **b** CV mode

intermediate capacitor is 200 V and max value is 362 V at 230 V supply voltage. The shown output voltage and current maintained constant DC value 400 V and 8 A, respectively, in Fig. 5a. When switch and diode is in off state, thus appeared voltage across switch and diode is 362 V, i.e., equal to half of varying input voltage and constant DC output voltage is also presented by Fig. 5a. When switch is in on state, the appeared current across switch is sum of input and output current shown by simulation result of Fig. 5a.

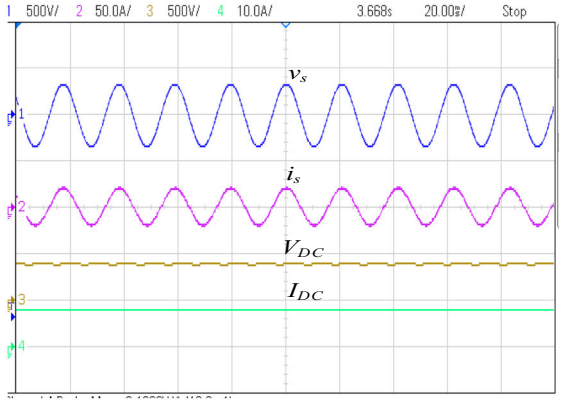
B. Dynamic analysis feeding resistive load

Figure 5b, c shows dynamic performance results at source voltage variation and load voltage variation, respectively, for time $t = 0.9$ to 1.6 s. The 20% step decrease in source voltage is done at $t = 1$ s then again set at $t = 1.2$ s with 230 V nominal supply voltage shown in Fig. 5b. The variation in source voltage from 230 to 184 V shows the variation in input current. However, the output voltage V_{DC} is unaltered after 300 ms small period of disturbance at unity PF shown in Fig. 5b. Figure 5c shows performance of the TL converter with load variation. The load is increased from 8 to 16 A at $t = 1$ s and then it again settled to 8 A at $t = 1.3$ s at same input voltage. In results, output voltage is maintained at its desired value (400 V) at unity PF with small disturbance of 200 ms. Both source and load variations show constant output voltage V_{DC} 400 V and maintained power factor unity which satisfied the PFC operation of proposed converter.

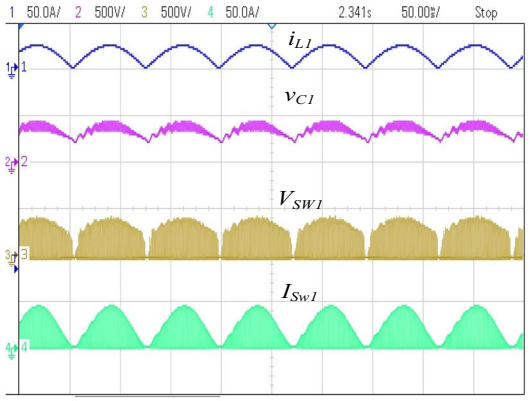
C. Steady-state analysis feeding the battery load

A battery charging is done by proposed PFC converter either in constant voltage (CV) mode or in constant current (CC) mode. Figure 5d, e presents steady-state analysis of PFC converter with battery load in CC and CV mode, respectively, at input voltage of 230 V, 50 Hz. Depending upon the SOC of battery, the operation of converter is shifted from CC to CV mode. Initially, converter operates in CC mode to charge battery with SOC of 30%. In CC mode, therefore, the battery is charging with constant output current of 8 A. Figure 5d presents the max value of source current (i_s) is 19.8 A, output voltage (V_{DC}) 388 V which is less than constant output voltage 400 V, and constant output current (I_{DC}) 8 A which is equal to constant charging current 8 A. Figure 5d also shows the voltage across the battery is less, i.e., 365 V and battery current is equal to 8 A of constant current shows the CC mode of charging operation.

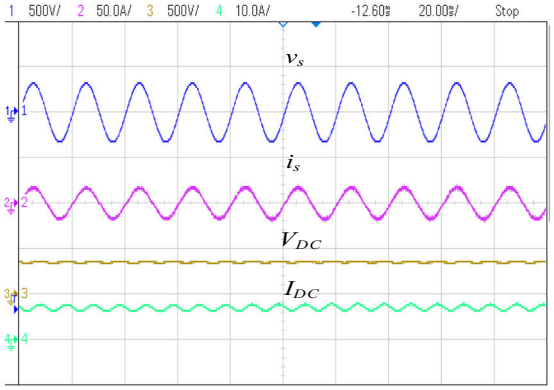
When SOC of battery reaches to 85%, converter operates in CV mode. Now, it shows the converter is charging with constant output voltage of 400 V. Figure 5e presents the max value of source current is 5.2 A, output voltage (V_{DC}) 400 V which is equal to constant charging voltage 400 V, the output current of 2.2 A which is less than constant output current of 8 A. Therefore, the voltage and current across the battery are 395.4 V and 2.2 A. It is identified that in CV mode, battery is charged with constant voltage of 400 V and in CC mode, the battery is charged with constant current 8 A, and the converter is maintained input power factor (PF) unity in both the operating modes. Figure 6 depicts the converter harmonic spectrum and THD of the source current (i_s) of battery charging in CC and CV mode at 230 V supply voltage. The shown input current THDs are 3.78% and 4.2% in CC and CV mode, respectively.



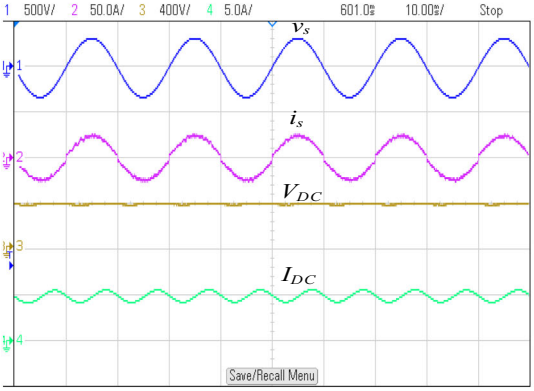
(a) In y-axis Ch1: 500V/div, Ch2: 50A/div, Ch3: 500V/div, Ch4: 10A/div, and in x-axis 20ms/div



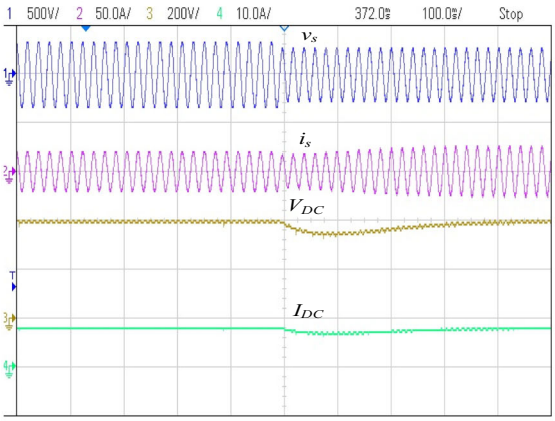
(b) In y-axis Ch1: 50A/div, Ch2: 500V/div, Ch3: 500V/div, Ch4: 50A/div, and in x-axis 50ms/div



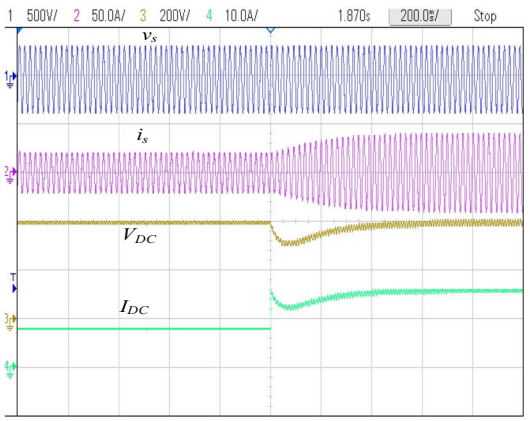
(c) In y-axis Ch1: 500V/div, Ch2: 50A/div, Ch3: 500V/div, Ch4: 10A/div, and in x-axis 20ms/div



(d) In y-axis Ch1: 500V/div, Ch2: 50A/div, Ch3: 400V/div, Ch4: 5A/div, and in x-axis 10ms/div

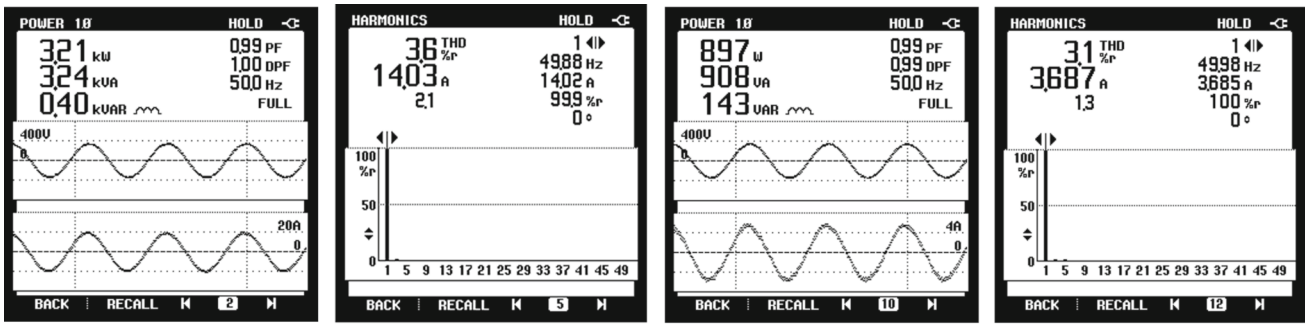


(e) In y-axis Ch1: 500V/div, Ch2: 50A/div, Ch3: 200V/div, Ch4: 10A/div, and in x-axis 100ms/div



(f) In y-axis Ch1: 500V/div, Ch2: 50A/div, Ch3: 200V/div, Ch4: 10A/div, and in x-axis 200ms/div

Fig. 7 Steady-state performance of converter **a**, **b** with resistive load, with battery load **c** in CC mode **d** in CV mode at source voltage ($v_s = 230$ V) and dynamic performance with resistive load under **e** supply voltage variation from 230 to 184 V and **f** load variation from 8 to 16 A



(a) (b) (c) (d)

Fig. 8 Performance of the converter under 230 V in **a**, **b** CC mode **c**, **d** CV mode (i) P_s, Q_s and PF (ii) THD in i_s

Table 1 Power quality features of converter with different source voltages

Source voltage (V)		Battery charging mode					
		CV mode			CC mode		
		v_{sTHD} (%)	i_{sTHD} (%)	PF	v_{sTHD} (%)	i_{sTHD} (%)	PF
85	Simu	0.0	4.9	0.98	0.0	4.57	0.98
	Exp	0.7	4.7	0.99	0.8	4.8	0.99
120	Simu	0.0	3.3	0.98	0.0	3.4	0.98
	Exp	0.6	3.5	0.99	0.6	3.5	0.99
150	Simu	0.0	2.4	0.99	0.0	2.3	0.99
	Exp	0.5	4.0	0.99	0.6	3.4	0.99
200	Simu	0.0	2.9	0.99	0.0	2.8	0.99
	Exp	0.5	3.8	0.99	0.5	4.3	0.99
230	Simu	0.0	4.52	0.99	0.0	3.78	0.99
	Exp	0.5	3.1	0.98	0.4	3.6	0.99
265	Simu	0.0	2.8	0.99	0.0	3.3	0.99
	Exp	0.5	4.2	0.98	0.4	3.4	0.99

5.2 Test results

The proposed charging system results are verified experimentally in real time using Spartan3 FPGA board (XC3S5000) with sampling time of 20 μs. The same design parameters shown in "Appendix" are also used for test results. A Fluke Power Analyser and a Digital oscilloscope (DSO) are used in recording of test results.

Figure 7 shows test performance of the proposed converter with resistive load, and battery load at supply voltage of 230 V in CC and CV mode, respectively. Figure 7a shows waveforms of input voltage and current are in same phase, and constant DC output voltage and current of 400 V and 8 A, respectively. Figure 7b displays results of input inductor current, intermediate capacitor voltage, switch voltage and current stress which is same as simulation results. It is observed that constant DC output current of 8 A is maintained during CC mode of battery charging depicts in Fig. 7c. Further, when SOC of battery reaches to 85%, the operation of converter is shifted to CV mode in which output voltage of 400 V is maintained constant as seen in Fig. 7d. Figure 7d, e shows unity power factor (PF) in both the charging operating modes.

To assess the dynamic performance of converter, the supply voltage variation from 230 to 184 V (20% variation) at 50 Hz is carried out with resistive load. It is observed in Fig. 7e that shows DC output voltage remained constant at 400 V after small disturbance of 300 ms with load current of 8 A. Figure 7f shows performance of converter under load variation from 8 to 16 A, at nominal supply voltage of 230 V, 50 Hz. The same constant DC voltage is maintained constant after 300 ms disturbance. In Fig. 7e, f, the dynamic state performance the charging system maintain both constant output voltage and power factor unity.

Figure 8 shows waveforms of THD of supply current, real power (P_s), reactive power (Q_s), input *PF* and distortion factor in both CC and CV modes at supply voltage 230 V, 50 Hz. it is observed that THD in source current is of 3.6% and reactive power required is 0.40 KVAR in CC mode, and THD in source current is 3.1%, reactive power required 143 kVAR

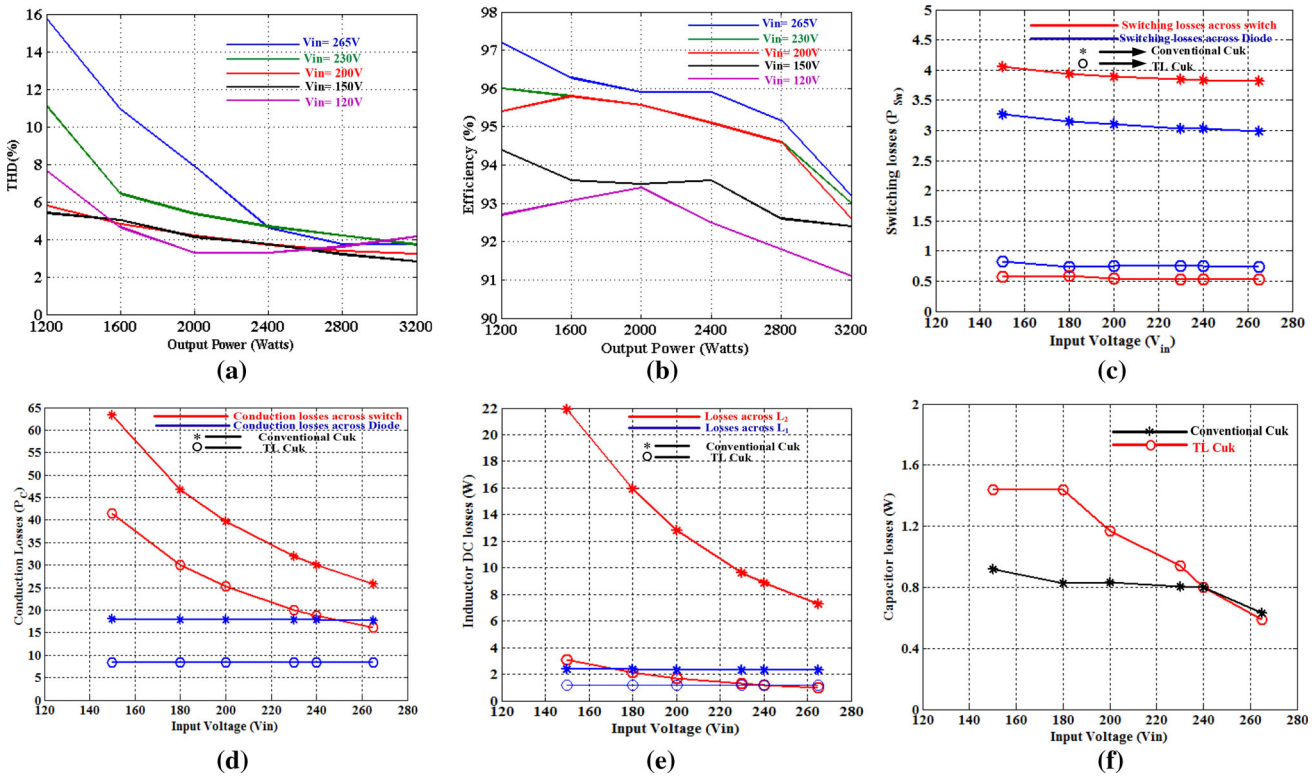


Fig. 9 TL CUK converter performance **a** THD v/s output power, **b** efficiency v/s output power graph, **c** switching losses, **d** conduction losses, **e** inductor DC losses (L_1, L_2) and **f** intermediate capacitor losses

in CV mode. Table 1 depicts comparison of experimental and simulation results of converter related to power quality features at universal input voltages (85–265 V).

A comparison study of proposed TL CUK converter is executed with conventional CUK converter under wide voltage variations shown in Fig. 9. It is perceived that THD and Efficiency variation with output power at different load conditions shown in Fig. 9a, b. At 230 V of supply voltage, the system efficiency achieved in CC and CV mode is 97.1% and 94.5%, respectively, and input current THDs in both operating modes are less than 5%. Figure 9c–f shows proposed converter losses are reduced as compared to conventional converter under voltage variations. In spite of the additional losses being incurred in the proposed converter, the total loss is found to be less under different input voltage conditions. Table 2 shows the comparison of TL CUK and conventional CUK PFC converter parameters. As compared to conventional Cuk PFC converter, proposed converter shows the reduction in reduced voltage stress across switches and diodes, switching and conduction losses across switch, and switching and conduction losses across diode.

6 Conclusion

The PFC-based three-level (TL) CUK converter is proposed and examined for resistive load of 3.2 kW/400 V and onboard EV battery charging application in both CC and CV operating modes. The proposed converter offers PFC characteristics in CCM mode by using feed-forward control techniques. The feed-forward technique advantages are to provide zero crossing error in sine template and made the supply current in phase with supply voltage. The designed converter validates power factor unity, efficiency 97.1% and current THD less than 5% meets the required criteria as prescribed by IEEE Standard 519-1992 and IEC61000-3-2. The added benefits of the proposed TL CUK converter topology are reducing voltage stress to half, reduce filter size, lesser losses across switch and diode as compared to conventional CUK converter. Thus, it reduces the switch rating, improves the overall efficiency 2–3%, and also improves dynamic response. The simulation results of a proposed converter with wide supply voltage variations are also examined with resistive and battery load. The proposed charger has shown satisfactory characteristics during steady-state, under load, and supply voltage variations. These results are also validated experimentally in a real-time approach. Therefore, the PFC converter is well suited for high input/output voltage applications such as onboard charging for electric vehicles.

Table 2 Parameters comparison of PFC-based CUK converters

S. no.	Parameters	TL (three level) CUK PFC converter	Conventional CUK PFC converter
1	Duty ratio (D)	$\frac{V_{dc}}{V_{in}} = \frac{D}{1-D}$; $D = 0.55$ Duty ratio is same in both cases	$\frac{V_{dc}}{V_{in}} = \frac{D}{1-D}$; $D = 0.55$
2	Input (L_1) and intermediate inductor (L_2)	$L_1 = \frac{(1-2D)V_o}{2 \cdot \Delta i_{L_1} \cdot f_s}$, $L_2 = \frac{(1-2D)V_o}{2 \cdot \Delta i_{L_2} \cdot f_s}$; $D < 0.5$ $L_1 = 0.8$ mH, $L_2 = 1.36$ mH; $D > 0.5$, $L_1 = \frac{(2D-1)(1-D)V_o}{2 \cdot D \cdot \Delta i_{L_1} \cdot f_s}$, $L_2 = \frac{(2D-1)(1-D)V_o}{2 \cdot D \cdot \Delta i_{L_2} \cdot f_s}$; $D > 0.5$ As compared to conventional Cuk, size of filter inductance is reduced. Ripple in inductor current is also reduced	$L_1 = \frac{V_s D}{f \Delta i_{L_1}}$; $L_2 = \frac{V_s D}{f \Delta i_{L_2}}$ $L_1 = 8.9$ mH $L_2 = 14.9$ mH
3	Intermediate capacitor (C_1, C_2)	$C_1 = C_2 = \frac{(1-D).T_s}{\frac{\Delta V_{C1}}{V_o}.R_o} r$; $D < 0.5$ $C_1 = C_2 = \frac{(2D-1)(1-D).T_s}{2D\frac{\Delta V_{C1}}{V_o}.R_o}$; $D > 0.5$ $C_1 = C_2 = 1.8$ μF, As compared to conventional Cuk, size of intermediate capacitance filter is reduced	$C_1 = \frac{DT_s}{\frac{\Delta V_{C1}}{V_o}.R_o}$; $C_1 = 24.26$ μF
5	Output capacitor (C_o)	$C_o = \frac{D \cdot T_s}{\frac{\Delta V_{Co}}{V_o} \cdot R_o}$; $D < 0.5$ $C_o = 1000$ μF $C_o = \frac{(2D-1) \cdot T_s}{2 \cdot \frac{\Delta V_{Co}}{V_o} \cdot R_o}$; $D > 0.5$	$C_o = \frac{(1-D)}{\frac{\Delta V_{Co}}{V_o} 8 L_2 R_o f_s^2}$; $hC_o = 1000$ μF
6	Switch voltage stress (V_{SW1}, V_{SW2})	$V_{SW1} = V_{SW2} = V_{D1} = V_{D2} = \frac{V_s + V_{DC}}{2} = 362.5$ V; switch voltage stress reduced to half	$V_{SW1} = V_{D1} = V_s + V_{DC} = 725$ V
7	No. of devices	Two switches and two diodes Two inductor and three capacitors	One switch and one diode Two inductor and two capacitors
8	Switch average voltage current (I_{SW1}, I_{SW2})	$I_{SW1} = I_{SW2} = I_{D1} = I_{D2} = I_{savg} + I_o$; $I_{SW1} = I_{SW2} = 21.46$ A; (same current stress)	$I_{SW1} = I_{D1} = I_{savg} + I_o$ $I_{SW1} = I_{D1} = 21.46$ A
9	Switching and conduction loss across switch	$P_{Sw(switch)} = P_{Sw(s)} = f_{sw}[0.5 \times V_{sw} \times I_{sw\_}\max \times (t_r + t_f)]$ $P_{sw(sw)total} = 0.5$ W $P_{C(switch)} = P_{CSw} = I_{sw\_rms}^2 \times R_{DS\_ON}$ $P_{C(sw)total} = 20$ W	$P_{sw(sw)} = 3.8$ W $P_{C(sw)} = 32$ W
10	Switching and conduction loss across diode	$P_{C(Diode)} = V_F \times I_D$ $P_{sw(D)total} = 0.8$ W $P_{Sw(Diode)} = 0.5 \times V_{RR} \times I_{RR} \times t_{rr} \times f_{sw}$ or $P_{Sw(Diode)} = Q_{RR} \times V_{rrm} \times f_{sw}$ $P_{C(D)total} = 9$ W	$P_{sw(D)} = 3$ W $P_{C(D)} = 18$ W

Appendix

S. no.	Specific parameters	Values
1	Single-phase supply voltage	230 V, 50 Hz
2	Input and output inductances (L_1, L_2)	5 mH
3	Intermediate capacitors (C_1, C_2)	10 μF
4	Output capacitor (C_0)	3000 μF
5	Switching frequency (f_s)	10 kHz
6	Load	400 V/8 A
7	Battery nominal voltage	345 V, 40 AH

Control parameters: Gains of output PI voltage controller $k_{pv} = 0.00005$, $k_{iv} = 20$ for CV mode, gains of the output PI current controller $k_{pi} = 0.1$, $k_{ii} = 10$ for CC mode and inner PI current controller $k_{p1} = 0.3$, $k_{i1} = 7.8$ same for both CV and CC mode operation; feed forward gain is $k_d = 1.8$.

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