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ORIGINAL PAPER

Simulation analysis of the switching of 230 kV substation shunt capacitor banks with a 6% series reactor for limiting transient inrush currents and oscillation overvoltage

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Abstract This paper presents the simulation and investigation of switching large shunt capacitor banks in a 230 kV Thailand substation system. Simulations are performed using PSCAD/EMTDC to determine the peak of the transient inrush currents, the oscillation overvoltage and the frequency of the inrush current. The inrush current is generated by energizing the 4 × 72 Mvar, 230 kV shunt capacitor banks. The purpose is to observe and investigate the behaviour of transient inrush currents and oscillation overvoltages to ensure the safe and successful operation of shunt capacitor banks. The methodology of inrush current transient analysis and transient reduction control was studied. The proposed method for controlling system transients during capacitor energization is through the use of a switching shunt capacitor bank with a series 6% reactor. The simulation cases for transient mitigation are numerically conducted for six different cases: a base case, with a pre-insertion resistor, with a pre-insertion inductor, with a current-limiting reactor, with a series 6% reactor and using synchronous closing control. The effects of parameters such as the sizing of the current-limiting reactor, the capacitor bank rating and the short-circuit impedance of the system are investigated. The simulation results demonstrate that the switching shunt capacitor bank with a series 6% reactor is effective in reducing the high transient inrush currents and oscillation overvoltages.

Keywords Shunt capacitor bank · Inrush current · Switching transients · Oscillation overvoltage · Current-limiting reactor · 6% reactor · Back-to-back capacitor switching

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1 Introduction

At present, the shunt capacitor bank is an important electrical equipment when we consider electrical systems in buildings, industries and utilities. The shunt capacitor bank generates the reactive power used in the network system. It is common practice to install shunt capacitors at all voltage levels in the power system. The application of shunt capacitor banks has many advantages such as reducing the power losses in power cables and transformers, improving the voltage profile in long transmission lines, increasing the system capacity, increasing the power factor, reducing the electricity bills and preventing penalty charges on kvar demand. These benefits apply to both distribution and transmission systems. However, the behaviour of the load profile of the system and the bus voltage are not constant, and shunt capacitor banks need to be switched in and out several times. The switching of shunt capacitor bank is a frequent utility operation that potentially occurs multiple times per day and hundreds of time per year throughout the system. It depends on the need for system voltage/Var support from the capacitor banks. Capacitor banks are applied to keep the reactive power at the voltage level of the transmission system. Transient-related currents and voltages appear on a power system as a result of utility capacitor bank installations, including voltage transients at the capacitor bank substation and neighbouring substations, thereby impacting the power quality on sensitive customer loads due to variations in voltage when capacitor banks are energized. In addition, capacitor bank switching can lead to the phenomenon of inrush currents. Inrush currents can cause the mal-operation of protective relays and insulation damage

of power equipment, especially power circuit breakers and capacitor units.

Therefore, the energization of capacitor banks, which affects the capacitive load, may lead to high transient inrush currents and oscillation overvoltage at the capacitor bank terminal. Capacitor bank energizing transients have becoming increasingly more important with the growing number of capacitor bank installations in power systems. When a capacitor bank is energized from a bus that does not have other capacitor banks energized, the situation is called "isolated capacitor bank switching"; on the other hand, when the capacitor bank is energized from a bus that has other capacitor banks energized, it is called "back-to-back capacitor bank switching" [1].

In addition to the work in various fields that are reviewed in this paper [2–42], there are many studies that focus on capacitor switching applications. A new method to determine the optimal location for capacitor banks and distributed generation (DG) systems has been proposed using multi-objective problem-solving techniques based on bacterial foraging particle swarm optimization (BF-PSO) [2]. The results from the simulation show that implementing the optimization algorithm can reduce the costs of power losses and improve the voltage profile of the system. Another study by Injeti and et al. used the Bat algorithm (BA) and Cuckoo search (CS) algorithm to determine the optimal placement of capacitor banks in a radial distribution and minimize the real power loss [3]. A shunt capacitor bank control strategy based on an ant colony system is shown in [4]. This can reduce the penalty bills of consumers by improving the power factor through the appropriate switching of shunt capacitor banks.

Capacitor switching transients were analysed to investigate the behaviour of high inrush currents and oscillation overvoltages for isolated capacitor banks. The transients that occur during capacitor bank energization are presented using both simulation and experimental measurements [5]. The mitigation of capacitor bank switching can be achieved using different techniques such as applying pre-insert resistors and series reactors, and synchronous switching control has been applied and simulated using systems with shunt capacitor banks in LV & MV distribution systems. According to the literature, pre-insertion resistors or pre-insertion inductors have been used in the electric utility industry for many years to control switching transients that result from the energization of the capacitor banks [6–8]. As a result, remote overvoltage mitigation methods have shown that pre-insertion inductors are not always as effective as pre-insertion resistors. The application of synchronous closing control is presented in the literature [9,10]. The paper discusses the functioning principles of modern methods for the synchronous switching of circuit breakers, especially for shunt reactors and capacitors, to limit the transients that occur. The problem of termination or failure on the high-voltage side is due to the installation of the capacitor bank on the low-voltage side [11]. This investigation is performed by the switching of an isolated capacitor bank in an electric distribution network. Methodologies for the analysis and control of the switching transients from the capacitor bank are discussed [12,13]. This includes a theory for controlling the switching transients along with simulation based on a distribution network. Isolated and back-to-back capacitor bank switching were studied. In the literature [14], the harmonic transients mitigation technique was studied by using a pre-insertion resistor at the distribution feeder. As a result, the pre-insertion resistor was effective in slightly reducing the harmonic transients. In addition, the mitigation of transients due to capacitor switching was presented in the literature [15,16]. However, the investigation was performed for a high-voltage system. The results show that the current-limiting reactor, pre-insertion inductor, synchronous switch and pre-insert resistor can significantly reduce the magnitude of transient inrush currents.

New innovations on transient mitigation techniques were presented in recent publications [17–27]. These methods proposed new techniques to limit transient inrush currents and overvoltage. They included decision tables [17], hybrid switches with controlled switching [18], thyristor-switched capacitors [19], changing the series reactor [20], new resistive capacitor switching transient limiters (RCSTLs) [23], mitigation techniques on MV-capacitor banks with VCBs [24], solid-state transient limiters for capacitor bank switching transient [25] and SVCs used instead of circuit breakers [26]. Some research papers have demonstrated the application of FACT devices, for instance, by applying TCSCs, static var compensators, STATCOM and power electronic devices [28–42]. The design of a reactive power control relay that measures reactive power and controls the capacitor bank pattern that can achieve desire reactive values has also been proposed [29]. Karaki and et al. [30] present a method for optimal capacitor placement using genetic algorithms to reduce the effect of simultaneous switching noise. A technique that involves soft-switching CSIs for photovoltaic systems to reduce switching losses with H-type communication modules was proposed in [35]. The optimum sizing of harmonic filters for industrial plants using a GA-based optimization approach is presented in [40]. These applications provide fast switching because of their operation at zero voltage. However, most studies were performed on distribution feeder and involved the use of knowledge in the field of power electronics device including mathematically applied algorithms. The results of these transient mitigation methods were successful. However, when considering harmonic distortion on the system due to nonlinear load connections on the bus, these methods are ineffective because of the resonance problem, and more investigations are required. Therefore, these mitigation methods cannot be implemented in industrial applications where high levels of harmonic currents are present.

Therefore, this paper presents a technique of limiting the high transient inrush current and oscillation overvoltage when switching shunt capacitor banks in an HV substation by using a series 6% reactor. The system under consideration is the typical capacitor bank switching configuration in a 230 kV substation in Thailand. The typical size of each capacitor bank in a 230 kV system is 4 steps, and the size of each step is 72 Mvar; the capacitor banks are connected in parallel with the network systems. The inrush current and oscillation overvoltage are simulated using PSCAD/EMTDC. This software is mostly used to analyse the electromagnetic transient phenomena of power system. The inrush current and oscillation voltage waveforms obtained from PSCAD/EMTDC are analysed for various cases. The technique to reduce transient overvoltage and inrush current is examined with six different system configurations including the base case (without transient limiting), using pre-insertion resistors, using pre-insertion reactors, using a current-limiting reactor, using a 6% reactor (the novel proposed technique) and synchronous closing control. This paper covers different operational cases to find the suitable method or technique that can be used to limit the transients from capacitor switching. The effects of parameters such as sizing of the current-limiting reactor, the capacitor bank rating and the short-circuit impedance of the system are investigated. The simulations results show that shunt capacitor bank switching with a series 6% reactor is effective in reducing the high transient inrush current and oscillation overvoltage. The utilization of a series 6% reactor with preselected values is an effective and economical approach to limit high transient inrush current and overvoltage and to prevent harmonic amplifications due to resonance issues. The peak inrush current and oscillation overvoltage obtained using a series 6% reactor are lower than those obtained for the base case, and the pre-insertion inductor, the pre-insertion resistor and current-limiting reactor techniques. The synchronous closing control is more effective than the series 6% reactor in limiting the transient inrush current and overvoltage. However, the results for the inrush current and overvoltage for both methods are similar. The 6% reactor can be used in industrial applications where high levels of harmonic currents are present. On the other hand, the other techniques cannot be implemented when there is harmonic distortion due to resonance issues. In future, the 6% reactor technique is promising and can be implemented for HV industrial loads, which have harmonic distortion. Typically, the 6% reactor method should be implemented for nonlinear loads where more than 25–30% of the total load is on the bus. In addition, the proposed methodology involves easy installation, it does not require autonomous control, it is effective for limiting fault outrush currents and it is low maintenance. However, the space requirement needs to be considered.

Furthermore, the results of the peak inrush current and oscillation frequency are compared for the PSCAD/EMTDC simulation, and the calculation was performed in accordance with public standards, IEC standard 60871-1:2005 [16] and IEEE standard C37.012:2005 [43], when transient reduction control is performed with the current-limiting reactor and only the 6% reactor.

2 Basic theory

2.1 Capacitor bank configuration

HV substation shunt capacitor banks are normally designed by series and parallel connections of single-phase capacitor units. In this paper, these banks use an H-configuration on each phase with a current transformer in the connecting branch to detect the unbalanced current [44]. This arrangement is used on large banks with many capacitor units in parallel. The employed 72 Mvar 230 kV shunt capacitor bank configuration is illustrated in Fig. 1.

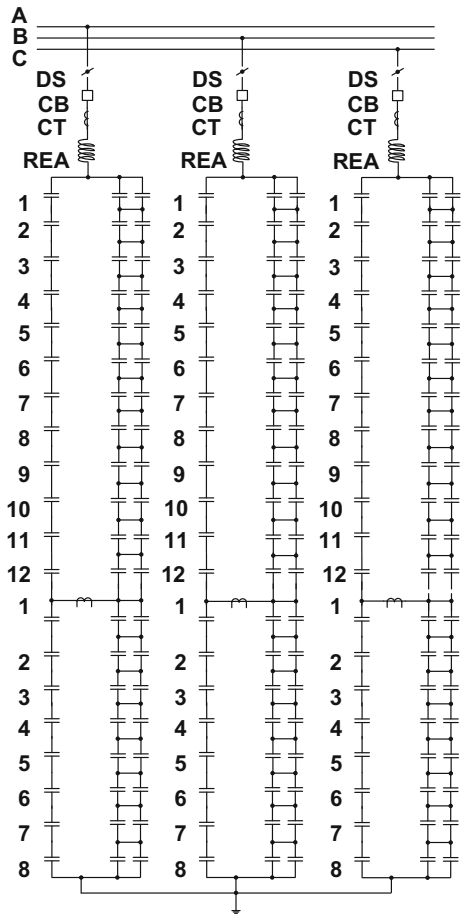


Fig. 1 The 4 × 72 Mvar 230 kV substation shunt capacitor bank [45]

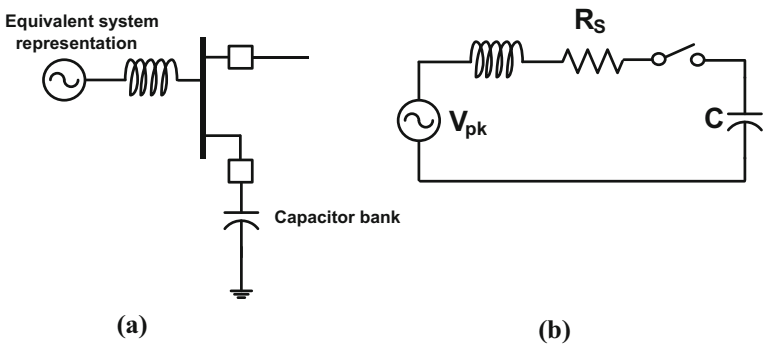


Fig. 2 System diagram and equivalent circuit for isolated capacitor switching operation. **a** System diagram. **b** Equivalent circuit

In Fig. 1, the grounded-wye capacitor banks are composed of series- and parallel-connected capacitor units per phase. The existing 72 Mvar, 230 kV shunt capacitor bank has a current-limiting reactor of 1 mH applied in series with the bank for reducing the transients. To compensate the increased reactive power, the capacitor banks are installed more than one step into the system at the same bus.

2.2 Isolated capacitor banks

Figure 2a shows a representative system of the isolated switching capacitor bank, and Fig. 2(b) shows an equivalent circuit for energizing an isolated capacitor bank from a predominantly inductive source. Note that the inductance between the capacitor bank and circuit breaker is L_1, the source inductance of the system is L_s and capacitance of the capacitor bank is C_1. The inductance L_1 includes inductances of the series reactor, capacitor bank and line power cable. This inductance helps to limit the inrush current and frequency. The circuit consists of a source inductance L_s in series with the capacitor bank $C_1 \times L_1$, which can be disregarded when $L_s \gg L_1$. In this case, the peak of the inrush current $\left(i_{i\,\mathrm{peak}}\right)$ is reached, and the inrush current frequency (f_i) is limited by the source impedance L_s [43].

A shunt capacitor bank is considered isolated when the inrush current upon energization is limited by the inductance of the source and the capacitance of the bank being energized. A capacitor bank is also considered isolated if the maximum rate of change, with respect to time, of the transient inrush current upon energizing an uncharged bank does not exceed the maximum rate of change of the symmetrical short-circuit current at the voltage at which the current is applied. Considering a discharged capacitor bank, the current is given by the following equation [43]:

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_{\max} = \omega_s I_{\mathrm{sc}}\sqrt{2} \tag{1}$$

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_{\max} = 2\pi f_i i_{\mathrm{i\,peak}} \tag{2}$$

$$i_{i\,\max} = \sqrt{2}\sqrt{I_{\mathrm{sc}} I_1} \tag{3}$$

$$f_i = f_s\sqrt{\frac{I_{\mathrm{sc}}}{I_1}} \tag{4}$$

where I_{sc} is the rated symmetrical rms short-circuit current of the source (A, rms), $I_{i\,\mathrm{peak}}$ is the peak value (A) calculated without damping, $\left(\frac{di_\mathrm{i}}{dt}\right)_{max} = 2\pi f_i i_{\mathrm{i\,peak}}$ is the rate of change of current for the isolated bank switching (A/μs), $\left(\frac{di_\mathrm{i}}{dt}\right)_{max} = \omega_s I_{sc}\sqrt{2}$ is the maximum rate of change for a rated short-circuit current (A/μs), $\omega_s = 2\pi f_s$ is the angular frequency of the system (rad/s), f_s is the power frequency (Hz) and f_i is the inrush current frequency (Hz).

The transient inrush current for an isolated bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank as the frequency approaches 1 kHz. Because a circuit breaker must meet the making current requirements of the system, the transient inrush current is not a limiting factor in isolated capacitor bank applications. So, the transient mitigation method for isolated capacitor banks is not considered.

2.3 Back-to-back capacitor banks

Figure 3a shows a representative system of the back-to-back switching shunt capacitor bank, and Fig. 3b shows an equivalent circuit. Note that the inductance between the capacitor bank and circuit breaker is L_1, the source inductance of the system is L_s, the inductance of the bus between switching devices is L_{bus} and the capacitance of the capacitor bank is C_1. The inductance L_1 includes inductances of the series reactor, capacitor bank and line power cable. The inductance in the circuit that limits the transient oscillatory current is composed of $L_{\mathrm{bus}}, L_1, L_2$ and any additional reactance inserted. Therefore, the limiting inductance (the inductance between bank 1 and bank 2) is very important for reducing the transient inrush currents and frequency [39].

By considering Fig. 3, when the capacitor bank 1 is connected to the busbar and the capacitor bank 2 is about to be connected, the high inrush current associated with the charging of capacitor bank 2 is supplied by capacitor bank 1 (i.e.

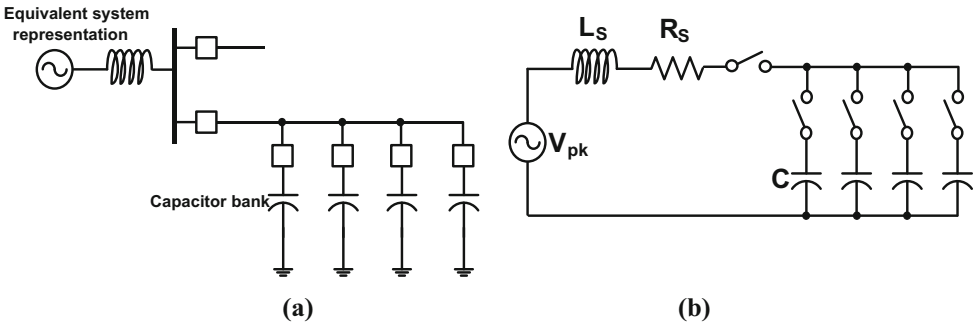


Fig. 3 System diagram and equivalent circuit for back-to-back capacitor switching operation. **a** System diagram. **b** Equivalent circuit

back-to-back switching). Back-to-back switching involves energizing a capacitor bank on the same bus when another energized bank is present. In this case, the magnitude and frequency of the high inrush current can be calculated as follows in Eqs. 5 and 6 [43]:

$$i_{i\,\mathrm{peak}} \approx 13{,}500\sqrt{\frac{\mathrm{U_r} I_1 I_2}{f_s L_{\mathrm{eq}}(I_1 + I_2)}} \tag{5}$$

$$f_i = 9.5\sqrt{\frac{f_s U_{\mathrm{r}}(I_1 + I_2)}{L_{\mathrm{eq}} I_1 I_2}} \tag{6}$$

where $I_{i\,\mathrm{peak}}$ is the inrush current peak (A, rms), $I_{1,2}$ are the capacitor bank currents (A, rms), L_{eq} is the equivalent inductance (μH) and U_{r} is the rated voltage (kV, rms).

These equations can also be used for computing inrush currents when more than two capacitor banks are switched back to back by accurately calculating the equivalent inductance. In practice, these equations will consider safety factors such as the tolerance of the capacitor unit, the harmonic content for an effective ground and the ratio of the voltage increase [43].

3 Transient reduction control

The magnitude and frequency of the inrush current must be limited to ensure the proper operation of the switching device as well as relay, fuses and more. At the present time, the mitigation methods of capacitor bank switching transients can be controlled by a variety of solutions [17–27]. Some of these techniques are presented here in detail as common methods that are used for the control of transients.

3.1 Pre-insertion resistors (PIRs)

The use of switching resistors in high-voltage breakers is well known to reduce overvoltages and the frequency of the transient recovery voltage. PIRs are usually fitted on circuit breakers and as such add to the complexity of the equipment.

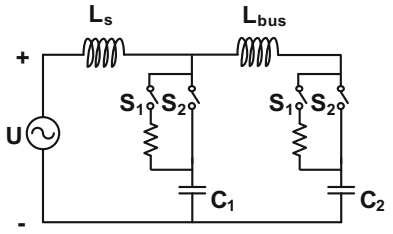


Fig. 4 Equivalent circuit of capacitor switching with PIR

Depending on the design, the added complexity may or may not result in a reduced availability of the equipment.

In Fig. 4, the resistor size is normally based on ensuring that the initial transient when the resistor closes is the same as the subsequent transient for resistor bypass (shorting). The operating time of the switch is about one-fourth of a cycle at 50 Hz (typically 5–15 ms) [46,47]. In power systems, the resistance is typically much less than the reactance. Therefore, the frequency of the transient is reduced to zero by using a pre-insertion resistor with the following value in Eq. 7 and 8 [12]:

$$r = \frac{1}{2}\sqrt{\frac{L}{C}} \tag{7}$$

Equation 7 can be converted into the following convenient form:

$$r = \frac{1}{2}\sqrt{\frac{V_{\mathrm{LN}}}{I_{\mathrm{sc}}\omega C}}. \tag{8}$$

3.2 Pre-insertion inductors (PIIs)

In Fig. 5, the inductors shown provide a large impedance between the capacitor banks to limit the inrush current. The high resistance of pre-insertion inductors will further limit the inrush current through damping similar to the case of pre-insertion resistors. Pre-insertion inductors, which were traditionally primarily used for overcurrent control for back-to-back capacitor switching applications, also provide magnitude reduction for transient overvoltages. Pre-insertion

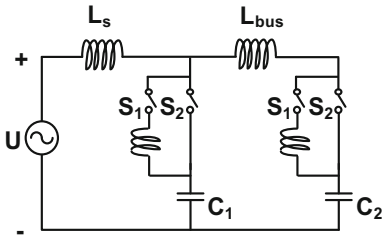


Fig. 5 Equivalent circuit of capacitor switching with PII

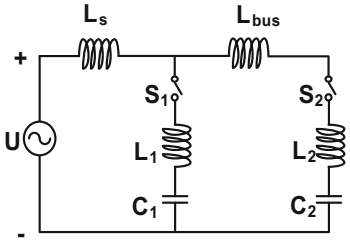


Fig. 6 Equivalent circuit of capacitor switching with CLR

inductors are generally very effective for reducing overvoltages if the inductance is equal to or greater than the source inductance [1].

The limitation of the transients has been performed using inductors (with resistance) inserted into the capacitor closing circuit for 7–12 cycles during the closing of the disconnect blade [46–48].

3.2.1 Current-limiting reactors (CLRs)

As shown in Fig. 6, this method can be performed by putting a reactor in series with the capacitor bank to decrease the peak current and frequency of the oscillatory inrush transients. The reactor increases the magnitude of the surge impedance, which effectively reduces the peak value of the inrush current. The sizing of the current-limiting reactor will limit the inrush current and force it to not exceed 100 times of the rated capacitor bank current [31,43].

Current-limiting reactors are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltage.

3.3 Detuning 6% reactor

The equivalent circuit of a detuning 6% reactor is the same as the energized capacitor bank circuit with the CLR, as shown in Fig. 6. This method is used to prevent resonance problems and to keep the resonance frequency as far away as possible from the harmonic frequencies that have considerable amplitudes. The most common solution to avoid resonance problems is to connect a 6% reactor in series with the capacitor and tune it to a series resonance frequency, which is below the lowest frequency of the harmonic voltages and currents in the network. This can be performed by changing the inductive reactance value of the series reactor to a value that is 6% of the capacitive reactance of the capacitor. The reactor may be specified by its relative impedance, as expressed in Eqs. 9 and 10 [49]:

$$\rho = \frac{|XL_1|}{|XC_1|} \tag{9}$$

The tuning order is given as follows:

$$\frac{f_{\mathrm{LC}}}{f_1} = \sqrt{\frac{1}{\rho}} \tag{10}$$

In most networks, the fifth harmonic is the lowest frequency with a considerable amplitude. For such networks, it is useful to choose a capacitor–reactor connection with a tuning frequency below $5 \times f_1$. The capacitor–reactor connection will be tuned to $4.08 \times f_1$ with a $\rho = 6\%$ reactor and a compensation power at the original power frequency.

3.4 Synchronous closing control

This method involves controlling the switching device to close at the instant a zero voltage difference is observed across the switch. Synchronous closing involves the independent contact closing of each phase near a zero voltage, as illustrated in Fig. 7 for grounded and ungrounded capacitor bank. For synchronous closing control of an energized capacitor bank, the three-pole circuit breaker should close at different times. The time differences depend on the application. For controlled capacitor bank energization, the operation of the three poles should be closed with a time separation of 1/6 cycle (3.33 ms at 50 Hz). In addition [9,50,51], the capacitor bank with an ungrounded neutral and voltage phase A (or voltage phase L1), which is the reference phase, and the two-pole circuit breaker (phase L1 and L2) should be closed simultaneously when the voltages of phase A and phase B are zero, and then, after a 1/4 cycle or later (or 5 ms at 50 Hz), the circuit breaker of phase C should be closed. Figure 8 shows the principle of synchronous closing for a single-pole circuit breaker operation, which can be controlled with respect to the point-on-wave position to prevent the generation of harmful transients.

For a three-pole operated circuit breaker, the required time difference must be obtained by modifying the operation mechanism (mechanical staggering) [9].

4 System simulation modelling

To obtain inrush current and transient oscillation voltage signals for investigation and analysis, PSCAD/EMTDC [52]

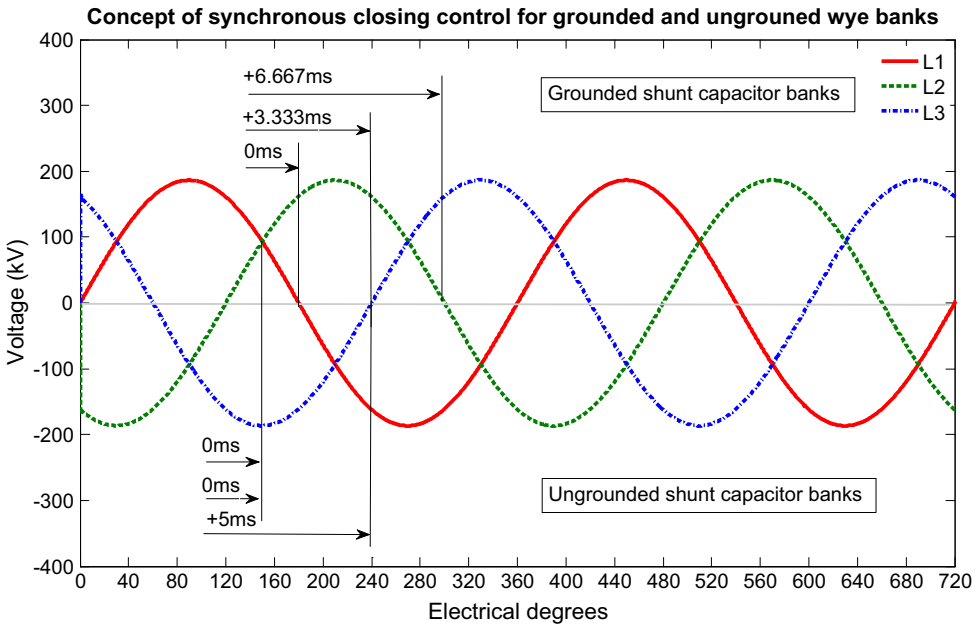


Fig. 7 Concept of synchronous closing control for single-pole operation of grounded-wye and ungrounded-wye capacitor banks

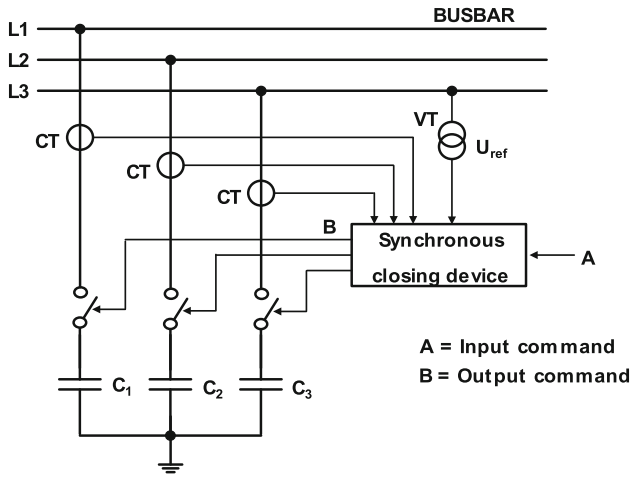


Fig. 8 Operating principle of synchronous closing control for single-pole operation of a circuit breaker

was used in simulations with a sampling frequency rate of 250 kHz. The system under study includes cable and loop inductances between 4-step capacitor banks. The system under investigation is a 230 kV HV substation that is a part of the Thailand electricity transmission network system, as shown in Fig. 9 [45]. The three-phase voltage source model is represented by equivalent circuit with a short-circuit value of 10 kA, which is the connecting bus of the proposed capacitor bank. The equivalent 500 kV system has a positive impedance sequence of 0.00022 p.u. and 0.00622 p.u. The step-down power transformer is rated 525/242-22 kV, and the impedance voltage at phase A is 21.63%. The bus impedance (Z_{bus}) is connected between each capacitor bank. A typical value of the inductance per phase between back-to-back switching capacitor banks and the bank inductance for a 230 kV voltage level is 0.935 μH/m [43]. This value does not include the inductance of the capacitor bank itself or the inductance of the installed reactor. The tapping conductor from the busbar to capacitor bank is at 1272 MCM ACSR conductor per phase. This cable conductor has an inductance of 0.072 Ω/1000 ft. and a reactance of 0.0173 Ω/1000 ft. The capacitor unit has a rating of 400 kvar, 6.9 kV. The power circuit breaker is three-pole operated with a built-in mechanical phase shift for control switching. The mechanical phase shift is adjusted (staggered) to ensure that the contact closing for all poles occurs at the intended times.

By considering Fig. 9, the capacitor bank no.1 group was simulated while the capacitor bank no. 2 to 5 groups were disconnected. The capacitor bank switching in the no.1 group includes 4-step capacitors, which are rated 72 Mvar, 230 kV, and each step has the bank configuration shown in Fig. 1. Here, the capacitor units are rated 400 kvar, 6.9 kV, with a total of 180 units per step. To obtain the switching transient patterns, the simulations to investigate the peak inrush current, the highest magnitude of the transient overvoltage as well as the inrush oscillation frequencies was varied into six different cases:

- Simulations using a base case (uncontrolled transient energization) by energizing the capacitor bank up to a 4-step H-connection with a grounded wye, rated 4 × 72 Mvar, 230 kV and 50 Hz.
- Simulation using the pre-insertion resistors, each with a resistance value of approximately 86 Ω.
- Simulation using the pre-insertion inductors, each with a reactance value of approximately 119 mH.

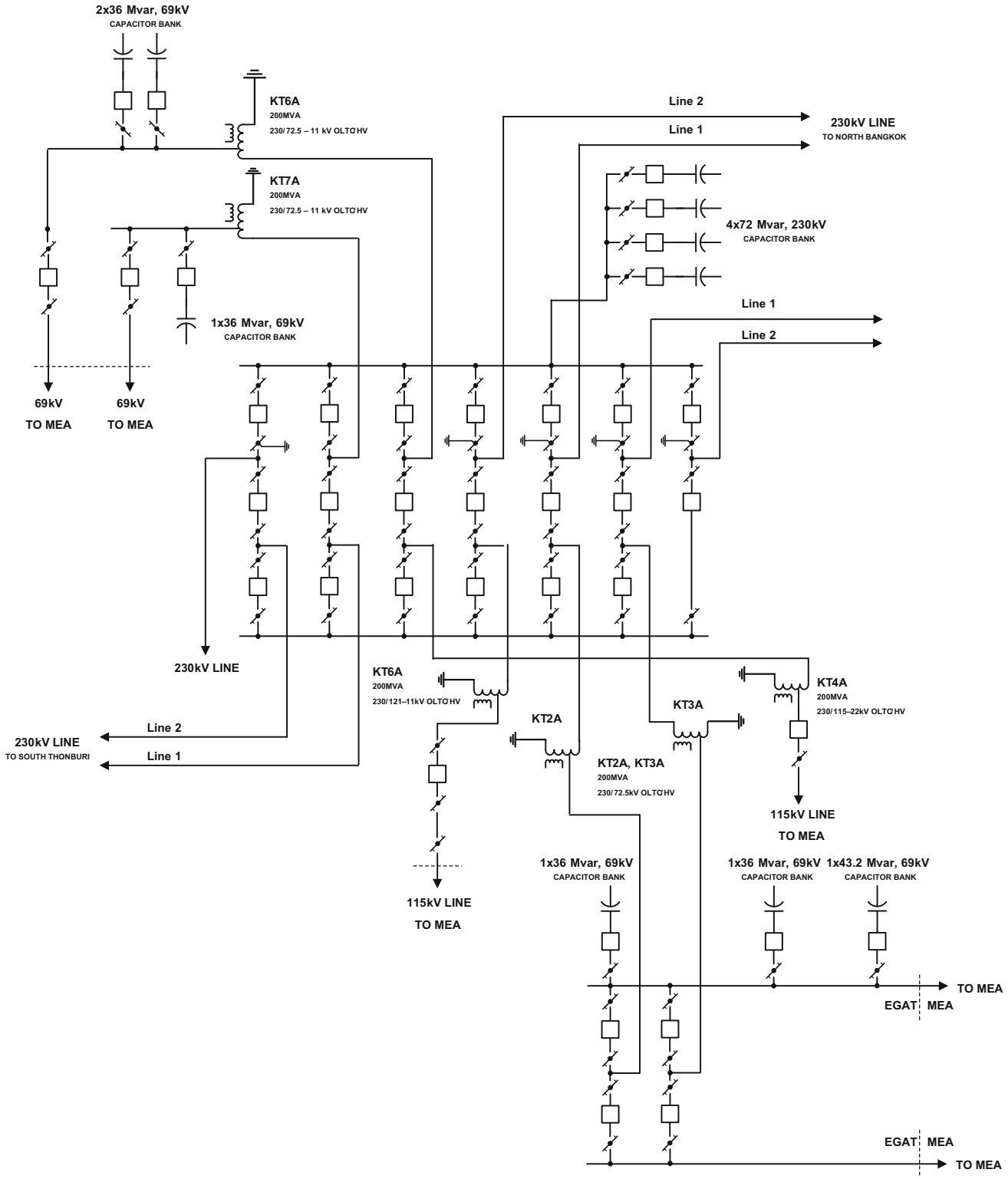


Fig. 9 System used in simulation studies for back-to-back capacitor switching transients [45]

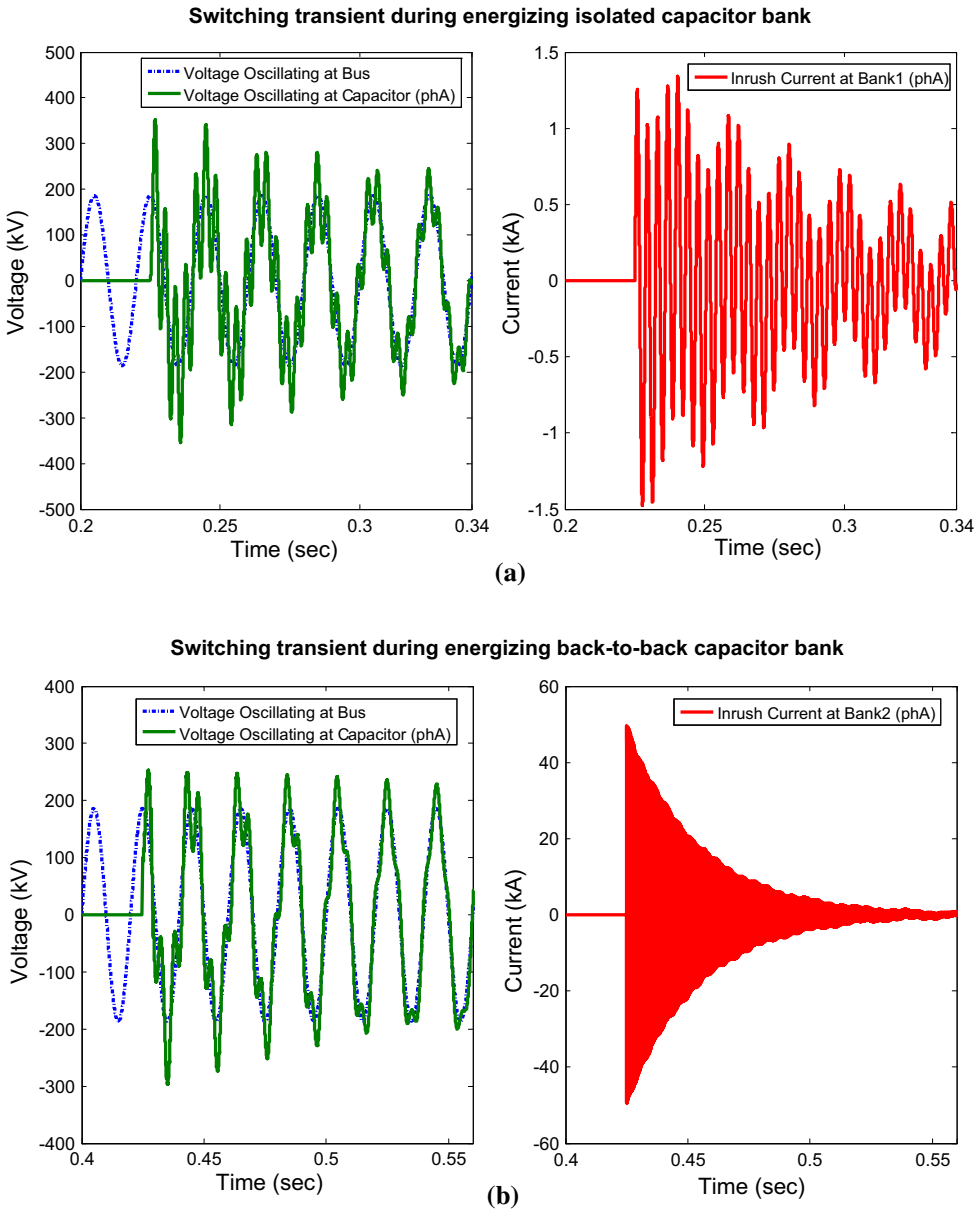


Fig. 10 Capacitor switching transient for inrush current and oscillation overvoltage waveform at phase A. **a** Energizing as isolated capacitor bank. **b** Energizing as back-to-back capacitor bank

– Simulations using the current-limiting reactors, each with an inductance value of approximately 1 mH per phase.
– Simulations using the series 6% reactors, each with an inductance value of approximately 166 mH per phase.
– Simulations using synchronous closing control for the controlled shunt capacitor bank.

Finally, the switching of the substation shunt capacitor banks was simulated without the connected load to determine the worst case of the highest inrush current and overvoltage.

The capacitor switching transient patterns in the simulations are obtained by changing the system parameters in the following ways:

– Variation of the impedance of short-circuit system to investigate the effect of fault currents at the capacitor bank bus at 5, 10, 20, 30 and 40 kA, which represent various substation locations and energization with a 1 mH CLR.
– Variation of the capacitor bank sizing to study the effect of capacitor bank size at 48, 52, 56, 60, 64, 68, 72, 76 and 80 Mvar at a bus voltage of 230 kV and energization with a 1 mH CLR.
– Variation of the sizing of the current-limiting reactor at 0.1, 1, 5 and 10 mH to study the behaviour of transient inrush currents for the existing 230 kV capacitor bank.

Figure 10 shows the waveform comparison between the isolated and back-to-back switching capacitor banks. Generally, the isolated capacitor bank switching has an inrush frequency between 300 Hz to 2 kHz.

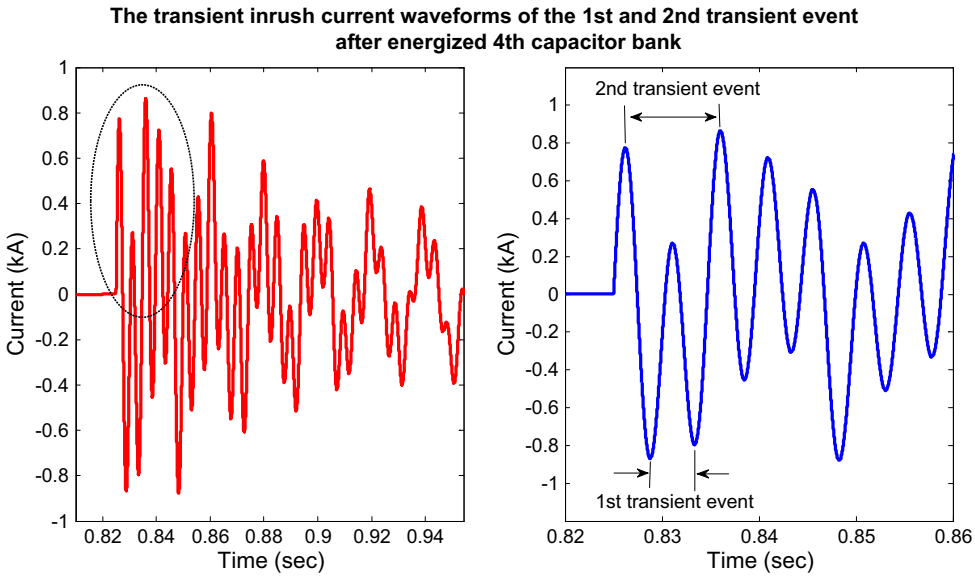


Fig. 11 Transient inrush current waveforms of the first (fi, 1) and second transient events

Table 1 Peak inrush current, event frequency and highest bus overvoltage in the base case (no transient limiting)

Step	Peak current and overvoltage in the base case						
	PSCAD/EMTDC				IEEE Std C37.012		IEC Std 60871-1
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$i_{i,\text{peak}}$ (kA)
1	1.476	0.284	–	353.516	1.943	0.364	2.063
2	49.584	22.727	0.210	296.023	50.106	18.680	54.052
3	64.470	20.833	0.498	259.736	63.908	17.869	72.069
4	74.488	20.833	0.989	263.598	70.416	17.501	81.078

The typical amplitude of the inrush current for back-to-back energization is several kAs with a frequency of more than 2 kHz. The magnitude and frequency of this inrush current are, therefore, much higher than that of an isolated bank.

In Fig. 11, the first rapid transient represents an exchange of charges during the capacitor switching; the two capacitor banks are brought to a common voltage since losses damp out the transients in practical installations. The common voltage is different from the supplied voltage, so a second transient occurs, during which the two capacitor banks are restored to supply voltage [53,54].

5 Simulation results

In this study, the magnitudes of the transient inrush current and oscillation overvoltage were simulated. Then, the simulation results were investigated for different cases, as follows.

5.1 Simulation for the base case

The capacitor banks are energized without the transient reduction technique. The controlled capacitor bank was switched into the network, and the worst-case switching occurs at the peak of the phase A voltage. The peak inrush current, the highest magnitude of the transient overvoltage and the inrush current frequencies under a 10-kA short-circuited system are summarized in Table 1.

By considering the data in Table 1 and Fig. 12, the simulation results indicated that the inrush current at step 4 will higher than when compared with another steps. The peak inrush current increases as the number of switching steps in the system increases because the large electric discharge from the switched capacitor bank will discharge energy to the capacitor bank to which it is to be connected. If the system has many capacitor switching steps, the inrush current is very high, especially for the last switching step. The frequency of inrush was exceeding 20 kHz in last step switching according to PSCAD simulation. Meanwhile, the highest oscillating transient overvoltage at the bus decreases because the shared common voltage among the capacitor banks increases. Therefore, the magnitude of the oscillating voltage from the shared common voltage in the system is reduced. In case of the inrush current frequency, the frequency of the first transient event is faster than that of the second transient event because the loop inductance between capacitor banks is very low. When the number of switching

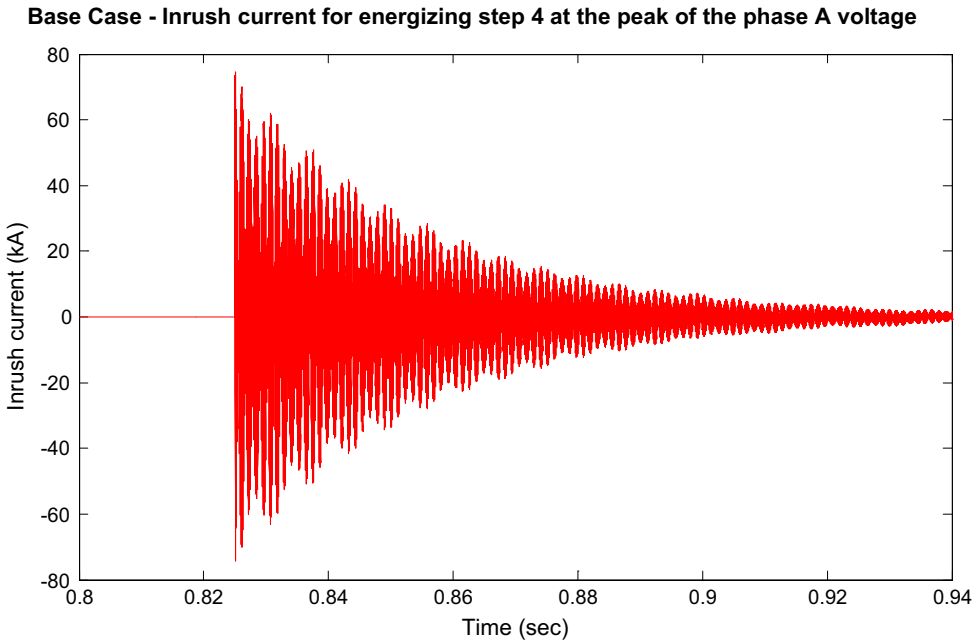


Fig. 12 Inrush current for energizing step 4 at the peak of the phase A voltage, I_{peak} (phase A) = 74.488 kA

steps is increased, the capacitance in the system is increased, and this leads to a lower oscillation frequency.

The IEEE standard C37.06 is used for the back-to-back capacitor bank switching current for a 245 kV circuit breaker at approximately 20 kA and an inrush current frequency of approximately 4.3 kHz [54]. By considering the results in Table 1, the inrush current for back-to-back switching in the second step is 49.584 kA and the frequency is approximately 22.727 kHz. This indicates that the circuit breaker is suited for the back-to-back capacitor switching application. It requires, then, a breaker of higher interrupting rating. Various mitigation methods for limiting the transient inrush currents will be discussed in the next section of this paper by comparing the effectiveness of each mitigation method in controlling the switching transients.

5.2 Simulation using the pre-insertion resistor

In order to damp the transient inrush currents, the resistors were connected in series with the controlled switching capacitor bank. This mitigation method is a conventional technology that requires the use of an additional switch to bypass the resistors for one quarter of a cycle after the energization of the controlled bank. The resistors were bypassed from the circuit to reduce the steady-state losses. The sizing of the resistor was calculated using Eqs. 7 and 8. The simulation result with the insertion of an 86 Ω resistor is presented in Table 2.

As a result in Fig. 13, the peak inrush current increases as the number of switching steps increases. The simulation indicates that the fourth-step switching is so high when compared with another steps. The first transient event is the capacitor current made through the pre-insertion resistor (S1). The operating time of switching resistor is about 1/4 cycle at 50 Hz (typically 5–15 ms). Then, the switching device will close the main circuit breaker (S2) and bypass the switch of resistor (S1) in order to prevent high losses from resistor. So, the second transient event will occur. The second transient is a high transient inrush current, and the peak is higher than the first transient event because no damping equipment. Transient inrush current flows to main contact of switching device instead resistor. It is interesting to note that the transient was damped faster with these resistors than with reactors. However, when bypass resistor and close with main contact of switching device, the transient was damped longer because the circuit does have resistance for damped. By observing the data in Table 2, the high frequency of inrush current was very similar to the one obtained in the base case simulations. This is because the inductance and capacitance of the circuit were not changed. In addition, the oscillation overvoltage is significantly reduced when compared with the base case. The peak inrush current is lower than the base case because the

Table 2 Peak inrush current, event frequency and highest bus overvoltage with the 86 Ω pre-insertion resistor

Step	Pre-insert resistor			
	PSCAD/EMTDC			
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)
1	0.851	0.284	–	240.191
2	8.582	20.833	0.218	235.160
3	11.613	20.833	0.497	236.054
4	12.714	20.833	0.873	257.648

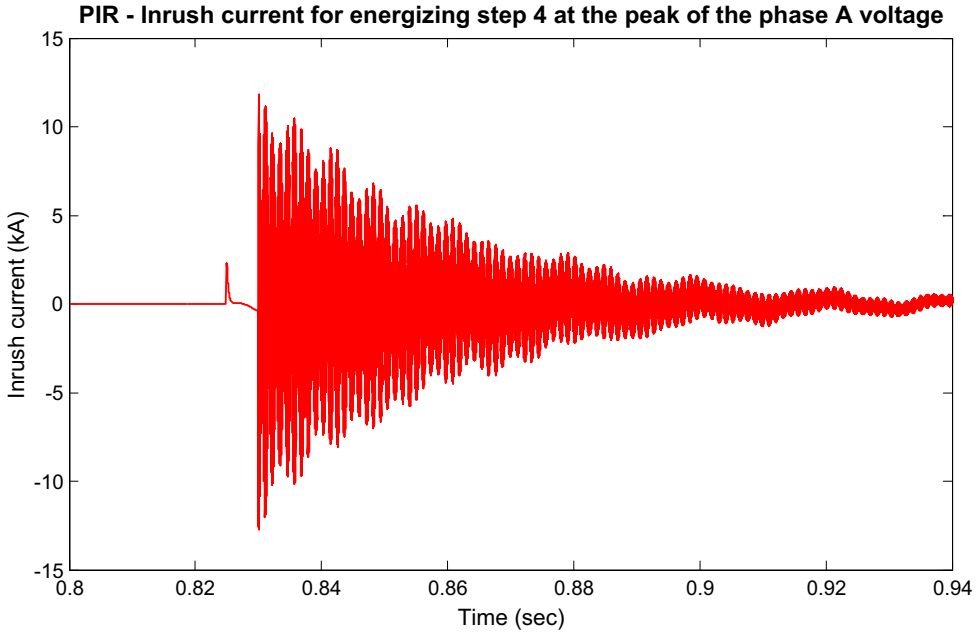


Fig. 13 Inrush current for energizing step 4 at the peak of the phase A system voltage, I_{peak} (phase A) = 12.714 kA

inserted resistor reduces the magnitude of inrush currents and provides damping of the transients. The peak inrush current is reduced to half of the base case value. It can be observed that the frequency of the high inrush current was very similar to the one obtained in the base case simulations. This is because the source inductance and capacitance were not changed. The high transient inrush current with the pre-insertion resistor is 12.714 kA, and the frequency is 20.833 kHz. The inrush current value is less than the standard limit. However, the inrush frequency is higher than the standard limit.

Table 3 Peak inrush current, event frequency and highest bus overvoltage with the 119 mH pre-insertion inductor

Step	Pre-insert inductor			
	PSCAD/EMTDC			
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)
1	0.366	0.288	–	256.289
2	8.378	20.833	0.204	261.862
3	9.042	20.833	0.498	269.647
4	9.634	20.833	0.876	299.968

5.3 Simulation using the pre-insertion inductor

For this analysis, the energization of the capacitor bank was performed using a 119 mH inductor (with a resistance of 3.783 Ω) inserted into the capacitor closing circuit for 0.14 sec. The worst-case transient occurred when the initial switch closing occurs at a voltage peak, and the bypass for the inserted device occurs at a current peak. As a result, the peak inrush current is lower than the base case and that of the PIR because the inserted inductor provides a high impedance between the capacitor banks to limit the inrush current.

In Table 3 and Fig. 14, the simulation indicated that the isolated capacitor bank switching provides the low transient inrush current. By the way, the fourth-step switching is so high when compared with another steps due to the capacitor bank switched as back to back. The oscillation overvoltage cannot control in last step. The oscillation overvoltage seems to be increased due to the effect of inductor on the circuit. The inductor has a low resistance. So, the transient inrush current has a long time to the final steady state. The shunt capacitor switching has shown that pre-insertion inductor is not effective to reduce oscillation overvoltage. The high resistance of pre-insertion inductors further limits inrush currents through damping transients, as in the case of PIRs. However, the oscillation overvoltage of both the bus and capacitor bank is significantly increased when we compared with the base case because the sizing of inductor is less than the source inductance. Therefore, the PII method is not effective for overvoltage reduction. The pre-insertion inductor will be effective when the inductance of the pre-inserted inductor is equal to or greater than the source inductance. In addition, the inrush current value is less than the standard limit, but the inrush frequency is higher than the standard limit.

5.4 Simulation using the current-limiting reactor

The inductance value of the current-limiting reactor is approximately 1 mH per phase. As a result, the magnitudes of the inrush current and frequency are decreased, while the highest transient oscillation overvoltage decreases slightly when compared with the base case. The use of the current-

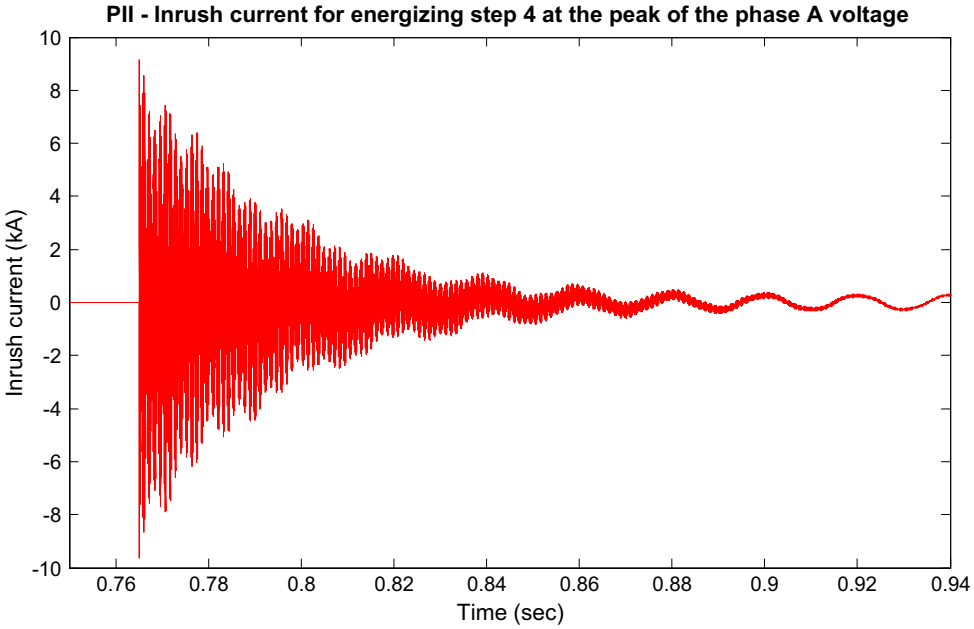


Fig. 14 Inrush current for energizing step 4 at the peak of the phase A system voltage, I_{peak} (phase A) = 9.634 kA

Table 4 Peak inrush current, event frequency and highest bus overvoltage with the 1 mH current-limiting reactor

Step	Peak current and overvoltage in the current-limiting reactor						
	PSCAD/EMTDC				IEEE Std 37.012		IEC Std 60871-1
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$i_{i,\text{peak}}$ (kA)
1	1.470	0.274	0.054	357.111	1.943	0.364	2.063
2	6.241	2.506	0.192	291.217	6.438	2.400	5.913
3	7.931	2.488	0.156	276.086	8.577	2.398	7.883
4	9.517	2.469	0.139	258.226	9.646	2.397	8.869

limiting reactor may lead to a lower frequency of transient oscillations. This mitigation method is applied in the existing 230 kV capacitor bank in Thailand substation systems.

According to the data in Table 4 and Fig. 15, the simulation results indicated that the fourth-step switching is so high when compared with another steps. The oscillation overvoltage will be reduced when we increase the number of step switching. Also, it can be seen that the frequency of high transient inrush current was reduced so much when compared with base case. The frequency of inrush current will be reduced slightly when we increase the number of step switching. Moreover, the transient inrush current is lower than base case, PIR and PII. Since the current through the reactor cannot change instantly, the higher-frequency components of the transient are limited and the severity of the inrush current transient is reduced. Sometimes reactors are intentionally built with higher resistances to increase the damping of the transient. The inrush current value is lower than the standard limit. This confirmed the assumption that increasing the surge impedance of the circuit would reduce the high-frequency transients. In addition, the inrush current and frequency are less than the standard limits. So, this concludes that this mitigation method is suited for the back-to-back capacitor switching applications in 230 kV systems.

5.5 Simulation using the 6% reactor

The 6% reactor was used to limit the peak inrush current between the banks, which is the same mitigation approach when using the current-limiting reactor. The simulation results are given in Table 5.

In Table 5 and Fig. 16, the simulation results indicated that the transient inrush current is lower than base case, PIR, PII and CLR. The oscillation overvoltage slightly reduces in first step. But when we increase number of step switching, the oscillation overvoltage will increase due to the effects of inductor in circuit. The frequency of inrush current is lower than base case, PIR, PII and CLR because the large inductance values can help to damp the oscillation and fast to final steady state. The transient inrush current when switching in 1$^{\text{st}}$ step is higher than another step because the source impedance is lower than the inductance of the capacitor

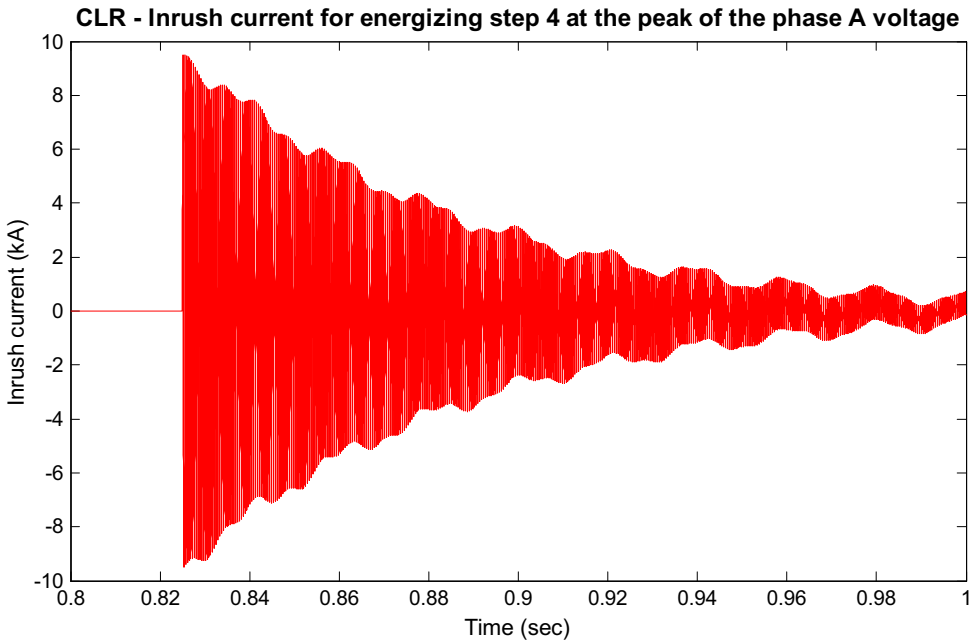


Fig. 15 Inrush current for energizing step 4 at the peak of the phase A system voltage, I_{peak} (phase A) = 9.517 kA

Table 5 Peak inrush current, event frequency and highest bus overvoltage with the 166 mH 6% reactor

Step	Peak current and overvoltage in the 6% reactor						
	PSCAD/EMTDC				IEEE Std C37.012		IEC Std 60871-1
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$i_{i,\text{peak}}$ (kA)
1	0.967	0.172	–	237.663	1.766	0.400	1.788
2	0.898	0.190	0.050	226.596	0.458	0.207	0.440
3	0.812	0.205	0.050	243.094	0.611	0.207	0.587
4	0.879	0.212	0.052	242.589	0.687	0.207	0.660

bank each of step. The 6% reactor is also advantageous for reducing the harmonic voltages in the network by absorbing the part of the harmonic currents with orders higher than the tuning frequency of the capacitor–reactor arrangement. Therefore, the inductance value in this paper is approximately 166 mH per phase, which can be calculated by Eq. 9 and is in accordance with IEC 60871-1 [16] and IEC 61642 [49]. The 6% reactor is normally used to prevent resonance problems and to keep the resonance frequency as far away as possible from the harmonic frequencies, which have considerable amplitudes. Consequently in Table 5, the peak inrush current is reduced comparing with the base case, and the PIR, PII and CLR cases because the high inductance value in the circuit limits the peak of the inrush current. However, the large inductance is not sufficient to mitigate the overvoltages at both the bus and capacitor bank. The inrush current oscillates at a low frequency. However, this mitigation method reduces the Mvar generated by the shunt capacitor banks. For example, a 72 Mvar capacitor bank would be de-rated by approximately 6% when a 166 mH series reactor is connected to it. So, the decrease in the Mvar should be considered when applying the 6% reactor.

The inrush current waveform is shown in Fig. 16; here, the inrush frequency oscillates close to the power frequency of the system. In this mitigation method, the capacitance per phase was changed to 3.647 μF. In practice, reactors cannot be added to existing capacitors to make a de-tuned filter because the installed capacitors may not be rated for the additional voltage and/or current caused by the added series reactors. Therefore, to design capacitor that is compatible with 6% reactors, the rated capacitor must be up-sized with respect to Mvar. This results in a significant improvement in the design and performance of 230 kV shunt capacitor banks because the 6% reactor prevents future problems related to harmonic transients.

To verify this method, an impedance scan was performed. In this study, the series connection of an inductor and a capacitor will result in a very low impedance in a certain frequency range, which is close to the series resonance frequency. The parallel connection of an inductor and a capacitor will result in a very high impedance in a certain frequency range, which is close to the parallel resonance frequency. Figure 17 shows that the switching of capacitor banks with a series current-limiting reactor (1 mH) can cause

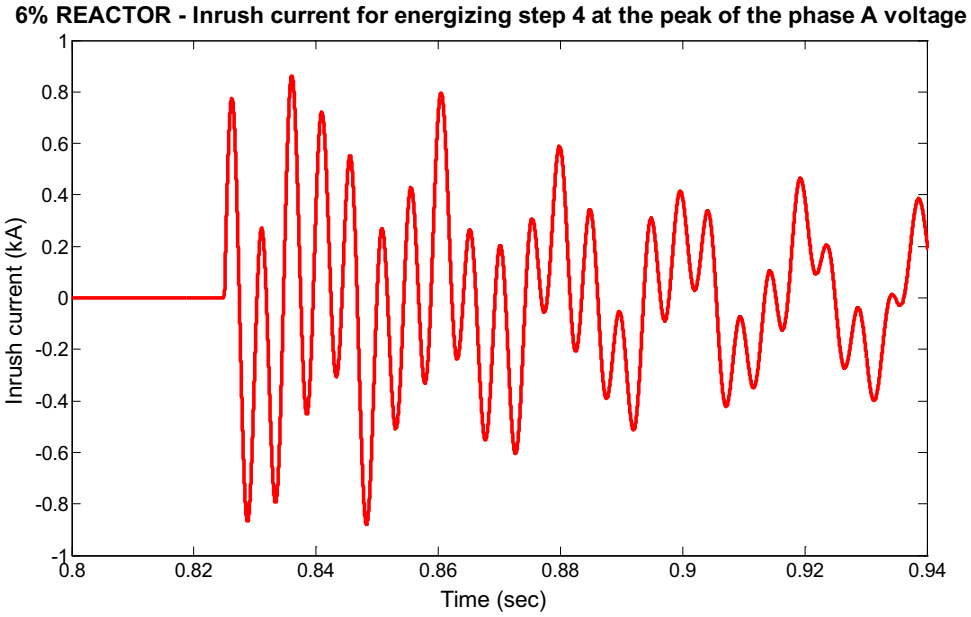


Fig. 16 Inrush current for energizing step 4 at the peak of the phase A system voltage, I_{peak} (phase A) = 879 A

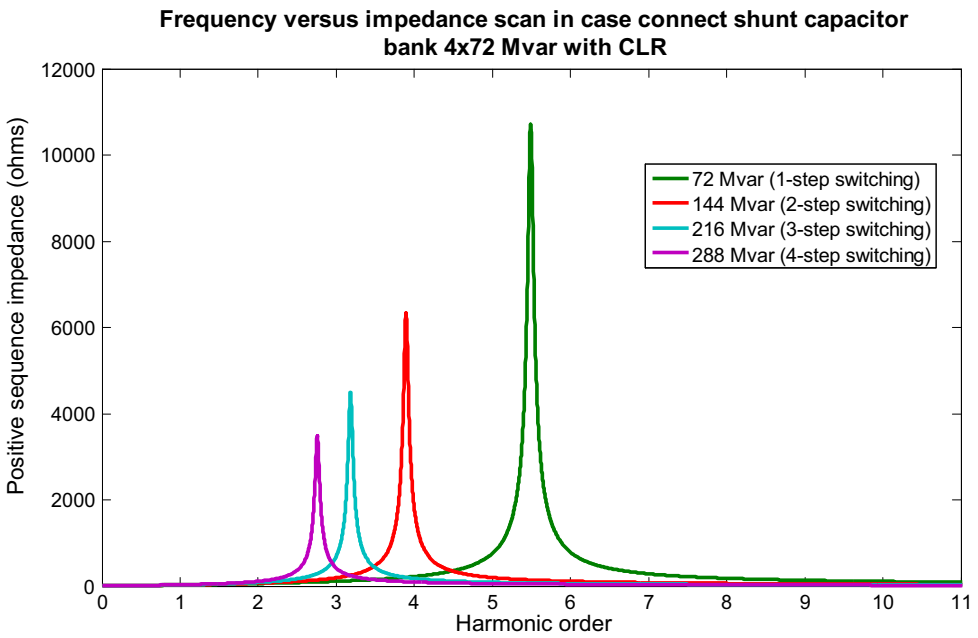


Fig. 17 Frequency versus impedance scans at the bus when switching the shunt capacitor bank with the current-limiting reactor (1 mH)

a parallel resonance problem. A high impedance occurs at about the third order when the capacitor bank is switched in four steps. The harmonic distortions are close to the parallel resonance frequency. In this situation, the harmonic current can be amplified. Higher-order harmonic currents are reduced because the capacitors have low impedance at these frequencies. On the other hand, other transient mitigation techniques give similar impedance scan results compared with this method.

To prevent the parallel resonance problem and the shortening of life of the capacitor unit, a shunt capacitor bank with a series 6% reactor was applied. An impedance scan indicates a series resonance phenomenon, as shown in Fig. 18. The series 6% reactor and capacitor provide a series resonance at approximately the 4.08th order. The high impedance occurs around the second order when the capacitor bank is switched in four steps. So, the overvoltage that occurs from the harmonic distortions is reduced due to the decreased impedance

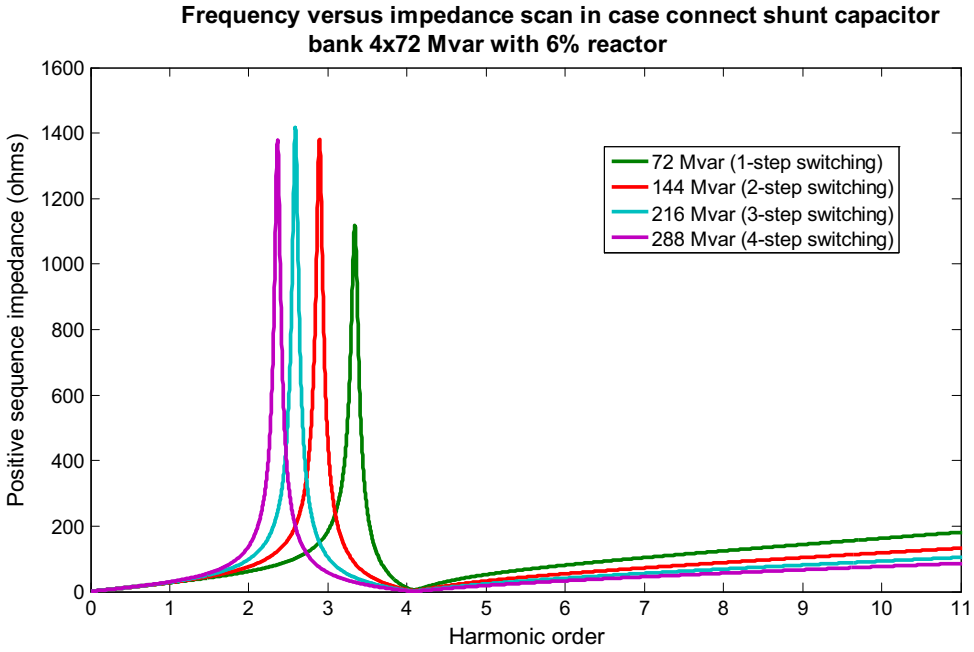


Fig. 18 Frequency versus impedance scans at the bus when switching the shunt capacitor bank with the 6% reactor (166 mH) to prevent the parallel resonance problem

at the third order. In this situation, the harmonic distortions on a system are reduced.

5.6 Simulation using synchronous closing control

This technique reduces the magnitude of transient inrush currents depending on the point on the wave of the voltage prior to pre-strike between contacts. A simple way to reduce the transients is to close the circuit breaker contact at a zero voltage across the circuit breaker [14]. The three-pole operation of the circuit breaker is applied here. This switching device requires that each pole of the circuit breaker be independently controlled, as in a three-phase system. The zero crossing in each phase will be displaced by 120° degrees. So, an electronic module can be fitted on the breakers to stagger the opening of the three different poles of the breaker.

In Table 6 and Fig. 19, the peak inrush current is reduced more than in other mitigation methods. The frequency of the inrush current is very similar to the power frequency. The peak of transient inrush current and oscillation overvoltage were nearly same in each step. The transient inrush current would be reduced to a minimum when compared with another transient mitigation methods. Addition, their peak values of inrush current and overvoltage were close to the steady-state results. The bus voltage is normal (there is no occurrence of transient oscillation overvoltage). This is because synchronous control does not provide a large inductance for damping the transients. Figure 20 shows the result of the voltage waveform when the three-pole operated circuit breaker with mechanical staggering has been chosen to control the closing time in the individual poles. The positive phase sequences L1, L2 and L3 should be connected to the phase-pole connections C1, B1 and A1, respectively [5]. For the sequence of the three phases, it should be noted that the zero current occurs at approximately every 60 electrical degrees or 3.35 ms. This study indicates that a closing consistency of 0.02–0.05 ms provides the best overvoltage control, which is comparable to that of a properly sized PIR and the 6% reactor.

Table 6 Peak inrush current, event frequency and highest bus overvoltage with synchronous closing control

Step	Synchronous closing control			
	PSCAD/EMTDC			
	$i_{i,\text{peak}}$ (kA)	$f_{i,1}$ (kHz)	$f_{i,2}$ (kHz)	Voltage BUS (kV)
1	0.604	1.458	0.289	229.839
2	0.517	22.727	0.212	222.350
3	0.459	21.277	0.463	214.724
4	0.458	21.739	0.749	222.931

However, it is not easy to accomplish closing near a zero voltage. The transient inrush currents and overvoltages will increase if the timing calibration drifts. Therefore, it is difficult to achieve the level of precision required. As shown in Figs. 21 and 22, when the timing error in closing the circuit breaker is varied both positively and negatively from 0 to 3 ms, the high inrush current and oscillation overvoltage are increased when the timing error is high. The simulations show that the inrush current and oscillation overvoltage have acceptable values. If the timing error in closing the switching device for the capacitor bank has a closing consistency

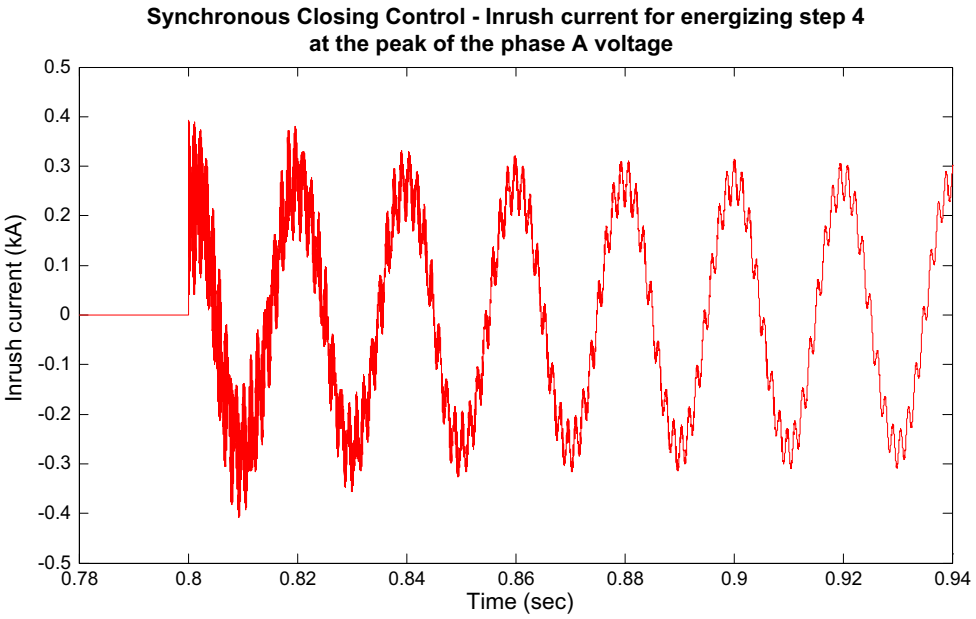


Fig. 19 Inrush current for energizing step 4 at the peak of the phase A system voltage, I_{peak} (phase A) = 458 A

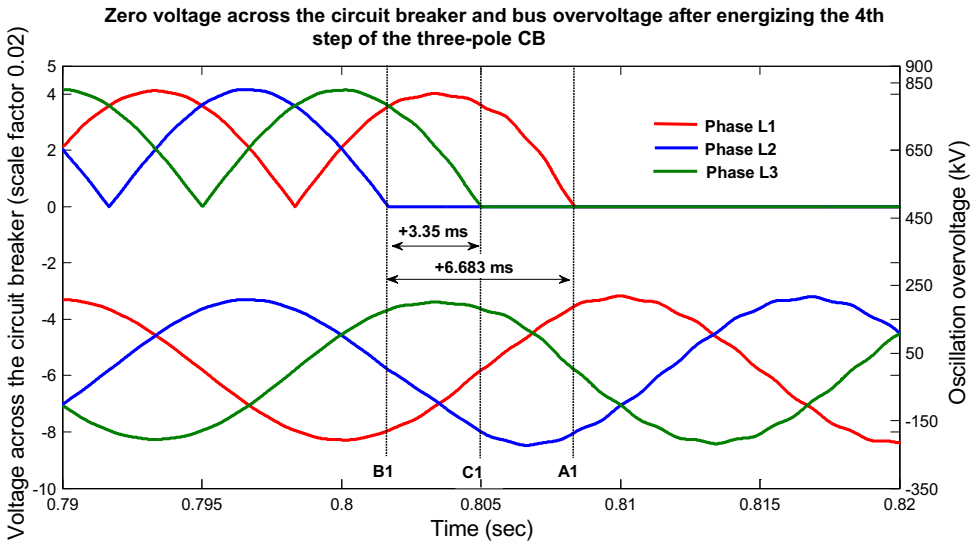


Fig. 20 Zero voltage across the circuit breaker and bus overvoltage after energizing the fourth step of the three-pole CB

within ±0.5 ms, this mitigation method requires precise timing closing and control of the three individual poles of the circuit breaker. In the electric network system and capacitor bank, the designer must analyse the situation and tailor the switching device accordingly.

5.7 Variation of system short-circuit current

The switching shunt capacitor bank of 4 × 72 Mvar, 230 kV with a 1 mH current-limiting reactor is considered in this case by varying the impedance of the short-circuit system to change the fault current. The short-circuit current is changed to 5, 10, 20, 30 and 40 kA to investigate the effect of the source impedance on the peak inrush current and transient oscillation overvoltage.

Figures 23, 24 and Table 7 show the dependence of n the peak inrush current, the peak phase-to-phase oscillation overvoltage and the transient frequency, respectively, on the available short-circuit current. The highest short-circuit current at 40 kA provides the lowest driving point impedance, which leads to the highest magnitude of the inrush current. Meanwhile, the relative minimum of the phase-to-phase oscillation overvoltage occurs at an available fault current of approximately 40 kA. This is because for the high short-circuit current of 40 kA, the frequency of the second transient event is close to a fundamental frequency, and the first transient event for the short-circuit current of 20 kA occurs

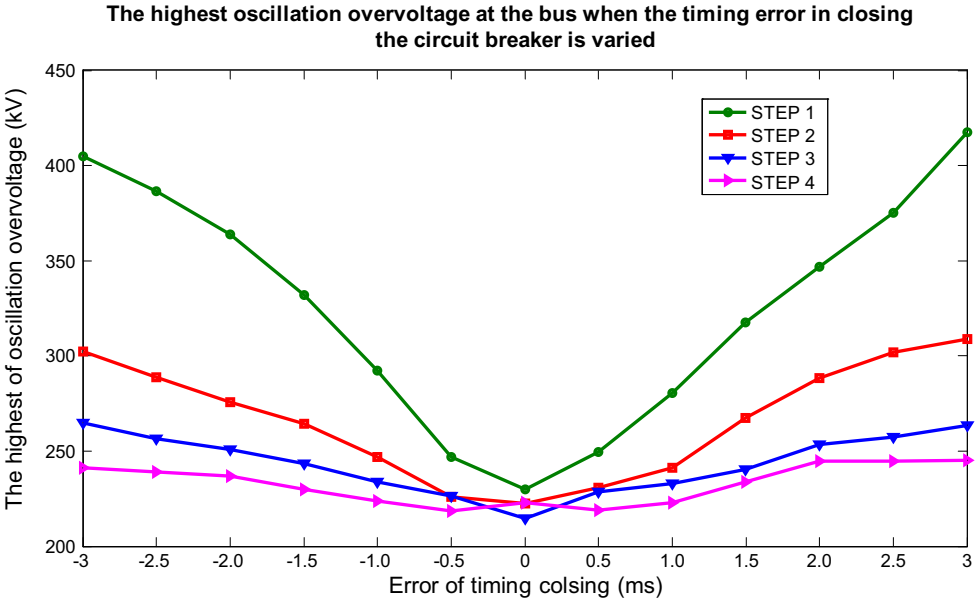


Fig. 21 The highest oscillation overvoltage at the bus when the timing error in closing the circuit breaker is varied

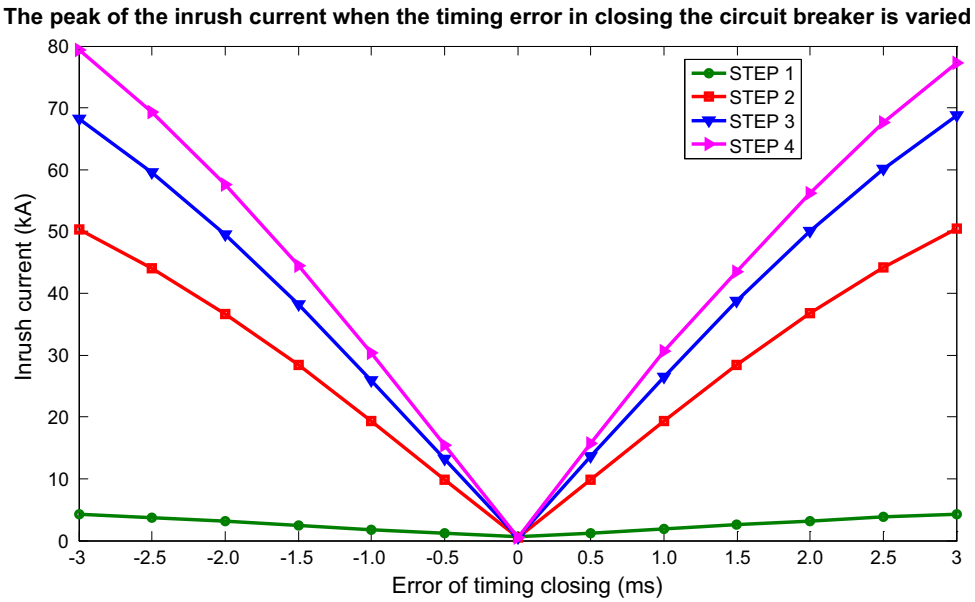


Fig. 22 Peak of the inrush current when the timing error in closing the circuit breaker is varied

faster than that of 40 kA. In this case, the instantaneous capacitor voltage energization of a capacitor bank results in an immediate drop in the system voltage, followed by a fast voltage recovery and finally an oscillating transient voltage that is superimposed on the fundamental waveform [8]. A low short-circuit power may result in a significant increase in the overvoltage [55]. The same phenomena can be observed in [56]. When the short-circuit capacity of the source is relatively low compared to the size of a capacitor bank, energizing the capacitor bank causes the most dramatic disturbances [14].

5.8 Variation of capacitor bank sizing

We will now consider the effect of capacitor bank sizing by investigating the peak inrush current and oscillation overvoltage. In Figs. 25 and 26, the simulation results indicated that the peak inrush current is very high when switching is performed with the higher-rated capacitor banks. A small capacitor bank results in a minimum oscillation overvoltage. Therefore, the transient capacitor switching can be reduced by dividing the capacitor bank into smaller bank sizes.

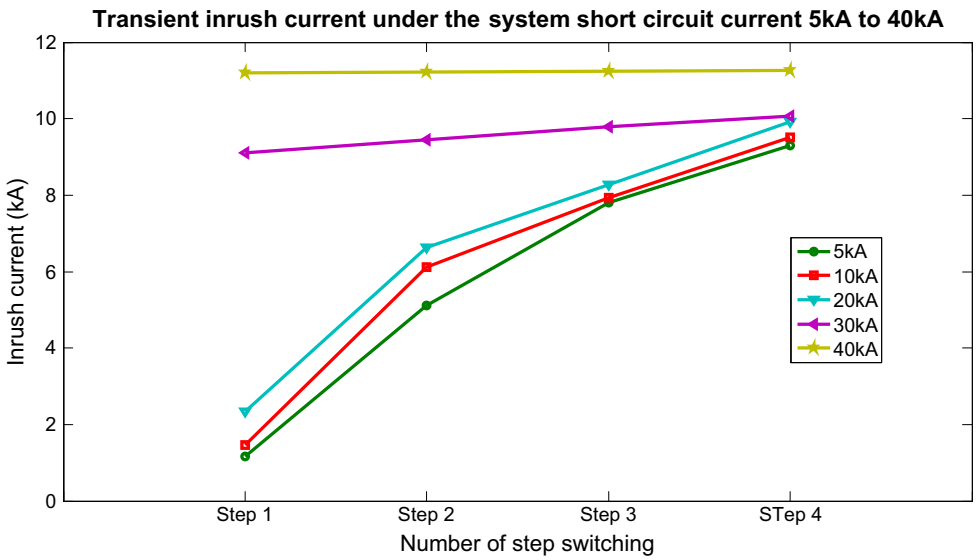


Fig. 23 Transient inrush current when the short-circuit current of the system is varied from 5 to 40 kA

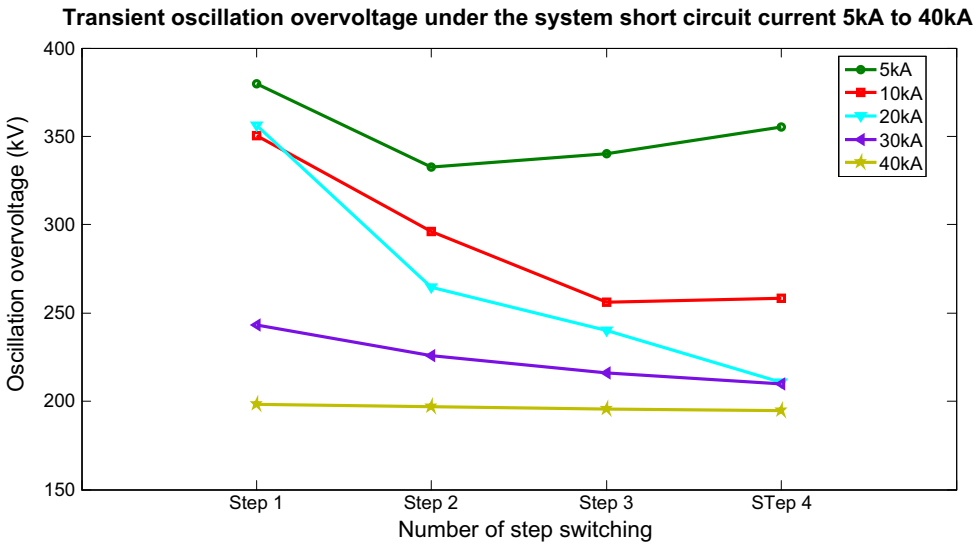


Fig. 24 Transient oscillation overvoltage at the bus when the short-circuit current of the system is varied from 5 to 40 kA

Table 7 Event frequency for each short-circuit current

Step	Short-circuit current 20 kA		Short-circuit current 40 kA	
	$f_{i,1}$ (kHz)	$f_{i,2}$ (Hz)	$f_{i,1}$ (kHz)	$f_{i,2}$ (Hz)
1	2.488	–	2.481	–
2	2.506	359.841	2.493	48.523
3	2.512	275.938	2.497	39.065
4	2.518	248.508	2.515	38.021

6 Results and discussion

During the switching of shunt capacitor banks, high magnitude and high-frequency transients can occur. The PSCAD/EMTDC was employed to evaluate and analyse the peak inrush current and the highest transient oscillation overvoltage when a 230 kV shunt capacitor bank in a substation system is energized; the analysis includes the conventional calculation of inrush currents and frequencies. The calculation method is based on published standards. Moreover, different cases for mitigating the transients were studied to find the optimal methods or techniques that can be used for limiting the transients. This paper presents the technique of using a series 6% reactor to limit the high transient inrush current and oscillation overvoltage for back-to-back switching of the shunt capacitor bank in the large HV substation system. The transient simulations are investigated in six different cases, including the base case, energization with a pre-inserted resistor, energization with a pre-inserted inductor, the use of a current-limiting reactor, the use of a 6% reactor and synchronous closing control, for mitigating the inrush current and oscillation overvoltage by either conventional calculations or simulations (conventional calculations cannot be used in the case of PII, PIR and synchronous switching).

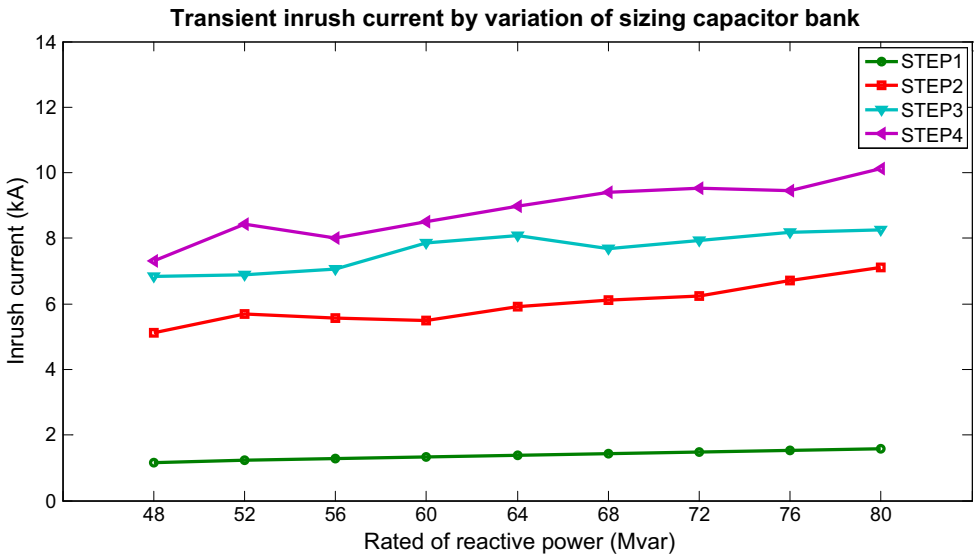


Fig. 25 Relation between transient inrush current and rated of reactive power at the bus

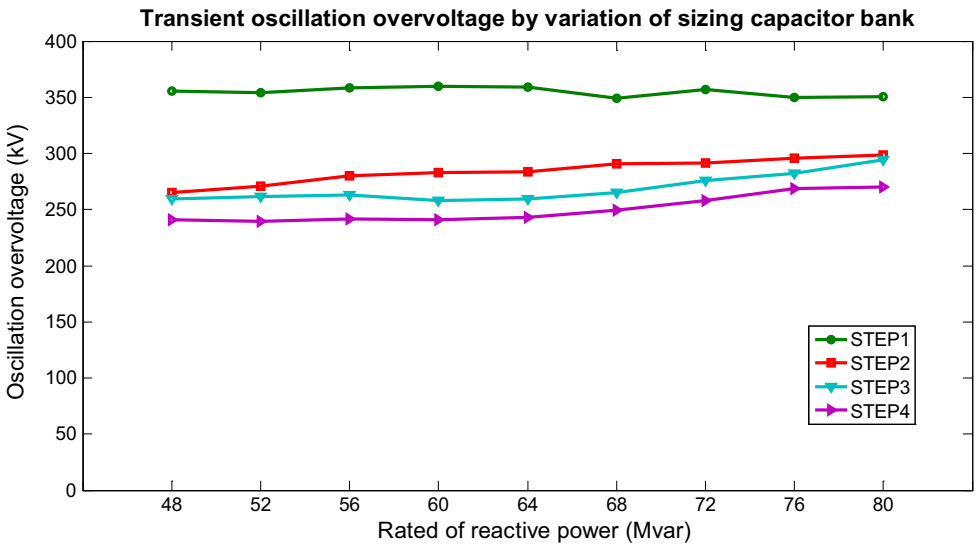


Fig. 26 Relation between transient oscillation overvoltage and rated of reactive power at the bus

From the simulation results, the mitigation methods presented successfully reduce the transient inrush current and oscillation overvoltage. However, the synchronous closing control technique reduces the inrush current and oscillation overvoltage better than the other methods, as listed in Tables 8 and 9, and Figs. 27 and 28. The series 6% reactor is an effective and economical approach to limit high transient inrush currents and overvoltages and to prevent harmonic amplification due to resonance issues. In addition, the 6% reactor is effective in limiting the outrush current (as the capacitor bank can feed from the capacitor to a fault point). The 6% reactor can limit the outrush current in this situation. Therefore, the application of 6% reactor can be used in harmonic pollution, which is an industrial application where other existing techniques cannot be implemented.

In Tables 8 and 9, the simulation results for limiting the high transient inrush current and oscillation overvoltage are described below.

1. The pre-insertion resistor (PIR) used an 86 ohm resistance to damp the inrush current and overvoltage during the energizing of the capacitor bank. This method effectively limits the inrush current when compared with the base case. However, the inrush current and overvoltage still remain high when compared with other techniques.
2. The pre-insertion inductor (PII) used a 119 mH inductor to damp the switching transients. The results show a successful limitation of the inrush current. However, the overvoltage at the last step still remains high. The oscillation overvoltage may be higher than those in other techniques. This method cannot control the oscil-

Table 8 Summary of peak transient inrush currents

Mitigation method	Peak inrush current (kA)			
	Step 1	Step 2	Step 3	Step 4
Base case	1.476	49.584	64.470	74.488
Pre-insertion resistors	0.851	8.582	11.613	12.714
Pre-insertion inductors	0.366	8.378	9.042	9.634
Current-limiting reactor	1.470	6.241	7.931	9.517
6% Reactor	0.967	0.898	0.812	0.879
Synchronous closing control	0.604	0.517	0.459	0.458

Table 9 Summary of highest bus oscillation overvoltage

Mitigation method	Highest oscillation overvoltage (kV)			
	Step 1	Step 2	Step 3	Step 4
Base case	353.516	296.023	259.736	263.598
Pre-insertion resistors	240.191	235.160	236.054	257.648
Pre-insertion inductors	256.289	261.862	269.647	299.968
Current-limiting reactor	357.111	291.217	276.086	258.226
6% Reactor	237.663	226.596	243.094	242.589
Synchronous closing control	229.839	222.350	214.724	222.931

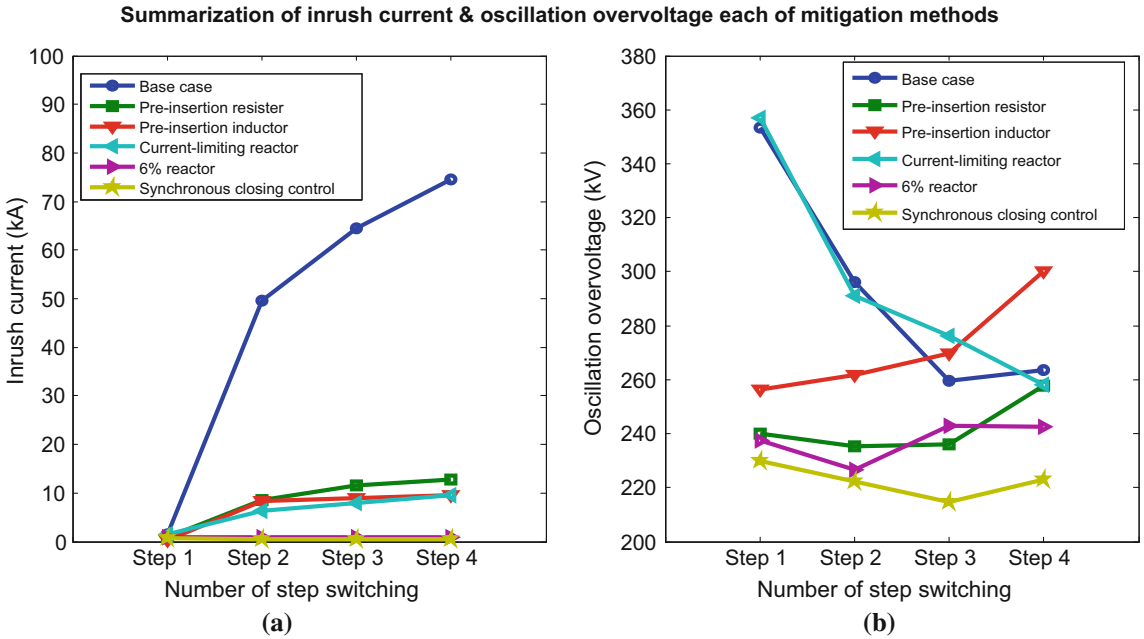


Fig. 27 Summary of each mitigation method for reducing the switching transients in capacitor banks. **a** Peak of transient inrush current. **b** Highest oscillation overvoltage

lation overvoltage when many steps switching are used. The voltages that appear at the capacitor terminal are increased in this situation.

3. The current-limiting reactor (CLR) method used a 1 mH reactor to damp the switching transients. This method slightly reduces the oscillation overvoltage at the bus. Meanwhile, the high inrush current is successfully reduced. The reduction in the inrush current is lower than that for the base case, and the cases where the pre-insertion inductor and resistor are used. The voltages that appear at the capacitor terminal are increased in this situation.
4. The series 6% reactor method used a 166 mH reactor to limit the high inrush current and oscillation overvoltage. This method effectively reduces the inrush current and overvoltage at the bus. The peak inrush current and oscil-

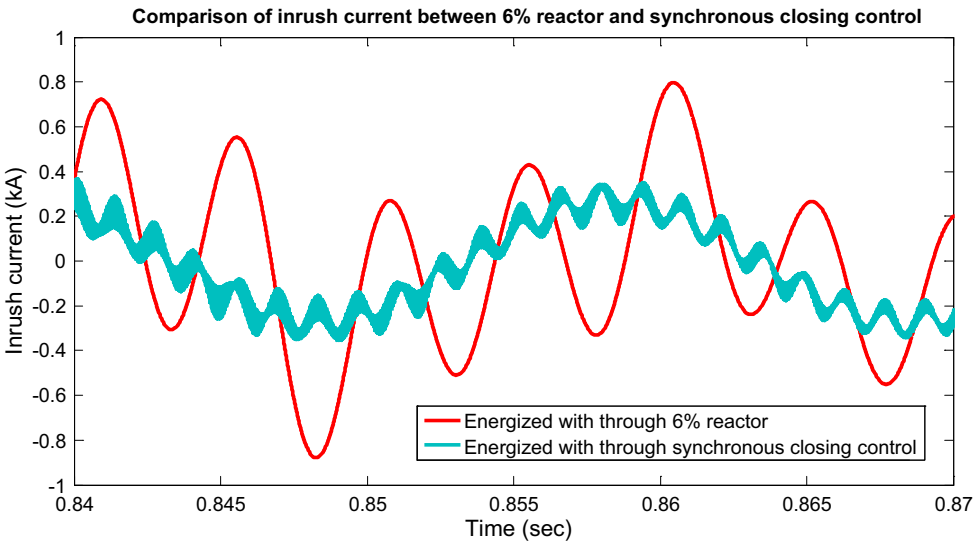


Fig. 28 Comparison of inrush current reduction between 6% reactor and synchronous closing control techniques

lation overvoltage are lower than those obtained for the base case, and the pre-insertion inductor, pre-insertion resistor and current-limiting reactor methods. However, the voltage and current that appear at the capacitor terminal are increased in this situation.

5. The synchronous closing control is the best solution to limit both the high inrush current and oscillation overvoltage. The peak inrush current and oscillation overvoltage are lower than those in other techniques. However, this method requires precise accuracy in timing for closing of the circuit breaker. The circuit breaker is switched at a zero voltage. The timing error for closing the breaker should be within ± 0.5 ms. If the timing error of a circuit breaker is over the limit, the inrush current and overvoltage become too high, and the circuit breaker and capacitor risk damage are due to insulation failure.
6. The synchronous closing control method is the best solution to limit the high inrush current. The order for the effectiveness of the remaining solutions is as follows: the 6% reactor, the current-limiting reactor, the pre-insertion inductor and the pre-insertion resistor techniques, respectively. There is a slight difference in the magnitude of the inrush current from the synchronous closing control and 6% reactor methods.
7. The synchronous closing control method is the best solution to limit the oscillation overvoltage. The second most effective method is the 6% reactor method and the third is the pre-insertion resistor method. On the other hand, the current-limiting reactor and pre-insertion inductor techniques only reduce the overvoltage a little.

Figure 29 shows the summary of transient inrush current and oscillation overvoltage waveforms by comparing between the base case and the pre-insertion resistor, current-limiting reactor, 6% reactor and synchronous closing control methods after the fourth switching step was performed in the system. The results show that the synchronous closing control method can reduce the inrush current and oscillation overvoltage better than other methods. Here, the application of synchronous closing control provides the ideal component to mitigate the effects of back-to-back capacitor switching. However, in the case of the three-pole circuit breaker operation, a specific mechanism (staggering) must be built in. These transients will increase if the timing calibration drifts; therefore, the level of precision required for timing control is difficult to achieve.

Figure 30 shows a comparison of the transient inrush current waveforms obtained from transient reduction with the current-limiting reactor and the base case; energizing the shunt capacitor bank is performed in four steps. As observed in Fig. 30a, the base case (no transient reduction) shows a peak of inrush current that is much higher than that for the current-limiting reactor method. Moreover, the frequency of the inrush current from the base case is very high compared with that from the current-limiting reactor method. This situation occurred because the loop inductance between each step is very low for the base case (there is no series reactor to damp the high inrush current and overvoltage). The transient inrush current was reduced in each step when the current-limiting reactor was connected in series. The sizing variation for the current-limiting reactor is shown in Fig. 30b. The results indicate that the magnitude of the inrush current is reduced when the rating of the current-limiting reactor is increased. The peak inrush current is inversely proportional to the inductance value of the current-limiting reactor. In addition, the frequency of the inrush current is very low when the inductance is large. The frequency of the inrush current is inversely proportional to the rated inductance of the current-limiting reactor.

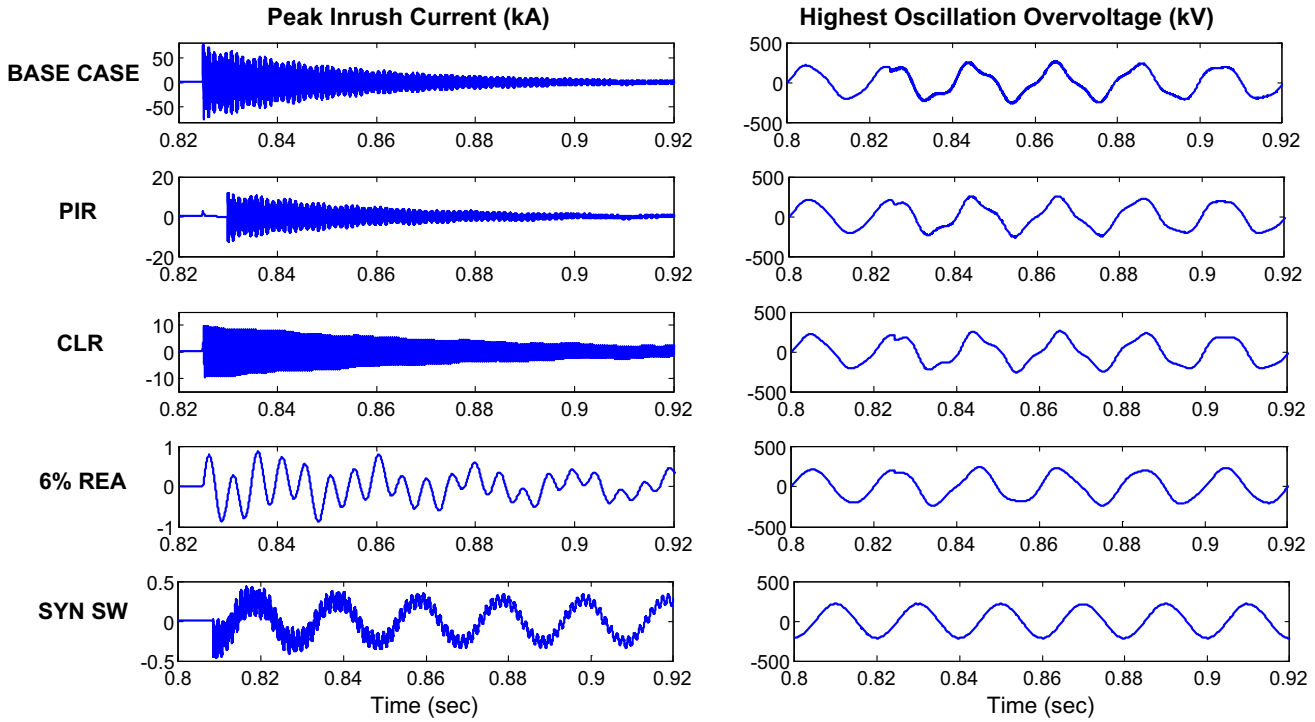
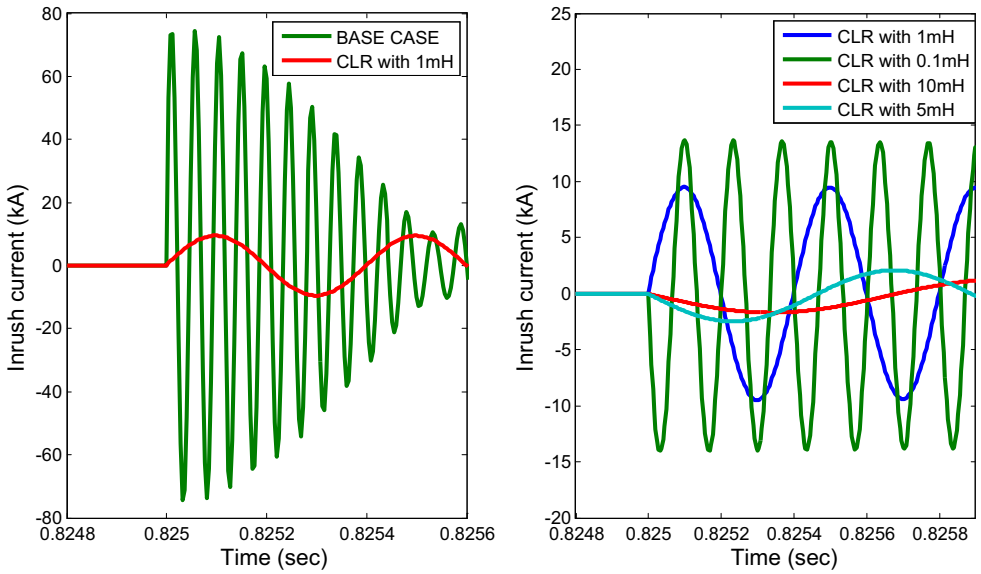


Fig. 29 Comparison of transient inrush current and oscillation overvoltage reduction between base cases, pre-insertion resistor, current-limiting reactor, 6% reactor and synchronous closing control methods when four switching steps are performed in the system

Fig. 30 Relationship between the size of the current-limiting reactor and the transient inrush currents. The existing 230 kV shunt capacitor bank in the Thailand substation system with a series current-limiting reactor is studied



Moreover, the circuit parameters that affect the magnitude and characteristics of the transients, such as the source strength, the switching device and the inductance loop between the banks should be considered. A reduction in the source strength will result in a more severe transient. If the short circuit is very low and the size of a capacitor bank is small, the transient inrush current that is generated by back-to-back capacitor bank switching is the most optimal. Therefore, the utility and/or user, the increased cost and the added complexity of the equipment should all be taken into consideration to evaluate a switching device and determine the mitigation method used to reduce the transient oscillation overvoltage and inrush current. The evaluation would determine the reliability, the capability for a high number of operations and the cost-effectiveness.

Practically, the network system of each substation is different; therefore, a designer must investigate and consider the specific situation to determine the method selected to

mitigate these transients, especially in resistive devices that can add losses to the circuit while reducing the voltage and current transients. The pre-insertion resistors and inductors have to be specially designed for capacitor bank applications; if the system parameters are changed, the inductor and resistor for both methods need to be re-designed. The use of the current-limiting reactor is the most popular method for reducing the transient stresses. Alternatively, if a system has high harmonic pollution, the use of a 6% reactor will be preferred to other techniques. Therefore, each of these transient control methods has various advantages and disadvantages in relation to the transient inrush current and overvoltage reduction, cost, installation requirements, operating/maintenance requirements and reliability. The designer must therefore consider these factors and make decisions to achieve the optimal technique required to limit transients when capacitor bank energizes the reactive power in network systems.

7 Conclusions

This paper presents a technique to limiting inrush current and oscillation overvoltage when switching large shunt capacitor banks in an HV substation system using a 6% series reactor. Comparisons have been provided between the proposed method and various mitigation techniques that are currently used, such as pre-insertion resistors (PIRs), pre-insertion inductors (PIIs), current-limiting reactor (CLRs) and synchronous closing control. The proposed technique and past methodologies have been applied and simulated using the PSCAD/EMTP program for an HV substation that is modelled after part of the Thailand substation system. From the simulation results, the synchronous closing control yields the best result for reducing the inrush current and oscillation overvoltage compared to the proposed methodology using the 6% series reactor. The application of synchronous closing control in the simulations is an ideal way to mitigate the effects of back-to-back switching. However, it is difficult to achieve precision in the actual operation and mechanism of circuit breaker, and the transient level will increase if timing is inaccurately controlled. The 6% series reactor is also advantageous in preventing harmonic amplifications due to resonance issues, especially in industrial applications with harmonic pollution. Thus, the proposed methodology can be used by substation systems as a solution to transient problems caused by energization of capacitor banks.

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References

1. (2010) IEEE guide for application of shunt power capacitors. IEEE Standard 1036-2010
2. Hooshmand RA, Mohkami H (2011) New optimal placement of capacitors and dispersed generators using bacterial foraging oriented by particle swarm optimization algorithm in distribution systems. Electr Eng 93(1):43–53
3. Injeti SK, Thunuguntla VK, Shareef M (2015) Optimal allocation of capacitor banks in radial distribution systems for minimization of real power loss and maximization of network savings using bio-inspired optimization algorithms. Int J Electr Power Energy Syst 69:441–455
4. Sarkar P, Baral A, Das K (Bhatacharya), Syam P (2016) An ant colony system based control of shunt capacitor banks for bulk electricity consumers. Appl Soft Comput 43:520–534. ISSN 1568-4946
5. Softić M, Tokić A, Uglešić I (2012) 7th Vienna international conference on mathematical modelling measurement, modeling and simulation of capacitor bank switching transients, IFAC proceedings volumes, Volume 45, Issue 2, 2012, pp 1254–1259
6. Bhargava B, Khan AH, Imece Ali F, DiPietro J (1993) Effectiveness of pre-insertion inductors for mitigating remote overvoltages due to shunt capacitor energization. IEEE Trans Power Deliv 8:1226–1238
7. Seyedi H, Golabi S, Abam Z (2010) Limitation of transmission line switching overvoltages. In: IEEE international conference on power and energy (PECon), pp 363–368
8. Peggs JF, Powell PW, Grebe TE (1994) Innovations for protection and control of high voltage capacitor banks on the Virginia power system. In: Proceedings of the 1994 IEEE power engineering society transmission and distribution conference, pp 284–290
9. Stroica P (2000) Modern methods for synchronous switching of the Romanian power system circuit breakers in 400 kV substation. In: 10th Mediterranean electrotechnical conference, MEleCon 2000, vol 3, pp 949–953
10. Zhang Q, Yuan H, Liu Y, Wang Q (2010) The operating transient process analysis and synchronous switching strategies research of vacuum breaker. In: Fourth international conference on genetic and evolutionary computing, pp 142–145
11. Amer AHA (2004) Transient over voltages in electric distribution networks due to switching of capacitor banks steps. In: International conference on electrical, electronic and computer engineering (ICEEC2004), pp 872–875
12. Das JC (2005) Analysis and control of large-shunt-capacitor-bank switching transients. IEEE Trans Ind Appl 41(6):1444–1451
13. Blooming TM, Carnovale DJ (2008) Capacitor application issues. IEEE Trans Ind Appl 44(4):1013–1026
14. Cipeigan L, Chindris M, Rull J, Rusu A, Sumper A, Ramirez R, Alves R (2006) Mitigation of capacitor bank energization harmonic transients. In: IEEE/PES transmission & distribution conference and exposition: Latin America, pp 1–5
15. Sadeghi M, Babaei E, Rabetian M, Nahalparvari H (2011) Mitigation of capacitor banks switching transients considering injected harmonics. In: Iranian conference on electrical engineering (ICEE), pp 1–5
16. Shunt Capacitors for A.C. Power Systems Having a Rated Voltage above 1000 V—Part 1: General, IEC Standard 60871-1, (Jul. 2005)
17. Srithorn P, Khojulklang K, Kulworawanichpong T (2004) Capacitor switching control using a decision table for a 115-kV power transmission system in Thailand. In: Knowledge-based intelligent information and engineering systems, Lecture Notes in Computer Science, vol 3213, pp 1262–1268

18. Alferov DF, Ahmetgareev MR, Budovskii AI, Evsin DV, Ivanov VP, Dermenzhi PG (2010) Hybrid switch with controlled switching for circuits with capacitor banks. Russ Electr Eng 81(3):152–158
19. Preethi B, Sumangala BV (2014) Voltage stabilization through reactive power injection at secondary terminals of distribution level feeders—using thyristor-switched capacitor. In: Emerging research in electronics, computer science and technology, Lecture Notes in Electrical Engineering, vol 248, Springer India. doi:10.1007/978-81-322-1157-0_56
20. Long X, Liu X, Song D (2016) Analysis of the choice of a serial reactor in a parallel capacitor device. In: Proceedings of the 5th international conference on electrical engineering and automatic control, Volume 367 of the series Lecture Notes in Electrical Engineering, pp 385–391
21. Yin W (2012) Transient analysis and time selection of capacitor switched device of reactive power compensation. In: Electrical, information engineering and mechatronics 2011, Lecture Notes in Electrical Engineering, vol 138, pp 1019–1024. doi:10.1007/978-1-4471-2467-2_120
22. Yuan T, Yu Q, Wu Z (2012) Design and implementation of the improved control algorithm for switching capacitor banks. Adv Electr Eng Autom 139:407–413
23. Ghanbari T, Farjah E, Naseri F (2016) Three-phase resistive capacitor switching transient limiter for mitigating power capacitor switching transients. In: IET generation, transmission & distribution, vol 10, pp 142–153. IET. ISSN :1751-8687
24. Upadhyay C, Chandwani H (2014) Modelling of switching effects & its mitigation techniques on MV—capacitor bank with VCB. In: Power and energy systems conference: towards sustainable energy (pp 1–5). IEEE
25. Taherzadeh M, Rostaminia R, Joorabian M, Saniei M (2013) Mitigation of capacitor bank switching transients by using SVCs in large plants instead of capacitor bank and circuit breaker. In: Power electronics, drive systems and technologies conference (PEDSTC), 2013 4th (pp 321–327). IEEE
26. Ghanbari T, Farjah E, Zandnia A (2013) Solid-state transient limiter for capacitor bank switching transients. In: IET generation, transmission & distribution, vol 7, pp 1272–1277. IET
27. Tseng S-T, Chen J-F (2010) A novel method for mitigating the capacitor switching-on transients. In: Universities power engineering conference (AUPEC), 2010 20th Australasian (pp 1–5). IEEE
28. Athanasiadis N (2002) A new technique for a static var compensator using the EMTP modeling environment. Electr Eng 84:85–89
29. Ozdemir A (2006) A reactive power control relay design with a new approach. Electr Eng 88:133–140
30. Karaki SH, Kayssi AI, Karaki HS (2005) Capacitor placement for switching noise reduction using genetic algorithms and distributed computing. Electr Eng 2005(87):11–18
31. Kamarposhti MA, Lesani H (2011) Effects of STATCOM, TCSC, SSSC and UPFC on static voltage stability. Electr Eng 2011(93):33–42
32. Karpagam N, Devaraj D, Subbaraj P (2010) Improved fuzzy logic controller for SVC in power system damping using global signals. Electr Eng 2010(91):395–404
33. Zdravković Z, Vukelja P, Mrvic J (2006) Insulation co-ordination for continuous operating voltages and temporary overvoltages. Electr Eng 2006(88):441–446
34. Ketabi A, Sadeghkhani I, Feuillet R (2013) Network switching and voltage evaluation during power system restoration. Electr Eng 2013(95):241–253
35. Han B-M, Kim H-J, Baek S-T (2004) New soft-switching current source converter for photovoltaic power system. Electr Eng 2004(86):285–291
36. Batura R, Opydo W (2005) Overvoltages caused by switching unloaded cable lines by a vacuum switch. Electr Eng 2005(87):181–189
37. Gitizadeh M, Khalilnezhad H, Hedayatzadeh R (2013) TCSC allocation in power systems considering switching loss using MOABC algorithm. Electr Eng 2013(95):73–85
38. Rahmani R, Othman MF, Shojaei AA, Yusof R (2014) Static VAR compensator using recurrent neural network. Electr Eng 2014(96):109–119
39. Asadi M, Jalilian A (2013) Using an active resistive damper in hybrid active power filter to avoid resonance over-voltage. Electr Eng 2013(95):301–313
40. Menti A, Zacharias T, Milias-Argitis J (2009) Optimal sizing and limitations of passive filters in the presence of background harmonic distortion. Electr Eng 2009(91):89–100
41. Gitizadeh M, Kalantar M (2009) Genetic algorithm-based fuzzy multi-objective approach to congestion management using FACTS devices. Electr Eng 2009(90):539–549
42. Aredes M, Portela C, van Emmerik EL, da Silva Dias RF (2004) Static series compensators applied to very long distance transmission lines. Electr Eng 86:69–76
43. (2005) IEEE application guide for capacitance current switching for AC high-voltage circuit breaker. IEEE Standard C37.012-2005
44. (2006) IEEE guide for the protection of shunt capacitor banks. IEEE Standard C37.99-2000 (R2006)
45. (2010) Switching and transmission line diagram. Electricity generation authorization Thailand (EGAT)
46. Beanland M, Speas T, Rostron J (2004) Pre-insertion resistors in high voltage capacitor bank switching. In: Western protective relay conference (pp 1–12)
47. Iizarry-Silvestrini MF, Vélez-Sepúlveda TE (2006) Mitigation of back-to-back capacitor switching transients on distribution circuits. Department of Electrical and Computer Engineering, University of Puerto Rico
48. Bellei TA, O'Leary RP, Camm EH (1996) Evaluating capacitor-switching devices for preventing nuisance tripping of adjustable-speed drives due to voltage magnification. IEEE Trans Power Deliv 11(3):1373–1378
49. (1997) Industrial A.C. networks affected by harmonics—application of filters and shunt capacitors. IEC Standard 61642
50. Alexander RW (1985) Synchronous closing control for shunt capacitors. IEEE Trans Power Appar Syst PAS–104(9):2619–2626
51. Faria da Silva F, Bak CL, Guomundsdóttir US, Wiechowski W, Knardrupgård MR (2009) Use of a pre-insertion resistor to minimize zero-missing phenomenon and switching overvoltages. In: IEEE power & energy society general meeting (PES' 09), pp 1–7
52. Manitoba HVDC Research Centre (2003) EMTDC: transient analysis for PSCAD power system simulation. Manitoba HVDC Research Centre Inc., Manitoba, Canada
53. Greenwood A (1991) Electrical transients in power systems, 2nd edn. Wiley, New York
54. (2009) IEEE standard for AC high-voltage circuit breakers rated on a symmetrical current basis—preferred ratings and related required capabilities for voltages above 1000 V. IEEE Standard C37.06-2009
55. Sabot A, Morin C, Guillaume C, Pons A (1993) A unique multipurpose damping circuit for shunt capacitor bank switching. IEEE Trans Power Deliv 8(3):1173–1183
56. O' Leary RP, Harner RH (1988) Evaluation of methods for controlling the overvoltages produced by the energization of a shunt capacitor bank. In: International conference on large high voltage electric systems (pp 1–12)