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Design and analysis of a single-phase low-frequency active power factor correction circuit: a symmetric trapezoidal current waveform approach

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Abstract This paper focuses on the design and analysis of the single-phase Low-Frequency Active Power Factor Correction (LFAPFC) circuit. The LFAPFC circuit has several attractive features such as low electromagnetic interference, low switching frequency and ease of implementation when compared with the High-Frequency Active Power Factor Correction circuit. Moreover, its performance is much better than that of the Passive Power Factor Correction circuit. However, few of the previous studies focus on determining the values of major parameters of the LFAPFC circuit and their corresponding performance. To conduct an in-depth study on the LFAPFC circuit, this paper proposes a systematic design method based on analyzing the characteristics of a symmetric trapezoidal current waveform. Using the proposed method, output performance indices such as total harmonics distortion and power factor of the LFAPFC circuit can be estimated. In addition, the relationship among the output performance, inductance and conduction parameters of the power switch is derived and investigated. Using the proposed method, designers can determine suitable values of conduction parameters and inductance for specific applications. Computer simulations and real experiments are carried out to verify the effectiveness of the proposed method.

Keywords Power factor · Total harmonic distortion · Power factor correction · Active power factor correction circuit

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1 Introduction

For modern power electronic devices such as power supplies, adaptors, electronic ballasts and motor drives, a full-bridge rectifier is commonly required. Conventional approaches use bulky electrolytic filtering capacitors in the rectifier to reduce voltage ripple. However, they result in a very low power factor (around 0.5–0.7) and cause serious harmonic pollution. Since 1990, the International Electric Committee (IEC) has issued a regulation on the line current harmonic emission in its IEC 1000-3-2 for personal computers, lighting equipment, portable tools, balanced three-phase equipment, etc. [1]. To meet the IEC regulation, a common approach is to employ a Power Factor Correction (PFC) circuit in power electronic devices to force the input current waveform to faithfully follow the sinusoidal input voltage waveform so that the Total Harmonics Distortion (THD) is nearly zero and the Power Factor (PF) is close to one [2].

In general, PFC circuits can be divided into two main categories-passive and active. With attractive features such as continuous input current waveform as well as smaller inductance, active PFC circuits such as boost converters with high switching frequency strategies have been commonly adopted in various power electronic appliances designed to achieve high PF and low THD [3-5]. However, the use of high switching frequency carriers leads to several drawbacks such as Electromagnetic Interference (EMI) issues and significant switching losses. To overcome these drawbacks, many approaches employ soft-switching techniques and additional electromagnetic interference filters. However, this will increase cost as well as the complexity of the circuit design. It is not surprising that the Passive Power Factor Correction (PPFC) circuit is still commonly used in many applications [6–14]. In general, the PPFC circuit consisting of low-frequency inductors and capacitors is designed to sup-

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press the high-order harmonics of the input current so that PF and THD can be improved and also comply with the IEC regulations. Although the PPFC circuit is simple and easy to implement, it has several drawbacks. For example, it consists of bulky passive components and its performance may deteriorate if the input voltage or load conditions are changed.

In addition to the PPFC circuit and the High-Frequency Active PFC (HFAPFC) circuit, the Low-Frequency Active PFC (LFAPFC) circuit [15, 16] can be viewed as a trade-off between the PPFC circuit and the HFAPFC circuit. Compared with the conventional PPFC circuit, the LFAPFC circuit has higher PF and smaller THD. Although its performance is not as good as that of the HFAPFC circuit, the LFAPFC circuit is cheaper and can also comply with the harmonic limit regulations [17–21]. In fact, in many applications the LFAPFC circuit has been used as an alternative to the HFAPFC circuit. However, in most existing literature, proper inductance and switching strategies of the LFAPFC circuit are determined by either trial and error or through computer simulations, with both approaches typically being inefficient and difficult to comprehend. To facilitate the design of the LFAPFC circuit, this paper proposes a new design method that is based on a symmetric trapezoidal current waveform. Using the proposed method, major performance indices such as PF and THD can be estimated. In particular, the proposed method simplifies the procedures for determining proper inductance and conduction parameters based on input conditions and output performance requirements. Several experiments have been conducted to verify the effectiveness of the proposed approaches. Experimental results indicate that the proposed approach for designing the LFAPFC circuit based on the symmetric trapezoidal current waveform is indeed feasible.

The remainder of the paper is organized as follows. Section 2 addresses the principle of the LFAPFC circuit. The proposed approach for designing the LFAPFC circuit based on the symmetric trapezoidal current waveform is introduced in Sect. 3. Experimental results and conclusions are given in Sects. 4 and 5, respectively.

2 Principle of low-frequency active power factor correction circuit

Figure 1 illustrates the circuit topology and typical waveforms of the LFAPFC circuit. The key issues in designing the LFAPFC circuit are choosing a proper inductor and determining the switching timing and conducting duration of the power switch for each half cycle of the input voltage, so that the input current waveform can be reshaped to comply with the regulations/standards. However, the analytical relationship among the input voltage, input power, PF, THD, conduction parameters of the power switch and inductance has yet to be thoroughly explored. Furthermore, in most of the existing approaches, the design parameters are determined by either trial and error or through computer simulations [15–21]. As previously mentioned, these approaches are usually inefficient, time-consuming and not easy to comprehend. To cope with this problem, this paper is aimed at developing a simple and systematic approach for determining suitable values of conduction parameters and inductance for specific applications.

2.1 Circuit analysis

According to the conducting status of the power switch and the input current of the rectifier, the operation of the LFAPFC circuit can be divided into four modes for each half cycle as illustrated in Fig. 1b. Without loss of generality, only the half cycle for which V_{in} is positive is analyzed in the following. In such a case, $i_{in}(t)$ is greater than zero in Mode 3. In the following derivation, it is assumed that the output voltage is fixed in the steady-state operation and all the circuit elements are ideal. In Fig. 1a, $v_{in}(t)$ is the input voltage, $i_{in}(t)$ is the input current, v_0 is the output voltage, and v_L is the voltage drop across the inductor. In Fig. 1b, $T_d = t_1$ is the delay time of the power switch, and $T_{on} = t_2 - t_1$ is the conduction time of the power switch. In addition, the frequency of the input voltage is denoted as ω_L .

Mode 1 and Mode 4 $(0 \le t < t_1; t_3 \le t < \frac{T}{2})$

In Mode 1 and Mode 4, the power switch Q is turned off. Both the inductor voltage $v_L(t)$ and input current $i_{in}(t)$ are zero.

$$v_L(t) = 0 \tag{1}$$

$$i_{\rm in}(t) = 0 \tag{2}$$

Mode 2 $(t_1 \le t < t_2)$

In Mode 2, the input voltage is smaller than the output voltage, i.e., $v_{in}(t) < v_o$. To increase the conduction angle of the input current of the conventional rectifier, the power switch Q is turned on, while the inductor is used for energy storage in this mode. The formulas of the inductor voltage $v_L(t)$ and input current $i_{in}(t)$ are described by (3) and (4), where the peak value and the Root Mean Square (RMS) value of the input voltage are denoted as V_{in_rms} , respectively.

$$v_L(t) = v_{\rm in}(t) = \sqrt{2} \cdot V_{\rm in_rms} \cdot |\sin(\omega_L t)|$$
(3)

$$i_{\rm in}(t) = \frac{v_{\rm in}PK}{\omega_L L} (\cos(\omega_L t_1) - \cos(\omega_L t))$$
(4)

Mode 3 $(t_2 \le t < t_3)$

In Mode 3, power switch Q is turned off. However, the inductor current is not equal to zero. The energy stored in





the inductor is released through the diode in this mode. The inductor voltage $v_L(t)$ and input current $i_{in}(t)$ are described by (5) and (6), respectively.

$$v_L(t) = v_{\rm in}(t) - v_o = \sqrt{2} \cdot V_{\rm in_rms} \cdot |\sin(\omega_L t)| - v_o \qquad (5)$$

$$i_{in}(t) = \frac{V_{in_PK}}{\omega_L L} (\cos(\omega_L t_1) - \cos(\omega_L t)) - \frac{v_o}{L} (t - t_2) \quad (6)$$

Equations (4) and (6) indicate that the input current depends on the conduction status of the power switch and the inductance, i.e., t_1 , t_2 , t_3 and L.

2.2 Output voltage and power factor

From (6), if $t = t_3$ and $i_{in}(t) = 0$, the output voltage v_o can be described by

$$v_o = \frac{V_{\text{in}_\text{pk}} \cdot (\cos(\omega_L t_1) - \cos(\omega_L t_3))}{\omega_L (t_3 - t_2)} \tag{7}$$

Equation (7) indicates that the output voltage is a function of t_1 , t_2 and t_3 . Note that the design parameters t_1 and t_2 are related to the conduction duration, while t_3 is related to the load conditions, namely the value of v_o depends on conduction status and load conditions.

Based on (2), (4) and (6), the RMS value of the input current can be determined using

$$I_{\text{in,rms}} = \sqrt{\frac{1}{T} \int_{0}^{T} i_{\text{in}}^{2}(t) \cdot dt} = \sqrt{\frac{\frac{V_{in_{-}PK}^{2}}{\pi \cdot \omega_{L} \cdot L^{2}} \left\{ \cos^{2}(\omega_{L}t_{1}) \cdot (t_{3} - t_{1}) - \frac{2 \cdot \cos(\omega_{L}t_{1}) \cdot [\sin(\omega_{L}t_{3}) - \sin(\omega_{L}t_{1})]}{\omega_{L}} + \frac{t_{3} - t_{1}}{2} + \frac{[\sin(2\omega_{L}t_{3}) - \sin(2\omega_{L}t_{1})]}{4 \cdot \omega_{L}} \right\}}{\sqrt{-\frac{\omega_{L} \cdot V_{o}^{2}}{\pi \cdot L^{2}} \cdot \left(\frac{t_{3}^{3}}{3} - t_{2}t_{3}^{2} + t_{2}^{2}t_{3} - \frac{t_{3}^{3}}{3}\right)}}$$
(8)

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Based on the relationship $v_{in}(t) = V_{in_PK} \cdot \sin(\omega_L t)$ and Eqs. (2), (4), (6), one can calculate the input power using

$$P_{\rm in} = \frac{1}{T} \int_0^T v_{\rm in}(t) \cdot i_{\rm in}(t) dt$$

$$= \frac{V_{\rm in_PK}^2}{\pi \cdot \omega_L \cdot L} \cdot \left[\frac{1}{2} + \frac{\cos(2\omega_L t_1) + \cos(2\omega_L t_3)}{4} - \cos(\omega_L t_1) \cdot \cos(\omega_L t_3) \right]$$

$$- \frac{V_{\rm in_PK} \cdot V_o}{\pi \cdot L} \left[\cos(\omega_L t_3) \cdot (t_2 - t_3) + \frac{\sin(\omega_L t_3) - \sin(\omega_L t_2)}{\omega_L} \right]$$
(9)

According to the obtained $I_{in,rms}$ and P_{in} , the power factor can be estimated by (10).

$$PF = \frac{P_{\rm in}}{V_{\rm in_rms} \cdot I_{\rm in_rms}} \tag{10}$$

Compared with the conventional PPFC circuit design, the computations of $I_{in,rms}$ and P_{in} are much more complex and involve many parameters (e.g., t_1, t_2, t_3, L). Moreover, the equation used to describe the relationship between conduction parameters and inductance is highly non-linear. All these factors contribute to the fact that the entire design procedure of the LFAPFC circuit is complex, time consuming and difficult to comprehend. It is conceivable that in most existing approaches, the values of conduction parameters and the inductance are usually determined by trial and error.



Fig. 3 THD under different load conditions of the LFAPFC circuit

3 Design of the LFAPFC circuit based on symmetric trapezoidal current waveform

3.1 Analysis based on symmetric trapezoidal current waveform

As mentioned previously, most of the existing approaches still rely on a trial and error approach to select a proper inductor and the corresponding conduction parameters (T_d and T_{on}) of the LFAPFC circuit. One of the major reasons why it is difficult to determine the circuit parameters is that the input current waveform of the LFAPFC circuit as shown in Fig. 1b is highly non-linear and asymmetric over a halfcycle. Suppose that the RMS value of the input voltage is 110 V, 60 Hz and the ripple of the output voltage is less than 5%. Figures 2, 3, 4 show the simulation results of the input current waveforms, THD, and PF of the input current under different load conditions, respectively. The values of major parameters used in the simulation are listed as follows: $T_d = 0.46$ ms; $T_{on} = 1.85$ ms; L = 38.8 mH; output capacitor $C = 1800 \,\mu$ F. The results shown in Figs. 2, 3, 4 reveal that if the input current waveform is closer to a symmetric trapezoid, the THD will be small and the PF will be high. Moreover, the inductance and the conduction parameters of the LFAPFC circuit can be determined analytically according to the desired regulation, as will be shown in the next section.

It is observed that when an LFAPFC circuit is well designed, as shown in Fig. 5, the waveform of the input current $i_{in}(t)$ is very similar to a symmetric trapezoid. In the following analysis, $i_{in}(t)$ is considered to consist of two parts as described by (11).

$$i_{\rm in}(t) = i_T(t) + i_{\rm inT}(t)$$
 (11)

where $i_T(t)$ is the desired current waveform which can be determined according to the regulations, and $i_{inT}(t)$ is the difference between $i_{in}(t)$ and $i_T(t)$. Figure 6 illustrates the typical waveforms of $i_{in}(t)$, $i_T(t)$ and $i_{inT}(t)$. According to



Fig. 4 PF under different load conditions of the LFAPFC circuit

Fig. 6, $i_{inT}(t)$ can be viewed as an odd symmetric current waveform centered at $\left(\frac{2nT-T}{4}, 0\right)$ for $\frac{nT-T}{2} \le t \le \frac{nT}{2}$ (where *n* is the cycle number, and $n \in N$). Moreover, if there is only a slight difference between $i_{in}(t)$ and $i_T(t)$, the average power produced by the input voltage $v_{in}(t)$ and $i_{inT}(t)$ is very small and thus can be neglected, that is, the input power P_{in} can be expressed as:



Fig. 6 Typical waveforms of $v_{in}(t)$, $i_{in}(t)$, $i_T(t)$, and $i_{inT}(t)$ of the LFAPFC circuit







$$m = T \int_{0}^{T} \int_{0}^{T} v_{in}(t) dt = T \int_{0}^{T} v_{in}(t) dt$$

$$\approx \frac{1}{T} \int_{0}^{T} v_{in}(t) \cdot i_{T}(t) dt \qquad (12)$$

According to (12) and Fig. 6, we have come up with the following observations:

- 1. To simplify calculation, $i_T(t)$ rather than $i_{in}(t)$ is used to compute the input power P_{in} without sacrificing too much accuracy.
- 2. When an LFAPFC circuit is well designed, the fluctuation of the waveform of $i_{inT}(t)$ can be neglected.

For simplification, the time variable t is replaced by the electrical angle θ in the following derivations.

As shown in Fig. 7, $\theta = \omega_L \cdot t$, $\theta_1 = \omega_L \cdot t_1$, $\theta_2 = \omega_L \cdot t_1$ $t_2, \theta_d = \omega_L \cdot T_d = \theta_1, \theta_{on} = \omega_L \cdot T_{on} = \theta_2 - \theta_1, \theta_3 =$ $\omega_L \cdot t_3$. Since $I_{T-PK} = i_{in}(t_2)$, for $0 \le \theta \le \pi$, $i_T(\theta)$ can be expressed as:

$$i_{T}(\theta) = \begin{cases} 0, & 0 \leq \theta \leq \theta_{1} \text{ and } \theta_{3} \leq \theta \leq \pi \\ \frac{I_{T_PK}}{\theta_{2}-\theta_{1}}(\theta-\theta_{1}), & \theta_{1} \leq \theta \leq \theta_{2} \\ I_{T_PK}, & \theta_{2} \leq \theta \leq \pi-\theta_{2} \\ \frac{I_{T_PK}}{\theta_{1}-\theta_{2}}(\theta-\theta_{3}), & \pi-\theta_{2} \leq \theta \leq \theta_{3} \end{cases}$$

$$(13)$$

According to (4), (12) and (13), the input power P_{in} can be rewritten as:

$$P_{in} = \frac{2 \cdot V_{in_PK} \cdot I_{T_PK} \cdot (\sin(\theta_2) - \sin(\theta_1))}{\pi \cdot (\theta_2 - \theta_1)}$$
$$= \frac{2 \cdot V_{in_PK}^2 \cdot (\cos(\theta_1) - \cos(\theta_2)) \cdot (\sin(\theta_2) - \sin(\theta_1))}{\pi \cdot (\theta_2 - \theta_1) \cdot \omega_L \cdot L}$$
(14)

It is clear to see that (14) is much simpler than (9). Since the THD of the symmetric trapezoidal waveform can be accurately estimated, the conduction parameters θ_d and θ_{on} can be determined according to the regulations. In other words, the drawbacks resulting from using the trial and error approach can be avoided. After the values of the conduction parameters of the power switch are decided, the desired inductance can then be determined using (14). Figure 8 shows the relationship between the inductance and the conduction parameters, where the input voltage is set to $110 V_{rms}$ and the input power is set to 746 W. One can also find that, with a fixed θ_d , as the value of θ_{on} increases, the inductance required to suppress the increasing rate of the input current during the conduction period increases as well. In contrast, when θ_d increases, the maximum inductance decreases.

According to (7) and assuming $\theta_3 = \pi - \theta_1$, the output voltage V_o can be rewritten as:

$$V_o = \frac{2 \cdot V_{\text{in}_PK} \cdot \cos(\theta_1)}{\pi - \theta_1 - \theta_2}$$
(15)

When $t_1 = t_2$, the output voltage can be further simplified as:

$$V_o = \frac{2 \cdot V_{\text{in}_{PK}} \cdot \cos(\theta_2)}{\pi - 2 \cdot \theta_2}$$
(16)





3.2 Performance evaluation and error analysis

In most existing literature, the PF and THD of the LFAPFC circuit are difficult to estimate even when the conduction parameters and inductance are given. Nevertheless, as shown in Fig. 6, the THD obtained using the symmetric trapezoidal current waveform can give a good estimation of the actual THD of the input current, namely designers can easily determine the desired switching conditions to meet the regulations. However, the magnitude of $i_{inT}(t)$ may exhibit significant fluctuation under different switching strategies. IsSpice simulation results of the THD obtained using the symmetric trapezoidal current waveform and the actual THD of the input current under different operation conditions are depicted in Fig. 9. Based on the results shown in Figs. 8 and 9, we have come up with the following observations.

- 1. As the value of θ_d increases, the value of θ_{on} that yields the smallest THD of the symmetric trapezoidal current waveform will decrease, while the resulting THD will increase.
- 2. When the value of θ_d is fixed, the output voltage increases as the value of θ_{on} increases. The reason is that as θ_{on} getting larger, the desired inductance defined by (14) becomes larger as well. As a result, the energy stored in the inductor increases and so does the output voltage.

3.3 Comparison with passive LC circuits

The above discussions provide insights about the systematic design for the LFAPFC circuit. Designers can firstly determine the desired current waveform according to the IEC regulations, and then find a suitable inductor. One interesting observation is that (14) actually suggests an alternative design approach-to determine the inductance firstly, and subsequently choose proper conduction parameters based on (14). For the purpose of comparison, constant multiples of the inductance used in the passive LC circuit is employed in 263



Fig. 9 Comparison curves between the THD obtained using the symmetric trapezoidal current waveform and the actual THD of the input current. **a** $\theta_d = 0^\circ$, **b** $\theta_d = 5^\circ$, **c** $\theta_d = 10^\circ$, **d** $\theta_d = 15^\circ$



Fig. 10 Comparison of various orders of harmonics of the PPFC circuit and different LFAPFC circuits obtained from IsSpice simulation. **a** 1st harmonics to 11th harmonics. **b** 13th harmonics to 39th harmonics

the design of LFAPFC circuits, while the conduction parameters are determined using (14). In this paper, (17) is used to determine the inductance of the passive LC circuit developed in [11], where L_{ON} represents the reference inductance. The selection of L_{ON} depends on the volume of the inductor and the THD of the input current. Usually, if the value of L_{ON} is set between 0.014 and 0.027 H, lower THD and higher PF can be obtained. In this paper, the value of L_{ON} is set to 0.022 H.

$$L = L_{\rm ON} \frac{V_{\rm rms}}{I_{\rm rms} \cdot f_{\rm line}}$$
(17)

In addition, (18) can be used to estimate the volume of the inductor, where K_L depends on the cross-section-window-area product given by (19) [22]. In (19), B_{max} is the maximum flux density, k_R is the window-filling coefficient, and J is the desired current density.

$$K_L = L \cdot I_{\rm Lrms} \cdot I_{\rm Lpk} \tag{18}$$

$$A_e \cdot A_w = \left(\frac{L \cdot I_{\text{Lpk}}}{N \cdot B_{\text{max}}}\right) \left(\frac{N \cdot I_{Lrms}}{k_R \cdot J}\right) = \frac{K_L}{k_R \cdot J \cdot B_{\text{max}}} (19)$$

When the desired inductance is determined, the proper values of conduction parameters θ_d and θ_{on} can be determined using (14).

In summary, the proposed symmetric trapezoidal current waveform approach provides two different design strategies. The elaboration of these two design strategies is given in the following. It is assumed that the input voltage and input power are constant and the efficiency is 1.

First design strategy The designers can firstly determine the conduction parameters θ_d and θ_{on} according to the IEC regulations on harmonics, and then find a suitable inductor. Suppose that the design requirement is that the power factor is larger than a prescribed value, say 95%, and $i_{inT}(t)$ is very small—so much so that it can be neglected. One can exploit the desired current waveform $i_T(\theta)$ described by (13) to calculate THD so as to determine the proper values of θ_d and θ_{on} . After the values of θ_d and θ_{on} are determined, the inductance L can be obtained using (14).

Second design strategy The volume of the inductor is taken into account. After determining the inductance using (17) and (18) [11,22], one can calculate the values of conduction parameters θ_d and θ_{on} based on (14). Moreover, through computer simulation, one can determine the values of θ_d and θ_{on} that yield the best power factor.

In general, there is a trade-off between the volume of the inductor and power factor (i.e., IEC regulation) in a practical design procedure. To have a fair comparison, the LFAPFC circuits designed using the aforementioned design strategies will be compared with a PPFC circuit. In particular, for the

Table 1 Values of various orders of harmonics of the PPFC circuit and different LFAPFC circuits obtained from IsSpice simulation

Harmonics	IEC-1000-3-2 Class A (A)	PPFC: $L = 6 \mathrm{mH} (\mathrm{A})$	$LFAPFC$ $L = 6 \mathrm{mH} (\mathrm{A})$	LFAPFC $L = 12 \mathrm{mH} (\mathrm{A})$	LFAPFC $L = 24 \mathrm{mH} (\mathrm{A})$
1	10	8.15417256	6.94483734	6.96605375	6.97312588
3	2.3	3.57142857	1.07496464	0.63649222	0.072843
5	1.14	0.68599717	1.42857143	0.75884017	0.54526167
7	0.77	0.44766619	0.65770863	0.58203678	0.27369165
9	0.4	0.2758133	0.28288543	0.20509194	0.00707214
11	0.33	0.15346535	0.41937765	0.04773692	0.11032532
13	0.21	0.11951909	0.24328147	0.12137907	0.07694484
15	0.15	0.09335219	0.0990099	0.076471	0.00260255
17	0.132	0.06577086	0.15063649	0.01800566	0.045686
19	0.118	0.05374823	0.08769448	0.05190948	0.03536068
21	0.107	0.04596888	0.01909477	0.04596888	0.00143564
23	0.098	0.03536068	0.05162659	0.0106082	0.02475248
25	0.090	0.02970297	0.01626591	0.02220651	0.02008487
27	0.083	0.02652051	0.03182461	0.0311174	0.00095474
29	0.078	0.02192362	0.04031117	0.01746818	0.01541726
31	0.073	0.01838755	0.00169731	0.00551627	0.01287129
33	0.068	0.01697313	0.03536068	0.0151768	0.00070721
35	0.064	0.01485149	0.03677511	0.01145686	0.01048091
37	0.061	0.01272984	0.01768034	0.00304102	0.00884724
39	0.058	0.01131542	0.02333805	0.011173974	0.00056577



Fig. 11 Waveforms of the input current, voltage and PWM signal under different inductances. **a** L = 6 mH, $\theta_d = 25^\circ$, $\theta_{on} = 14^\circ$. **b** L = 12 mH, $\theta_d = 10^\circ$, $\theta_{on} = 32^\circ$. **c** L = 24 mH, $\theta_d = 5^\circ$, $\theta_{on} = 60^\circ$

 Table 2
 Simulation results of the LFAPFC circuit and the passive LC

 PFC circuit
 PFC circuit

	Р	A1	A2	A3
<i>L</i> (mH)	6	6	12	24
THD (%)	45.5	27	16.4	8.62
PF	0.77	0.957	0.98	0.98
CF	1.839	1.603	1.44	1.389
K_L (mJ)	849	485	822.7	1587

P Passive LC, A1-A3: LFAPFC circuit with different inductances

purpose of comparison, the inductances used in the design of LFAPFC circuits will be constant multiples (e.g., one time, two times and four times) of the inductance of the PPFC circuit. The following is an illustrative design example.

Suppose that the input voltage is 110 V_{rms} and input power is 746 W. The desired inductance of the PPFC circuit calculated using (17) and (18) is 6 mH. As a result, the

inductances used in the design of LFAPFC circuits will be 6, 12 and 24 mH. In addition, several prescribed values of θ_d are also given. With these given inductances and θ_d , the values of corresponding θ_{on} can be determined using (14). Performance indices such as THD, volume of the inductor and PF of the PPFC circuit and that of the proposed LFAPFC circuit are analyzed and compared using IsSpice. The simulation results of IsSpice indicate that the best conduction parameters for the LFAPFC circuit with 6 mH inductance are: $\theta_d = 25^\circ$, $\theta_{on} = 14^\circ$, THD=27 %; the best conduction parameters for the LFAPFC circuit with 12 mH inductance are: $\theta_d = 10^\circ$, $\theta_{on} = 32^\circ$, THD=16.4 %; the best conduction parameters for the LFAPFC circuit with 24 mH inductance are: $\theta_d = 5^\circ$, $\theta_{on} = 60^\circ$, THD = 8.62 %. Comparisons of various orders of harmonics of the PPFC circuit and different LFAPFC circuits obtained from IsSpice simulation are shown in Fig. 10a, b. Note that the dash blue line in Fig. 10a, b represents the IEC 1000-3-2 CLASS A regulation. In addition, the values of various orders of harmonics of the PPFC

circuit and different LFAPFC circuits obtained from IsSpice simulation are listed in Table 1. From the results shown in Fig. 10a, b and Table 1, it is found that the harmonics of the LFAPFC circuit with 12 mH inductance comply with the IEC 1000-3-2 CLASS A regulations. Its PF is around 98 %.

Figure 11 and Table 2 list the simulation results of the LFAPFC circuit and the passive LC circuit. In particular, Fig. 11 shows that using the proposed switching strategy, the shape of the input current waveform meets the design requirements. Moreover, from the results listed in Table 2,

the volume of the inductor used in the LFAPFC circuit can be effectively reduced when the inductance is the same as that of the passive LC circuit.

4 Experimental results

Several experiments have been conducted to verify the effectiveness of the proposed approach. Figure 12 shows a picture of the prototype developed in this paper, while the load is a





(b)





Fig. 13 Waveforms of input line current under different load conditions of the LFAPFC circuit, $v_{in} = 110 V_{rms}$, L = 46.6 mH, $C = 1800 \,\mu\text{H}$, $T_d = 0.46 \text{ ms}$, $T_{on} = 1.85 \text{ ms}$ a $P_o = 250 \text{ W}$, THD = 13.5 % b $P_o = 175 \text{ W}$, THD = 19.1 %



Fig. 14 THD of input line current under different load conditions of the LFAPFC circuit



Fig. 15 Waveforms of input line current under different load conditions of the passive LC circuit, $v_{in} = 110 V_{rms}$, L = 16.8 mH, $C = 1800 \mu$ H. **a** $P_o = 138$ W. **b** $P_o = 275$ W

direct drive variable-speed washing machine. In this paper, the switching control signals are implemented using the phase shift control IC-TCA785 manufactured by SIEMENS. The TCA785 can detect the zero crossing point of the input voltage so as to generate PWM signals for the gate driver. To protect TCA785 and also suppress noise, the photo coupler TLP250 is used to isolate the control signal and the driving signal. As shown in Fig. 12a (based on datasheet of TCA785), V_{s1} is generated from a circuit that consists of a resistor, a diode, a Zener diode and a capacitor. The value of V_{s1} used in this paper is 15 V. In addition, V_{s2} is provided by an isolated power supply, the value of which used in this paper is 12 V. The boost converter used in the full bridge rectifier is the KBJ1506 (manufactured by Pan Jit International Inc.), while the diode is the UF1606CT made by TRSYS. In addi-



Fig. 16 Waveforms of input line current under different load conditions of the LFAPFC circuit, $v_{in} = 110 V_{rms}$, L = 16.8 mH, $C = 1800 \,\mu\text{H}$, $T_d = 1.157 \,\text{ms}$, $T_{on} = 0.74 \,\text{ms}$. **a** $P_o = 138 \,\text{W}$. **b** $P_o = 275 \,\text{W}$

tion, the N-channel power MOSFET IRF460 manufactured by IR is also used in this paper. Figures 13 and 14 show the experimental results of the LFAPFC circuit under different load conditions. The experimental results agree well with simulation results shown in Figs. 2, 3, 4; i.e., the THD can be reduced as the input current waveform is controlled to be close to a symmetric trapezoid. Figures 15 and 16 show the experimental results of the passive LC circuit and the proposed LFAPFC circuit. The detailed output performances are listed in Tables 3 and 4.

It should be noted that the peak current can be suppressed and the size of the inductor can be effectively reduced with the LFAPFC circuit. Moreover, both theoretical analysis and experimental results suggest that the output performance of the LFAPFC circuit can be well predicted using the proposed method if the load condition is given. It is well known that the complex and costly HFAPFC circuit is suitable for closed loop operation while the low-cost PPFC circuit can also be designed for open loop operation with limited additional components when compared to the PPFC circuit. In addition, it is also possible to design an LFAPFC circuit for closed loop operation if a low-cost microcontroller is used to determine the conduction parameters based on different load conditions and output voltage through a lookup table approach.

5 Conclusions

Although conventional PPFC circuits are still widely used in home appliance and consumer products, they also suffer from drawbacks such as bulky circuitry and the fact that their performance is sensitive to input voltage and load conditions. In contrast, the LFAPFC circuit has several advantages over conventional PPFC circuits. The LFAPFC circuit results in high power factor converters with low THD of the input current. Moreover, the size of the inductor can be significantly reduced. To facilitate the use of the LFAPFC circuit, this paper has conducted a thorough study on the analysis and design of the LFAPFC circuit. The relationship among the conduction parameters, inductance, and load conditions for the LFAPFC circuit can be derived using the proposed method. Moreover, this paper also provides an effective design procedure for selecting the desired inductance and conduction parameters when the input voltage, rated power, and performance requirements are given. Using the proposed method, designers can save considerable time in selecting suitable desired inductance and conduction parameters for the LFAPFC circuit. Considering issues such as cost, complexity, EMI, and implementation, the LFAPFC circuit is a highly competitive alternative to the HFAPFC circuit. In particular, the LFAPFC circuit is suitable for fractional horsepower variable-speed motor drives used in home appliances.

$P_o = 138 \text{ W}$			$P_o = 275 \text{ W}$				
THD (%)	PF	CF	η (%)	THD (%)	PF	CF	η (%)
51.9	0.788	2.02	91.4	35.1	0.777	1.898	89.5
L = 16.8 mH	I			L = 29.8 mJ	H		
THD (%)	PF	CF	η (%)	THD (%)	PF	CF	η (%)
24.5	0.959	1.637	91.6	16.4	0.979	1.479	91
	$ \frac{P_o = 138 \text{ W}}{\text{THD (\%)}} $ $ \frac{L = 16.8 \text{ mF}}{\text{THD (\%)}} $ $ 24.5 $	$P_o = 138 \text{ W}$ THD (%) PF 51.9 0.788 $L = 16.8 \text{ mH}$ THD (%) PF 24.5 0.959	$P_o = 138 \text{ W}$ THD (%) PF CF 51.9 0.788 2.02 $L = 16.8 \text{ mH}$ THD (%) PF CF 24.5 0.959 1.637	$P_o = 138 \text{ W}$ THD (%) PF CF η (%) 51.9 0.788 2.02 91.4 $L = 16.8 \text{ mH}$ THD (%) PF CF η (%) 24.5 0.959 1.637 91.6	$P_o = 138 \text{ W}$ $P_o = 275 \text{ W}$ THD (%) PF CF η (%) THD (%) 51.9 0.788 2.02 91.4 35.1 $L = 16.8 \text{ mH}$ $L = 29.8 \text{ mH}$ THD (%) PF CF η (%) THD (%) PF CF η (%) 24.5 0.959 1.637 91.6 16.4	$P_o = 138 \text{ W}$ $P_o = 275 \text{ W}$ THD (%) PF CF η (%) $\overline{\text{THD}}$ (%) PF 51.9 0.788 2.02 91.4 35.1 0.777 $L = 16.8 \text{ mH}$ $L = 29.8 \text{ mH}$ $L = 29.8 \text{ mH}$ $THD (\%)$ PF 24.5 0.959 1.637 91.6 16.4 0.979	$P_o = 138 \text{ W}$ $P_o = 275 \text{ W}$ THD (%) PF CF η (%) THD (%) PF CF 51.9 0.788 2.02 91.4 35.1 0.777 1.898 $L = 16.8 \text{ mH}$ L = 29.8 mH THD (%) PF CF η (%) $L = 29.8 \text{ mH}$ THD (%) PF CF η (%) THD (%) PF CF 24.5 0.959 1.637 91.6 16.4 0.979 1.479

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