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Current-tunable current-mode RMS detector

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Abstract A new realization of root mean square (RMS) detector comprising two controlled current conveyors, metal-oxide-semiconductor transistors and a single grounded capacitor is presented in this paper, without any external resistors and components matching requirements added. The proposed circuit can be used for measuring the RMS value of periodic, band-limited signals. Inherently, the circuit is well suited for IC implementation. The errors related to signal processing and errors bound were investigated and provided. To verify the theoretical analysis, the circuit PSpice simulations have also been included, showing good agreement with the theory. The maximum power consumption of the converter is ∼4.28 mW, at ±1.25 V supply voltages.

Keywords RMS detector · Controlled current conveyors · MOSFET · Multi-harmonic band-limited signals · Simulation

1 Introduction

Root mean square (RMS) amplitude is a consistent, useful, and standard way to measure and compare dynamic signals of all shapes and sizes. RMS detectors of various designs can be found in many applications in the fields of communication and of measurement systems [1,2]. Mobile communication terminals or handsets have become ubiquitous in modern society, which has led to an insatiable demand on the market for cost reduction and power consumption of the mobile terminal. Monitoring accurately the transmitting power of the mobile terminal helps to optimize power consumption and performance of the wireless network [2]. The power detector is widely used to detect the transmitting power in a power control loop of the mobile terminal to optimize its power consumption or improve the linearity of the power amplifier. It is also applied in a gain control loop to optimize the gain of the mobile terminal in the transmitting or receiving chain. Using an RMS or a peak detector, high-frequency voltages can be estimated by measuring DC output voltages, which alleviates the need for costly high-frequency equipments during testing. Generally, RMS power detection is more useful than peak power detection because RMS power is a consistent and standard way to measure and compare dynamic signals independent of waveform shape [2]. Detectors intended for this purpose need to involve wide bandwidth, high input impedance, low loss, low noise, and are expected to be compact and robust in the presence of process–voltage–temperature variations. High dynamic range and low power consumption are also desirable.

Root mean square detectors based on Joule heating provide good accuracy and wide bandwidth. However, the rather complex packaging requirements do not lead to a low cost solution. Diode detectors based on square law are conventionally employed in communication systems as a form of power measurement because of their favourable high-frequency performance and low cost. However, elaborate compensation techniques are required to make them meet the demands of most applications. Dynamic range and temperature stability also limit their application.

Different methods have been reported for the precision measurement of the RMS value of an AC voltage, such as sampling [3], Monte Carlo [4], and the wavelet transform [5,6]. The implicit RMS converter described in [7–12] has been used for many years. Although many data sheets and textbooks include a mathematical discussion on the operation of these circuits, this type of RMS detector design is

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seen as insufficiently efficient in adequately processing the input multi-harmonic signals. Most of these devices similarly consist of two main parts: a full-wave rectifier (or absolute-value) circuit and a multiplier/divider circuit employing a log–antilog principle. Due to the band width and the slew rate of the full-wave rectifier, the high-frequency performances of these devices are limited to <5 MHz. Design techniques based on bipolar dynamic trans-linear circuits have been proposed to implement true RMS-to-DC converters [13,14]. Although these scheme require only NPN transistors, their circuits are operated in only one quadrant and employ full-wave rectifier. A new design technique for RMS-to-DC converter that design around a dual trans-linear-based squarer circuit is proposed in [15,16], where the input current can be a two-quadrant current signal. Because the full-wave rectifier is not required by this conversion scheme, the circuit exhibits a wide bandwidth, but limited compared to thermal-based or diode-based detectors (due to input interference) [17].

Second-generation current conveyors (CCIIs), first introduced in [18], are functionally flexible and versatile. The current-mode circuits have been receiving considerable attention due to their potential advantages such as inherently wide bandwidth, higher slew rate, greater linearity, wider dynamic range, simple circuitry, and low power consumption. The CCII is a reported active component, especially suitable for a class of analogue signal processing. However, the CCII-based circuit for measuring RMS value of multi-harmonic voltage signal has not been reported so far [19]. On the other hand, the CCII cannot control the parasitic resistance at x (R_x) port, therefore, when it is used in some circuits, it absolutely requires some external passive components, especially resistors. This makes it inappropriate for IC implementation due to its high chip area requirements, high power dissipation, and lack of electronic controllability. The introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [20]. Also, the use of dual-output current conveyors is found to be useful in the derivation of current-mode single input circuits [21–23].

The features of the proposed circuit are as follows: the circuit description is very simple; it employs two CCCIIs and single grounded capacitor as passive component, which is suitable for fabrication in monolithic chip, and it makes it suitable for high-frequency operations [24,25]. Unlike the detector described in [42], the one described in this paper involves simpler and more accurate control structure. Additionally, it has fewer active building blocks, the time constant of integrator can be electronically controlled contrary to circuits described in [25,26], and has a wider dynamic range and lower power consumption. Unlike previous works, exact integration on a period is performed instead of estimating the mean value with a low-pass filter. In terms of frequency range, the proposed circuit operation covers a wide range—up to 10 MHz, with increased linearity and precision in determining the effective value. The performance of the proposed circuit, illustrated by PSpice simulations are in good agreement with the calculation.

2 Proposed RMS measuring circuit

The proposed circuit for measuring the RMS value of multi-harmonic, band-limited input signal is shown in Fig. 1. The NMOS transistors (T_1, T_3) and PMOS transistor T_2 have threshold voltage $V_{\mathrm{Tn}} \geq 0$ and $V_{\mathrm{Tp}} \leq 0$, respectively. The y port of the former CCCII is biased at the threshold voltages of the MOS transistors as $V_{\mathrm{B1}} = -V_{\mathrm{Tn}}$ and $V_{\mathrm{B2}} = -V_{\mathrm{Tp}}$. The bulks of all of the PMOS transistors are connected to the source terminals, while the bulks of all of the NMOS transistors are connected to the V_{SS}. This arrangement yields a good performance of the proposed circuit in twin-tube technology implementations, as well as in discrete-component implementations. If N-well CMOS technology is used in the realization of the proposed detector, threshold voltages of the MOS transistors can deviate from their actual nominal value. It is for this reason that we can use techniques proposed for the realization of some other circuits [27–29]. Twin-tube CMOS processes allow independent setting of the well and local substrate doping. In these processes, it is customary to refer to N-well and N-well for the P and N MOSFET bodies, respectively. Generally, both N-wells and N-wells are implanted into the same epitaxial layer (typically a lightly P-doped layer). As a result, all P-wells are still connected so that independent body connections for the NMOS are not allowed. To obtain electrically independent P-wells and N-wells, it is necessary to use more expensive processes, such as SOI or BiCMOS processes. In the latter, buried layers or buried wells are available, so that P-wells can be enclosed in a continuous N-box.

By introducing self-biasing, it is possible to avoid the necessity for external biasing and the entailing requirements for special band-gap bias circuits; since all the internal bias voltages and currents are generated from each other, the bias levels are completely determined by the operating conditions.

The characteristics of the ideal CCCII are represented by the following hybrid matrix:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}. \tag{1}$$

If the CCCII is realized using CMOS technology, R_x can be, respectively, written as:

$$R_x = \sqrt{\frac{1}{k I_{\mathrm{B}}}}. \tag{2}$$

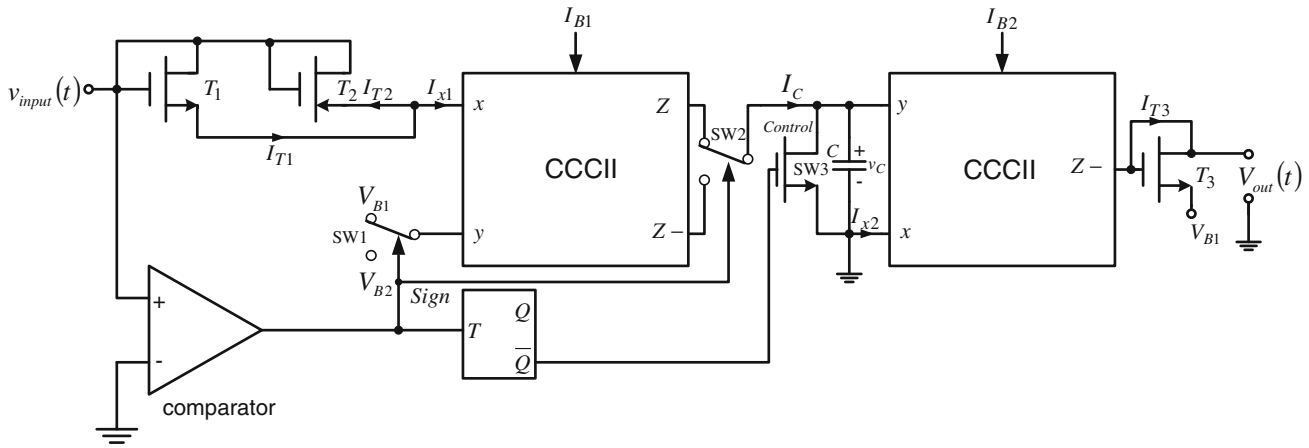

Fig. 1 The proposed realization of RMS circuit

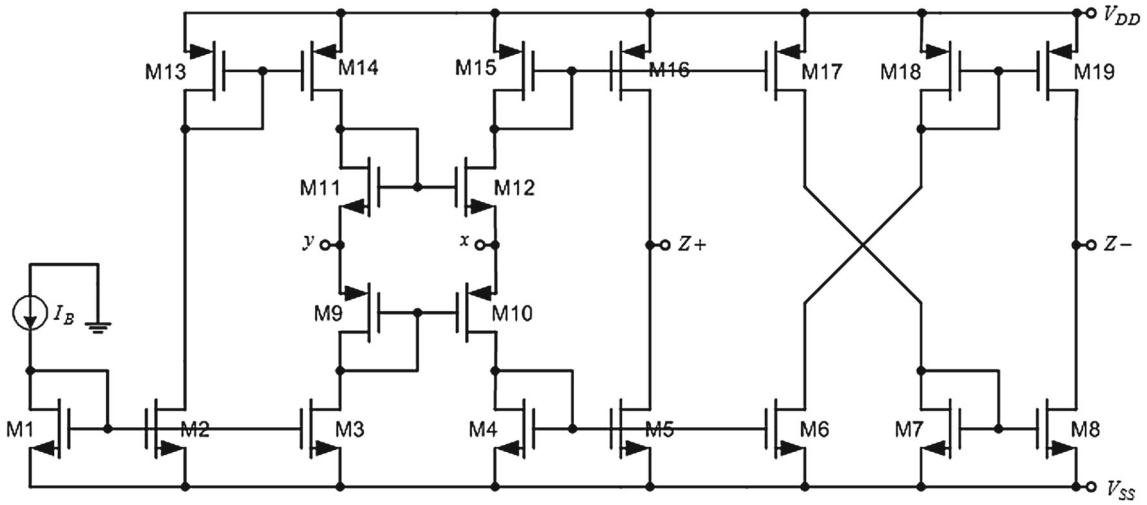

Fig. 2 Schematic of the CMOS CCCII

Here k is the process trans-conductance parameter of the MOS transistor. I_B is the bias current used to control the intrinsic resistance at x port. In general, CCCII can contain an arbitrary number of z terminals; provide both directions of currents I_z. The internal construction of the CMOS CCCII is shown in Fig. 2.

It should be noted that the first CCCII in Fig. 1 should has low impendance ($R_{x1} \cong 0$) by setting value of I_{B1} at the highest possible value allowed by the proposed configuration of CCCIIs to achieve low input impedance of the first CCCII. The real limit of the bias current is defined after simulation checks in Sect. 4. Also, the graph of the bias current vs. R_x will be also included. The second CCCII in Fig. 1 forms current-mode inverting lossless integrator. Considering the circuit in Fig. 1 and using CCCII properties, the current transfer function of second CCCII is written as:

$$\frac{I_{T3}}{I_C} = -\frac{1}{sCR_{x2}}. \tag{3}$$

If $v_{\text{input}}(t) > 0$, the current is conducted through the NMOS transistors T_1 to the output. However, if $v_{\text{input}}(t) < 0$, the PMOS transistor T_2 conducts the current to the output hence the current–voltage relationships of the MOS transistors are given by:

$$I_{T1} = \frac{k_n}{2}(v_{\text{GS1}} - V_{\text{Tn}})^2 = \frac{k_n}{2}v_{\text{input}}^2(t); \quad \text{for } v_{\text{input}}(t) > 0$$
$$I_{T2} = \frac{k_p}{2}v_{\text{input}}^2(t); \quad \text{for } v_{\text{input}}(t) < 0. \tag{4}$$

NMOS and PMOS transistors conduct in opposite halves of the input signal. Depending on the detected sign of the input signal (the control signal *Sign*), over the comparator, the position of the switches SW1 and SW2 can be determined (CMOS analogue switch like single-pole double-throw *Maxim* MAX319), and the corresponding threshold voltage is connected to y port of the CCCII. Such control enables current input from the port $z+$ on the integrator at the interval in which the input voltage signal is positive, i.e.,

from the port $z-$ when the input voltage is negative. If the input amplitude is below $V_{\mathrm{Tn}(p)}$ as in sub-threshold circuits (very rare situation in practical applications), it will require boosting the level of the input signal. If we assume that:

$$k_{n(T1-T3)} = k_{p(T2)} \tag{5}$$

it follows that:

$$I_C = -\left(I_{T1} + I_{T2}\right) = -\frac{k}{2} v_{\mathrm{input}}^2(t)\,. \tag{6}$$

The voltage formed in this way at the condenser C will generate current which will be equalized with the current of the T_3 transistor:

$$I_{T3} = \frac{1}{R_{x2}C}\frac{k}{2}\int_0^{t_1} v_{\mathrm{input}}^2(\tau)\,\mathrm{d}\tau = \frac{k}{2}V_{\mathrm{out}}^2(t_1)\,. \tag{7}$$

As inferred from above, it follows that:

$$V_{\mathrm{out}}(t_1) = \sqrt{\frac{1}{R_{x2}C}\int_0^{t_1} v_{\mathrm{input}}^2(\tau)\,\mathrm{d}\tau}\,. \tag{8}$$

By choosing $R_{x2}C = T$ and $t_1 = T = 1/f$, where T is the period of the input complex signal, it is clear that relation (8) is a definition expression which enables calculating the effective value of the input complex voltage signal. It is important to note that (8) is valid for any input signal (sine-, square-, triangular-wave) with a T period. The performance of the proposed circuit is controlled by means of the SW1, SW2, and SW3 (switches), as well as the *Control* signal. The switch SW3 ought to be open at the interval equalling the T period of the input signal. The control signal *Control* can be generated in accordance with the detected zero-crossing of the input signal, over the edge-triggering T flip-flop. The flip flop toggles at any negative-to-positive sign reversal. Integration over a period occurs only if there is only a single zero-crossing transition (with positive slope) in a signal period, which is valid for most real signals. In the period where the SW3 closes, the C condenser is discharged to the zero voltage, thus preparing the integrator for the next round of the charging process.

This kind of processing does not introduce limitations regarding the type of the signal and number of harmonics that is being processed, i.e., this signal can contain non-harmonic components as well (inter-harmonics and sub-harmonics. However, it will be necessary to determine the period of such a complex signal, as it was done in [30]. The proposed circuit is very appropriate for hardware realization in the integrated technology, and possesses much simpler structure than circuits described in [7,31–33].

3 Error analysis

Given the non-ideal current gains of the CCCIIs α_1 and α_2 (ignoring the effects of voltage gains), the output voltage (Fig. 1) is given by:

$$V_{\mathrm{out}}(t_1) = \sqrt{\frac{1}{R_{x2}C}\int_0^{t_1}\left(\alpha_1 v_{\mathrm{input}}^2(\tau)_+ + \alpha_2 v_{\mathrm{input}}^2(\tau)_-\right)\mathrm{d}\tau}$$
$$v_{\mathrm{input}}(t)_+ = \begin{cases} v_{\mathrm{input}}(t)\,, & \text{for } v_{\mathrm{input}}(t) > 0 \\ 0, & \text{otherwise} \end{cases} \tag{9}$$
$$v_{\mathrm{input}}(t)_- = \begin{cases} v_{\mathrm{input}}(t)\,, & \text{for } v_{\mathrm{input}}(t) < 0 \\ 0, & \text{otherwise.} \end{cases}$$

Therefore, the parameters α_1 and α_2 are in the form of multiplier constants for the two cycles of input voltage. If Eq. (5) is not satisfied, the following inequality is obtained:

$$V_{\mathrm{out}}(t_1) = \sqrt{\frac{1}{R_{x2}C}\int_0^{t_1}\left(\alpha_1 v_{\mathrm{input}}^2(\tau)_+ + \alpha_2\frac{k_p}{k_n} v_{\mathrm{input}}^2(\tau)_-\right)\mathrm{d}\tau}\,. \tag{10}$$

It is observed in (10) that the square of the negative cycle of input signal is multiplied by k_p/k_n instead of unity. Fortunately, using ECCIIs [34], $\alpha_1 = \alpha_2 k_p/k_n = 1$ can be adjusted. It is obvious that the relation (8) is valid under the ideal condition: $R_{x2}C = T = t_1; \alpha_1 = 1; \alpha_2 = 1; k_p/k_n = 1; \lambda_i v_{\mathrm{DS}i} = 0, i = [1, 2, 3]$, where λ, the channel-length modulation parameter, models current dependence on drain voltage due to the early effect, or channel-length modulation. In the proposed circuits, $v_{\mathrm{DS}i} = v_{\mathrm{GS}i}$.

If the body effect is considered, body–source voltage affects the threshold voltage, which is shown in Eq. (11):

$$V_{\mathrm{T}} = V_{\mathrm{T0}} + \Delta V_{\mathrm{T}} = V_{\mathrm{T0}} + \gamma\left(\sqrt{V_{\mathrm{SB}} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{11}$$

where V_{T} is the threshold voltage when substrate bias is presented, V_{SB} is source-to-body substrate bias, $2\phi_F$ is surface potential, and V_{T0} is threshold voltage for zero substrate bias, $\gamma = (t_{ox}/\varepsilon_{ox})\sqrt{2q\varepsilon_{si}N_A}$ is body effect parameter, t_{ox} is oxide thickness, ε_{ox} is oxide permittivity, ε_{si} is permittivity of silicon, N_A is doping concentration and q is charge of an electron. In the proposed peak detector, each body of every MOS transistor is connected to its source ($V_{\mathrm{SB}} = 0$) then $V_{\mathrm{T}} = V_{\mathrm{T0}}$, except for central positioned NMOS transistors in CCCIIs and transistors T_1, T_2, and T_3 (Fig. 1). The body of transistor T_3 is actually connected to V_{SS}, while its drain provides the voltage output. This output offset voltage cannot be eliminated. When a small deviation offset occurs, the output voltage $v_{\mathrm{out}}(t)$ in non-ideal condition becomes:

$$V_{\text{out}}(t_1) = \sqrt{\frac{1}{(1+\lambda_3 v_{\text{DS3}})\, R_{x2}C} \int_0^{t_1} \left(\alpha_1 v_{\text{input}}^2(\tau)_+ (1+\lambda_1 v_{DS1}) + \alpha_2 \frac{k_p}{k_n} v_{\text{input}}^2(\tau)_- (1+\lambda_2 v_{\text{DS2}}) \right) \mathrm{d}\tau + \Delta V_{\text{T}}} \tag{12}$$

A question is raised as to the nature of the output voltage in the proposed RMS detector in circumstances when ideal conditions are not met. For any divergence in the value of the parameter in relation to its nominal value, it is possible to determine the value of the output voltage and calculate the ensuing error. For example, in (12), parameter α_2 is replaced with $(1+\delta\alpha_2/100)\,\alpha_2$, where $\delta\alpha_2$ represents the percentage divergence in the value of the α_2 parameter in relation to its nominal value, then the value of the output voltage V_{out} is calculated. Relative error in the measuring is subsequently calculated:

$$e = \frac{V_{\text{out}} - V_{\text{eff}}}{V_{\text{eff}}} 100. \tag{13}$$

But, how large is the uncertainty of error e, calculated in this way given the partial uncertainties of the parameters considered? The answer to this question ought to represent the *uncertainty budget* which is based on the procedures described in GUM [35], and is shown in Table 1.

The values in Table 1 correspond to the case where all the parameters of interest are known within the limits of ±1 % in relation to their nominal values, based on a uniform distribution of probability. Further on, the input voltage is formed in such a manner that its DC component, as well as amplitudes and phases of its harmonics, are set in random manner (uniform distribution), respectively. The specific nature of the uncertainty budget set in this manner is reflected in the fact that for certain parameters it is not possible to establish exact values for sensitivity coefficients, since the particular values are dependent on the form of the input voltage $v_{\text{input}}(t)$.

Intervals for possible values of those sensitivity coefficients, as well as their distributions, can be determined by a fairly large number of simulations of the measuring procedure, and by varying parameter values and harmonic content of input voltage. (*Sensitivity to changes in certain factors is a function of the form of the input voltage $v_{\text{input}}(t)$; *for practical reasons, uncertainty of parameters $\lambda_i v_{\text{DS}i}$ has been expressed in percentages of one.).

- Sensitivity coefficients for parameters $R_{x2}C$ and $\lambda_i v_{\text{DS}i}$ do not depend on the waveform of the input voltage and are known exactly.
- As for parameters $\alpha_i \lambda_i v_{\text{DS}i}$ and k_p/k_n, sensitivity coefficients range between 0.0 and 0.5, with approximately uniform distributions.
- Sensitivity coefficient for parameter t_1 extends from 0.0 to ∼3.0, with approximately hyperbolic distribution.

In Table 1, sensitivity coefficients take their maximum values whereby the combined uncertainty and expanded uncertainty (for a coverage factor $k = 2$) are 1.9 and 3.8 %, respectively. It is clear that these figures are overestimated, but, for which amount? The GUM procedures do not offer the answer.

Regardless of the fact that the uncertainty budget given in Table 1 is the base for the analysis of the uncertainty, this Table is useful because it yields information on the extent to which variations in certain parameters influence the precision of measuring.

If some entries in Table 1 were already determined using simulations and by varying parameter values and waveform of the input voltage, it is reasonable that attempts that complete treatment of uncertainty estimation would be based on simulation of the measuring procedure, as it is suggested in [35]. It can be expected that this approach offer more realistic uncertainty evaluation, given the fact that it does not imply any assumptions, neither regarding the distribution of the output value—the error in the measuring results, nor the

Table 1 Uncertainty budget

The size of the error in determining the RMS value of the input voltage, which occurs as a consequence of the non-ideal nature of the components applied in the circuit proposed in Fig. 1

[a] Uncertainty of parameters is expressed as percentages of one, for practical reasons

Parameter	Estimate	Standard uncertainty (%)	Type	Distribution	Sensitivity coefficient	Contribution to the standard uncertainty (%)
$R_{x2}C$	0.020 ms	0.58	B	Uniform	−0.50	0.29
t_1	0.020 ms	0.58	B	Uniform	3.0	1.73
α_i	1	0.58	B	Uniform	0.50	0.29
ΔV_{T}	1	0.58	B	Uniform	0.50	0.29
k_p/k_n	0	0.58	B	Uniform	0.50	0.29
$\lambda_i v_{\text{DS}i}$	1	0.58[a]	B	Uniform	0.50	0.29
e	0					1.91

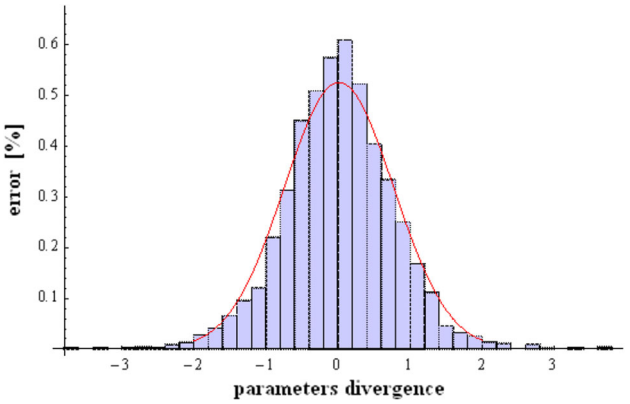

Fig. 3 The distribution of errors, for the divergence in the value of the parameters, from their nominal values

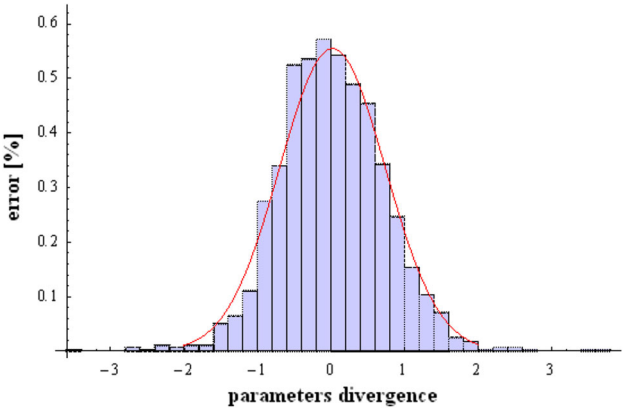

Fig. 4 The distribution of errors for the divergence in the value of the parameters, from their nominal values in case of processing the signal containing inter-harmonics

distributions of the sensitivity coefficient values. Therefore, under the identical assumptions, we assumed that the input voltage has randomly set DC component, and amplitudes and phases of its harmonics; the observed parameters gain, in random manner, the value within the range of ±1 % around their nominal values. The result of implementation of the Monte Carlo variants is shown in Fig. 3.

The expanded measuring uncertainty obtained here amounts to 1.5 %, and it ought to be compared with the data obtained from the uncertainty budget (3.8 %, i.e., 1.6 %). The estimated error is much lower than in case of RMS detector presented in [31]. The number of individual simulations in the presented case was 2,200. The simulations were performed assuming that the input voltage $v_{\text{input}}(t)$ has a DC component and ten harmonics, with randomly chosen amplitudes and phases. An almost identical result is obtained in the case where the selected number of harmonics is 3.

3.1 Impact of inter-harmonics and sub-harmonics

The experiments were repeated, in case the input voltage $v_{\text{input}}(t)$ should contain inter-harmonics, in addition to harmonics. The input voltage is represented by:

$$v_{\text{input}}(t) = V_0 + \sum_{i=1}^{n} V_i \sin(i\omega t + \varphi_i) + \sum_{i=1}^{n-1} V_i' \sin\left(\frac{i}{n}\omega t + \varphi_i'\right) + \sum_{i=2}^{n-1} V_i'' \sin\left(\frac{n}{i}\omega t + \varphi_i''\right). \quad (14)$$

For the simplicity reasons, i.e., alleviating the complexity of concrete calculations and reducing the time for performing simulations, it was decided to apply $n = 3$. No suppositions were made concerning the amplitudes and phases of certain harmonics (i.e., the fact that amplitudes of harmonics in real systems tend to decrease, the later in the sequence they occur, etc.). Parameters V_0, V_i', V_i'', φ_i, φ_i', φ_i'' will gain random values within 0–1, i.e., within 0–2π. The number of individual simulations was 1,500 (Fig. 4), the measuring uncertainty obtained here amounting to 1.4 %. It can, therefore, be concluded that the system functions equally well when inter-harmonics are added to the input voltage.

4 Simulation results

The operation of the proposed circuit was verified using PSpice simulation program. The PMOS and NMOS transistors were simulated, respectively, using the parameters of a 0.25 μm TSMC CMOS technology [36]. The comparator was simulated based on the realization described in [37]. Comparator detects passing of the voltage signal through zero, thus ensuring synchronization of the measuring cycle with the frequency of the processed signal. This comparator triggers at about 2.5 mV, so the error is about 20 ns. This error can be ignored as there is no accumulation. Switches SW1–SW3 were simulated using the parameters of CMOS analogue switches MAX319/318 [38]. The positive-edge-triggered T flip-flop was simulated using the parameters of D flip-flop 74LVC1G80 [39].

The aspect ratios of a PMOS and NMOS transistor are listed in Table 2. Figure 2 provides schematic description of the CCCII used in the simulations. The circuit was biased with ±1.25V supply voltages, $C = 0.1$ nF, $I_{B1} = 300\,\mu$A, and $I_{B2} = 100\,\mu$A. In addition, $V_{B1} = -0.4238$ V and $V_{B2} = 0.5536$ V were chosen.

The possible design of such bias voltages is shown in Fig. 5, based on circuits proposed in [40]. In contrast to the circuit described in [40], the simulation check involved the

Table 2 Dimensions of transistors

Transistor	W (μm)	L (μm)
M1–M8	5	0.5
M9–M10	16	0.25
M11–M12	8	0.25
M13–M15, M17–M19	15	0.5
M16	15.1	0.5

parameters defined in [41], at temperatures $T = -45$, 25 and 145 °C. At room temperature, for supply voltage of 1.25 V circuits generate voltage $V_B = 0.424$ V operating at 1.7 μA supply current, and with $\sigma = 0.81$ % (reference voltage 1 sigma spread). Within the observed temperature range (from −45 to +145 °C), the temperature coefficient (TC) of the proposed circuits was 30 ppm/°C. The circuit specified in [42] can also be used along with the solution described in the paper.

Figure 6 shows the relation of the bias current I_B vs. port resistance R_x for the proposed realization of the CCCII, implying the real limits of the bias currents in the possible practical implementation of the proposed RMS detector. To achieve the conditions defined in Sect. 2, the bias current needs to be set as $I_{B1} = 260\,\mu$A so as to obtain low input port resistances of the first CCCII. By changing the bias current I_{B2} (second CCCII) we can change the time constant of the realized integrator.

During the simulation, the parameters of the input signals correspond to the values given in Table 3, with fundamental frequency $f = 1/T = 5$ MHz.

The plots for the RMS of the multi-harmonic, square- and triangular-wave signals are, respectively, depicted in Fig. 7

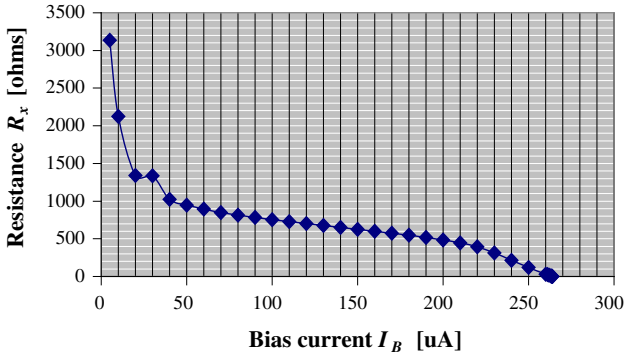

Fig. 6 Dependence of the port resistance on bias current of the proposed CCCII

(the signal at the output of the circuit), for the parameters defined in Table 3. It can be observed that the value of the signal at the output of the suggested circuit reaches the effective value that the processed input signal has at the end of its period. After reading this value, capacitor C is discharged, which allows the circuit to perform a new calculation of the effective value of the input signal that is being processed.

Power consumption of the simulated RMS detector was 4.28 mW. Small power consumption of the proposed circuits results from applying low-voltage current mode and transconductance mode integrated circuits using CMOS technique. Applying the current mode signal processing to solve issues under consideration is the right approach to the problem. Considering the dynamic range as the one with the nonlinearity level lower than 1 dB, the dynamic range of the circuit proposed in this paper is around 26 dB. The maximum amplitude of the processed input signal is 1 V.

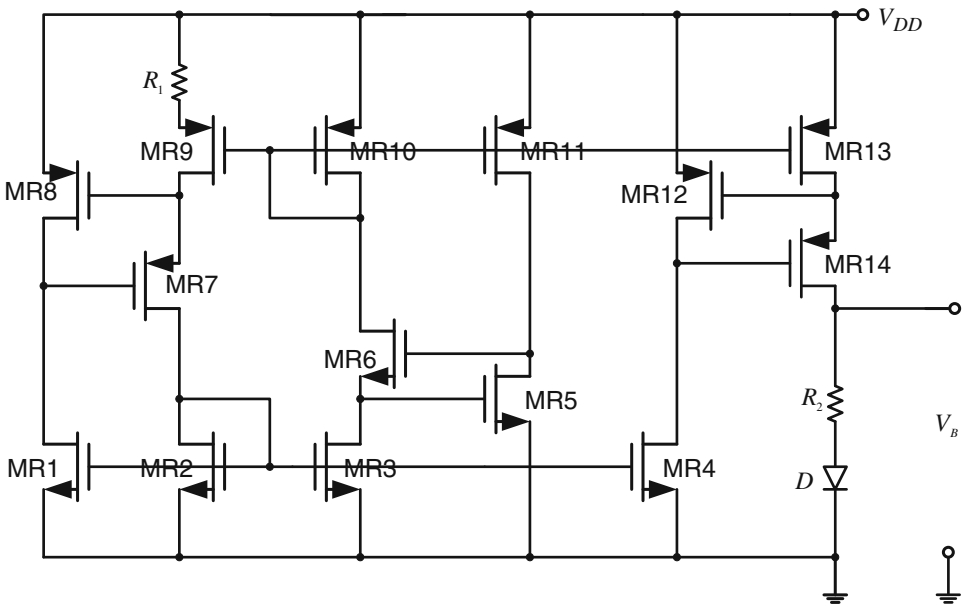

Fig. 5 CMOS voltage reference circuits

Table 3 Simulation results of the proposed RMS circuit in the SPICE program

Type of input signal	Amplitude (V)	Phase (rad)	Obtained RMS value	Relative error of measured RMS value of voltage (%)
Multi-harmonic sine signal $v_{\text{input}}(t) = \sum_{r=0}^{N} V_r \sin(r\omega t + \psi_r)$	V_1=0.3; V_2=0.25; V_3=0; V_4=0.12; V_5=0.05	$\psi_1 = 0$; $\psi_2 = \pi/2$; $\psi_3 = 0$; $\psi_4 = \pi/3$; $\psi_5 = \pi$	0.291	0.13
Square-wave input signal	0.5		0.499	0.16
Triangular-wave input signal	0.5		0.288	0.14

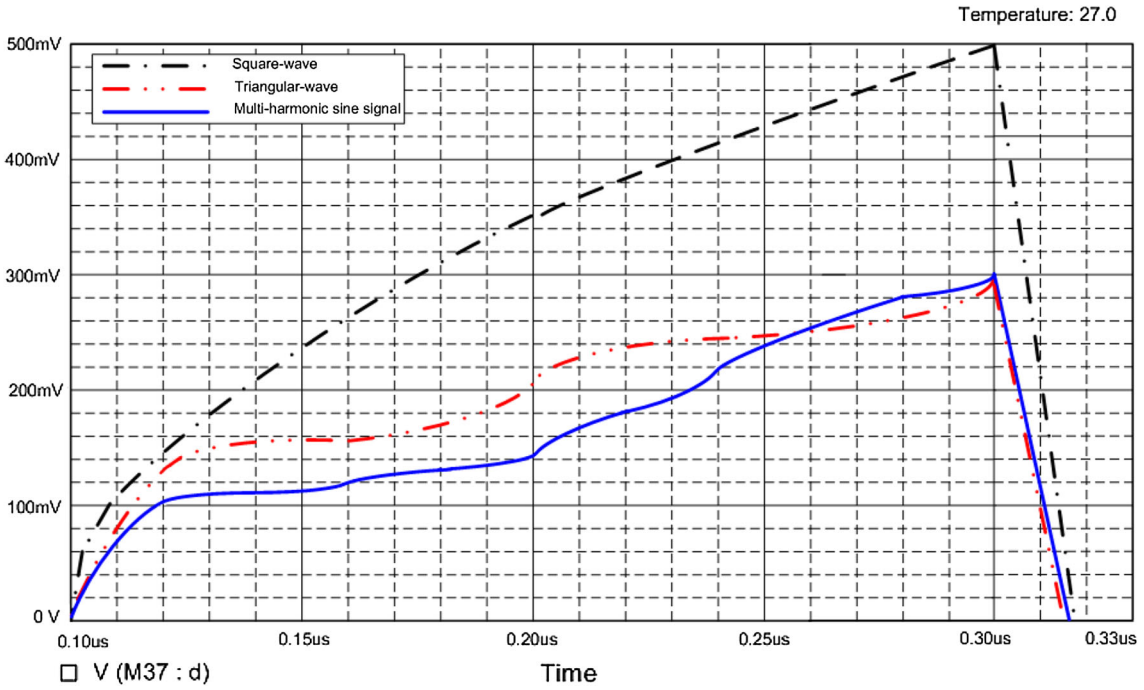

Fig. 7 Time–domain response of the proposed RMS circuit for the multi-harmonic sine, square-wave, and triangular-wave input signals

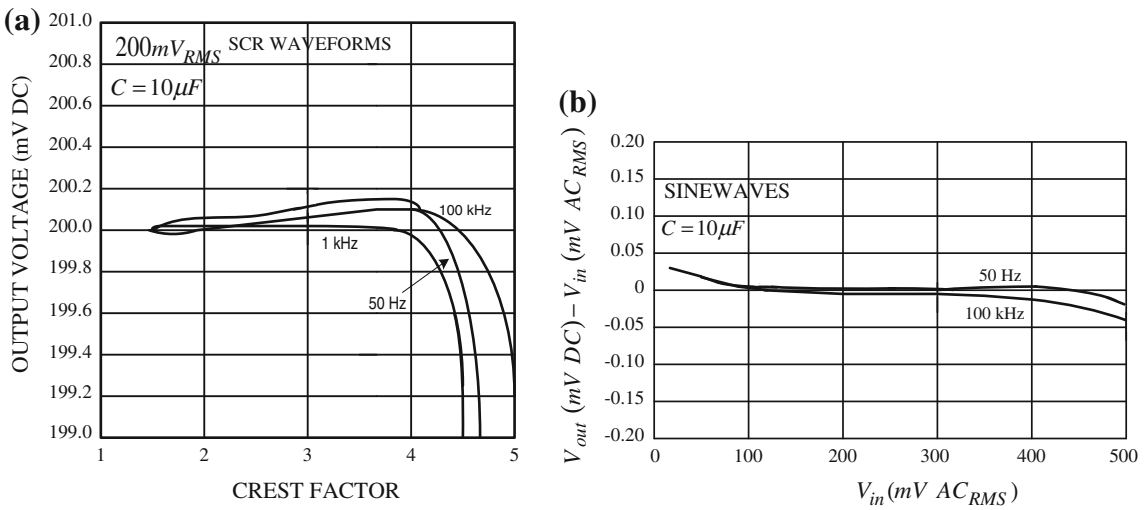

Fig. 8 **a** Performance vs. crest factor; **b** AC linearity

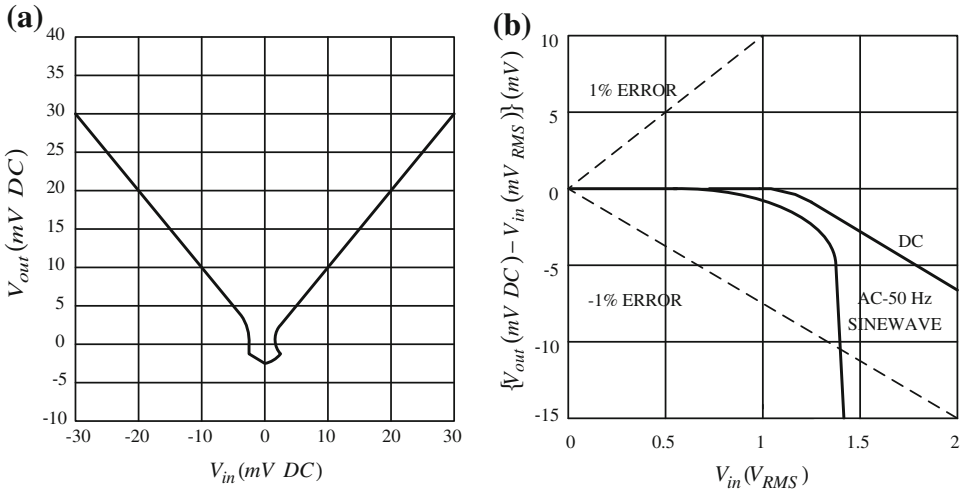

Fig. 9 **a** DC transfer function near zero; **b** output accuracy vs. signal amplitude

Figures 8 and 9 show the typical performance characteristics of the proposed detector.

The results shown in Table 3 and in Figs. 8 and 9 confirm the possibility of highly precise determination of the effective value of the input multi-harmonic signal using the proposed circuit. The error in calculating the RMS value of multi-harmonic signals is smaller than the detector proposed in [10,43,44], where the structure of the proposed circuits are much simpler than in [31].

In many applications, particularly in sensor signal processing, the inputs and outputs need to be analogue, so that the unlimited resolution and accuracy possible with purely digital circuitry will not be available [45].

5 Conclusion

In this paper, an electronically tunable current-mode RMS detector for measuring the RMS value of multi-harmonic, band-limited input voltage signal has been presented. The proposed configuration is simple and can be electronically controlled. The proposed circuit requires only single grounded capacitor as passive element, which is advantageous in integrated circuit implementation and high-frequency operation point of view. The calculation of the effective value has been performed in full accordance with the definition formula, successfully overcoming almost all of the shortcomings that hindered the calculation of the effective value using the realizations known so far. The PSpice simulation results were depicted, and agree well with the theoretical anticipation.

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