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ORIGINAL PAPER

Power factor-corrected DCM-based electronic ballast

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Abstract This paper deals with the design, modeling, analysis and simulation of power factor-corrected and low crest factor-based electronic ballast for a compact fluorescent lamp. The proposed electronic ballast is a combination of a buck–boost ac–dc converter as power factor regulator operating in discontinuous conduction mode and a half bridge series resonant inverter, which is used for converting constant dc link voltage into high-frequency ac voltage to drive the fluorescent lamp. The design, modeling and simulation of this topology are performed using MATLAB-Simulink for an 18 W, 220 V, 50 Hz compact fluorescent lamp. With the utilization of proper commutation techniques like zero voltage switching, the overall switching losses are reduced at high operating frequency of 60 kHz. The power quality indices such as displacement power factor, distortion factor, total harmonic distortion of ac mains current, power factor and crest factor are evaluated for proposed electronic ballast, which is found as per IEC-61000-3-2 class C requirements.

Keywords Discontinuous conduction mode (DCM) · Electronic ballast · Power factor regulator (PFR) · Series resonant inverter (SRI) · Zero voltage switching (ZVS)

1 Introduction

In these days, a high-frequency (HF) electronic ballast is preferred due to high luminous efficacy, no flicker, no humming noise, less size and weight, long life, over the electromagnetic ballast to drive the fluorescent lamps, since it cannot be ignited directly from the ac mains. The fluorescent lamp consists of a gas tube which is completely filled with argon gas and mercury vapors along with two filament electrodes at each end. The inner part of the tube is coated with phosphors material and filament electrodes are coated with such materials which can assist in the emission of more electrons. With a proper ignition voltage, an electric discharge is produced between both the electrodes. This discharge generates the invisible ultraviolet radiations and phosphor absorbs these ultraviolet radiations to produce visible light [1–3].

All discharge lamps inherently have negative dynamic impedance characteristics in their normal operating region. Thus, electronic ballast plays an important role to serve two purposes, one is to provide a sufficient ignition voltage normally of the order of 500–1,000 V for necessary discharge required inside the lamp and the other is to limit and stabilize the lamp current after the ignition process, otherwise the lamp electrodes may be damaged.

Power factor correction (PFC) can be achieved using passive and active PFC techniques. Active PFC technique is better than passive PFC technique, but it is costly, since active PFC converter design and its proper control are complicated as compared to the passive PFC [4]. Power quality improvement at the input ac mains can be achieved using improved power quality converters and it has been discussed in detail by Singh et al. [5]. But the existing HF electronic ballast has power quality problems like poor power factor (PF), high crest factor (CF) and high total harmonic distortion (THD_i) of ac mains current which is not as per the compliance of IEC 61000-3-2 standard for class C equipments [6]. In power factor-corrected electronic ballast, the input power factor can be improved nearly up to unity.

In this paper, PFC is performed using a buck–boost converter operating in discontinuous conduction mode (DCM), where the input ac mains current inherently follows sinusoidal ac mains voltage waveform using the voltage follower scheme. In the present work, two power conversion

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stages are used, one is a high power factor regulator (PFR) stage, which converts the ac mains voltage to a regulated dc voltage and second stage converts this regulated dc voltage to a high frequency ac voltage, which is essential to drive the fluorescent lamp.

This method provides nearly unity power factor with low CF and low THD of ac mains current for varying ac mains voltage in between 170–270 V, which is as per IEC-61000-3-2 class C requirements. Section 2 deals with the description of proposed electronic ballast. The design and analysis of the proposed circuit are presented in Sect. 3. Section 4 deals with the voltage follower control strategy used for achieving PFC and Sect. 5 covers the different operating modes of the proposed ballast. A MATLAB model of the proposed ballast is developed in discrete time frame using Simulink and Sim Power System (SPS) toolboxes in Sect. 6. Section 7 deals with the results and discussion. The concluding remarks are given in Sect. 8.

2 Proposed PFC electronic ballast

The proposed electronic ballast is shown in Fig. 1, which consists of a PFC buck–boost converter and a high-frequency series resonant inverter (SRI). Since PFC buck–boost converter operates in DCM, it inherently modulates the ac mains current to follow the line voltage and achieves nearly unity power factor for a widely varying input ac mains voltage. Simultaneously the resonant inverter provides sufficient ignition voltage and supplies constant lamp current at high frequency.

In proposed electronic ballast, the input ac mains voltage is rectified and filtered to provide dc output voltage. Then a constant dc link voltage of 400 V is achieved for wide varying input ac mains voltage (i.e., 170–270 V) using a PFC buck–boost converter [2]. This dc link voltage is converted into a high- frequency ac waveform by alternately turned on and off power MOSFETs M_1 and M_2 at operating switching frequency of 60 kHz. The dc blocking capacitor blocks the dc components present in this high- frequency voltage waveform. The high-frequency ac voltage causes the resonance through the LC network to create high ignition voltage across the electrodes to develop arc inside the fluorescent lamp. The switching frequency of the SRI is kept more than the resonance frequency of LC network to ensure zero voltage switching (ZVS) operation of both power switches, which reduces switching losses at high operating frequency. This improves the efficiency of the electronic ballast.

3 Design and analysis of PFC buck–boost converter-based electronic ballast

The design procedure of the components of PFC buck–boost converter [4,7] and the resonant inverter of electronic ballast are given as follows.

3.1 Design of buck–boost converter

For a buck–boost converter operating in DCM, the selection of dc link voltage should be done properly and it is defined as,

$$V_{dc} \geq \frac{D}{1-D} V_{in(peak)} \tag{1}$$

For operating the PFC buck–boost converter in DCM, the value of inductance should be less than the critical inductance value. The critical value of buck–boost inductance L_{bb} is determined as,

$$L_{bb(crit)} = \frac{(1-D)V_{dc}}{2 f_s I_o} \tag{2}$$

The output capacitor (C_o) must have enough capacitance to maintain constant dc link voltage and should provide continuous load current. It is calculated as,

$$C_o \geq \frac{I_o}{2\omega \Delta V_{co}} \tag{3}$$

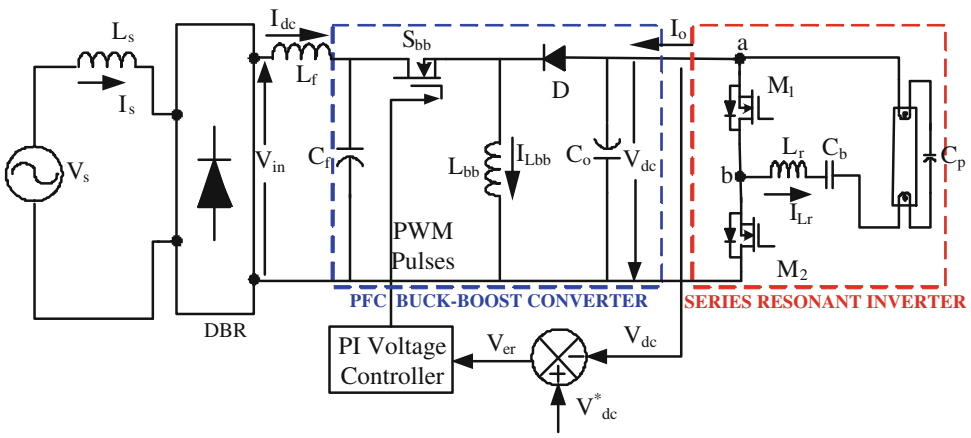

Fig. 1 Schemetic of proposed electronic ballast

where, D is duty cycle, V_o is dc link voltage, $V_{in(peak)}$ is peak value of the input voltage, I_o is output rated current, f_s is switching frequency, V_{co} is the ripple voltage of the output capacitor.

For $f_s = 60$ kHz, $I_o = 0.1636$ A, after solving Eqs. (1–3) for a wide varying ac mains voltage (i.e., 170–270 V), the value of minimum and maximum duty ratio is 0.59 and 0.7. At the input ac mains voltage of 270 V rms, the calculated value of dc link voltage is 395 V (hence it is selected as 400 V). From Eq. (2), the critical value of buck–boost inductance is 6.11 mH (selected as 4 mH, to ensure the DCM operation). The calculated value of bulk capacitor (C_o) is 16.28 μF for voltage ripple of 4 % (it is selected as 18 μF).

3.2 Design of resonant circuit parameters

Under the steady-state condition, the equivalent circuit of the SRI with load as fluorescent lamp is shown in Fig. 2.

In this equivalent circuit, L_r, C_b and C_p are the resonant circuit parameters and R_{lamp} is the steady-state resistance of the fluorescent lamp. The purpose of blocking capacitor C_b is to block the dc component present in the square wave output of the inverter and to allow only the ac components to reach the lamp. The parallel capacitor C_p is used to provide high ignition voltage after the pre-heating interval and as soon as ignition occurs inside the lamp, the steady state current starts flowing through the lamp.

At the time of starting, the resonant circuit is formed by L_r, C_b and C_p thus the starting resonance frequency is defined as,

$$\omega_{starting} = \frac{1}{\sqrt{L_r \cdot C_{eq}}} \tag{4}$$

Under steady-state condition, the resonant circuit is formed by L_r and C_b hence the resonance frequency is given as,

$$\omega_{running} = \frac{1}{\sqrt{L_r \cdot C_b}} \tag{5}$$

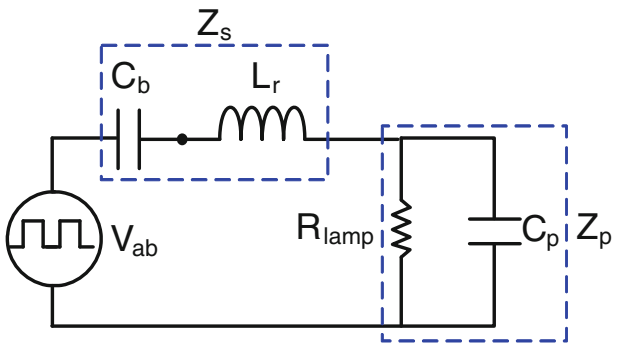

Fig. 2 Series resonant inverter (SRI)

By applying the voltage division rule (Fig. 2), the ratio of rated lamp voltage (V_{lamp}) and fundamental component of input square voltage (V_{ab}) is given as,

$$\left|\frac{V_{lamp}(j\omega)}{V_{ab}(j\omega)}\right| = \left|\frac{Z_p(j\omega)}{Z_s(j\omega) + Z_p(j\omega)}\right|$$

It is simplified as,

$$\frac{V_{lamp}(j\omega)}{V_{ab}(j\omega)} = \frac{1}{[1 + (C_P/C_b) - \omega^2 L_r C_p + j(\omega L_r/R) - (j/\omega CR)]} \tag{6}$$

Now substituting the quality factor, $Q_s = \omega_s L_r / R_{lamp}$, the frequency ratio $x = (\omega_r/\omega_s)$ and resonance frequency after ignition $f_r = (1/2\pi\sqrt{L_r C_b})$ in Eq. (6), then it results in,

$$\left|\frac{V_{lamp}}{V_{ab}}\right| = \frac{1}{\sqrt{\left[1 + (C_P/C_b)(1-x^2)^2 + Q_s\left(x - \frac{1}{x}\right)^2\right]}} \tag{7}$$

Under steady state condition, the resistance of fluorescent lamp is given as,

$$R_{lamp} = V_{lamp}^2 / P_{lamp} \tag{8}$$

The parallel resonant capacitor is given as,

$$C_p = \frac{C_b}{(1/x)^2 - 1} \tag{9}$$

The series resonant inductor is given as,

$$L_r = \frac{1}{C_{eq}\omega_s^2} \tag{10}$$

where, $C_{eq} = \left(\frac{C_b C_p}{C_b + C_p}\right)$, V_{lamp} is the rated lamp voltage, V_{ab} is the fundamental component of square voltage, R_{lamp} is the lamp resistance under steady state condition, ω_s is the angular switching frequency, C_b is blocking capacitor, C_p is parallel resonant capacitor and L_r is the series resonant inductor as shown in Figs. 1, 2.

At the time of starting, for sufficient ignition voltage, a quality factor Q_s is selected as 1.7. For ensuring the ZVS operation of both power switches of resonant inverter, frequency ratio is selected as 0.25. By solving Eqs. (7–10), the calculated values of lamp resistance and different components of resonant inverter are $R_{lamp} = 672\,\Omega$ (with 110 V as steady state lamp voltage), $L_r = 3.03$ mH (selected as 3 mH), $C_b = 37.56$ nF (selected as 45 nF), $C_p = 3$ nF.

4 Control strategy

Figure 3 shows the schematic of the control strategy of PFC converter. In this voltage follower control strategy, ac mains

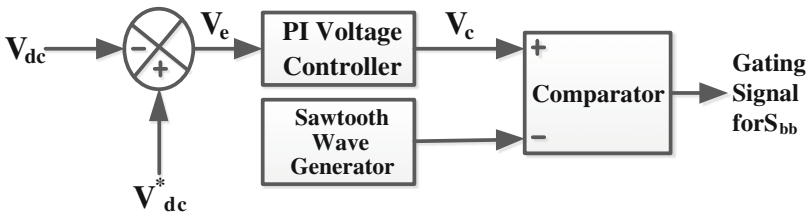

Fig. 3 Control strategy of PFC converter in discrete time frame

current inherently follows the shape of ac mains voltage to achieve high power factor using a PFC buck–boost converter. This control scheme consists of a PI (proportional integral) voltage controller and PWM generation, which provide switching pulses to the solid-state power switch (S_{bb}).

A PI voltage controller is selected for the voltage loop for the regulation of the output dc voltage. The DC voltage, V_{dc} is sensed and then compared with set reference voltage V^*_{dc}. The resulting voltage error $V_e(n)$ at nth sampling instant is given as,

$$V_e(n) = V^*_{dc}(n) - V_{dc}(n) \tag{11}$$

and the output of PI voltage controller at nth sampling instant can be given as,

$$V_c(n) = V_c(n-1) + K_p\{V_e(n) - V_e(n-1)\} + K_i V_e(n) \tag{12}$$

where, K_p and K_i are the proportional and integral gains.

To achieve unity power factor and to reduce current harmonics, the input ac mains current naturally follows the ac mains voltage waveshape. The output of PI voltage controller is compared with fixed frequency carrier wave to generate PWM gating signals for power MOSFET of the PFC buck–boost converter.

If

$$V_c(n) > \text{carrier signal then } S_{bb} = 1 \text{ else } S_{bb} = 0. \tag{13}$$

This gating signal (S_{bb}) is given to gate of the MOSFET of buck–boost converter.

5 Operating modes of proposed electronic ballast

Different operating modes of proposed electronic ballast and its corresponding waveforms are shown in Figs. 4, 5, 6, 7 and 8. The sinusoidal input voltage is considered as constant in each switching cycle, since the switching frequency is much higher than the line frequency. The operating modes are divided into Mode-A to Mode-D and each one is explained in brief.

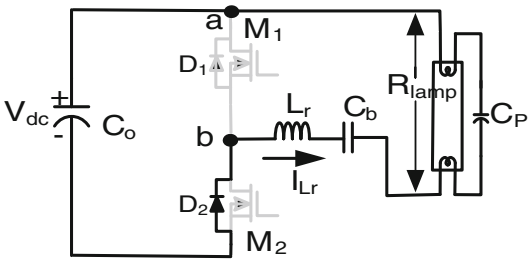

Fig. 4 (Mode-A)

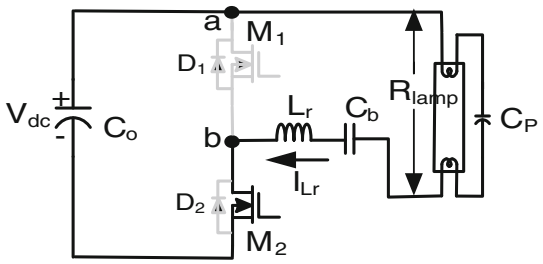

Fig. 5 (Mode-B)

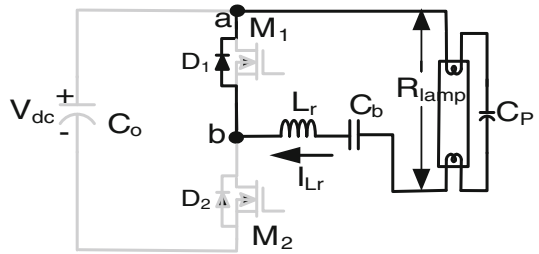

Fig. 6 (Mode-C)

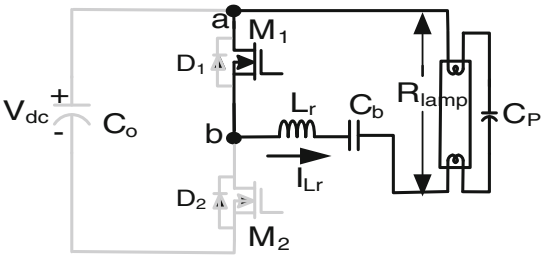

Fig. 7 (Mode-D)

Mode-A ($t_0 \le t \le t_1$)

At time t_o, intrinsic diode D_2 is conducting and it allows the dc link capacitor to be charged and during this interval, the gate pulse (S_2) is also applied to active switch M_2. The path of current is given in Fig. 4.

$$\mathbf{C_o(-) \rightarrow D_2 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow C_o(+)}$$

Mode-B ($t_1 \le t \le t_2$)

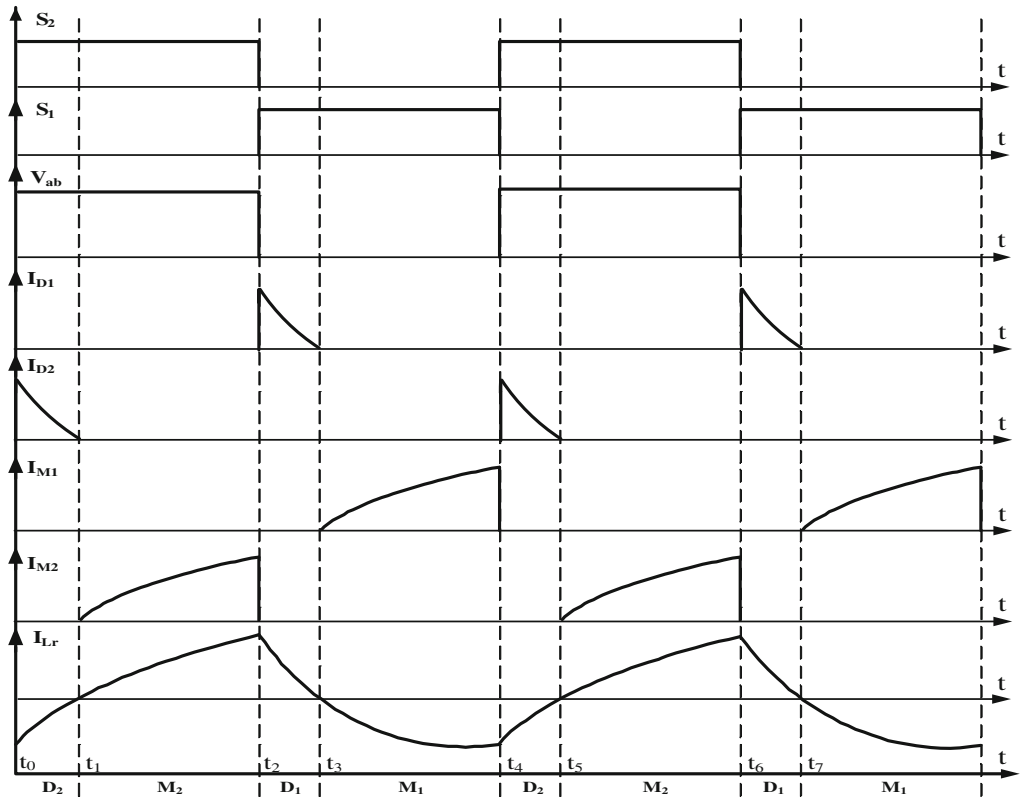

Fig. 8 Theoretical waveforms of resonant inverter stage of proposed electronic ballast

At time t_1, the MOSFET M_2 is turned on at ZVS (zero voltage switching) and dc link capacitor is allowed to discharge. The direction of resonant inductor current changes and increases upto time t_2. At time t_2, this mode completes and the flow of current is shown in Fig. 5.

$$\mathbf{C_o(+) \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow M_2 \rightarrow C_o(-)}$$

Mode-C ($t_2 \leq t \leq t_3$)

MOSFET M_2 is tuned off at time t_2 and intrinsic diode D_1 starts conducting, this allows resonant current to flow in the same direction due to resonating nature of the circuit. During this interval, the gate pulse (S_1) is also applied to active switch M_1. The path of the current is shown in Fig. 6.

$$\mathbf{D_1 \rightarrow (R_{lamp} \| C_P) \rightarrow C_b \rightarrow L_r \rightarrow D_1}$$

Mode-D ($t_3 \leq t \leq t_4$)

At time t_3, the MOSFET M_1 starts conducting and it is confirmed that it is turned on at ZVS. This ensures the change in the direction of resonant current. The path of current is shown in Fig. 8. This mode ends up at time t_4 and then Mode-A to Mode-D repeat for the next switching cycle.

$$\mathbf{M_1 \rightarrow L_r \rightarrow C_b \rightarrow (R_{lamp} \| C_P) \rightarrow M_1}$$

It is shown from the different operating modes over a switching cycle of the above circuit that both MOSFETs (M_1 and M_2) are operating at ZVS. Moreover, to ensure the ZVS of both power MOSFETs M_1 and M_2, the resonant current should lag behind the fundamental component of inverter input voltage (V_{ab}). Hence, switching frequency must be greater than the resonant frequency of the inverter (i.e., $f_s > f_r$), such that nature of resonant circuit as inductive. The theoretical waveform of resonant inverter stage is shown in Fig. 8.

6 MATLAB model of proposed PFC buck–boost converter-based electronic ballast

As shown in Fig. 9, the proposed PFC buck–boost converter-based electronic ballast is modeled in MATLAB/SIMULINK environment, in which compact fluorescent lamp is considered as a resistor at high frequency (60 kHz). In proposed PFC buck-boost converter-based topology, a voltage follower control scheme is applied using a PI voltage controller for operating the buck–boost converter in DCM. The designed values of the PFC converter components and resonant inverter components have been selected properly to get improved power quality at input ac mains. These component values are given in Appendix along with the PI voltage controller parameters. Figure 10 shows the developed model

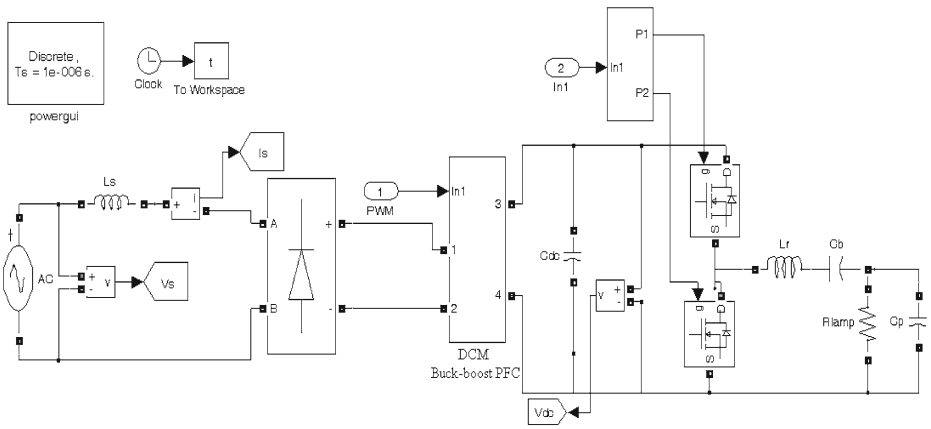

Fig. 9 MATLAB model of proposed electronic ballast

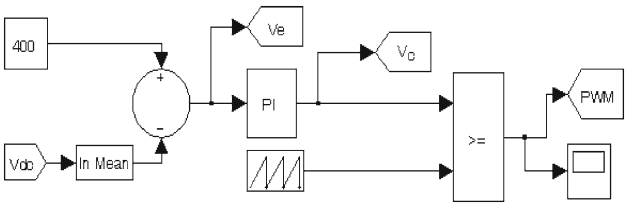

Fig. 10 Voltage follower control scheme for PFC

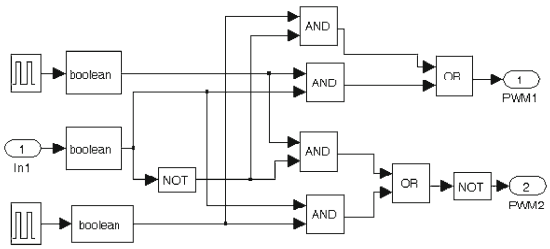

Fig. 11 Switching pattern of SRI MOSFETS

of voltage follower control scheme for achieving PFC with buck–boost converter and Fig. 11 shows the developed model for the generation of switching pattern for active switches of SRI.

7 Results and discussion

The analysis, modeling and simulation of the proposed electronic ballast are performed to validate the design of the circuit, which has low crest factor, high power factor and low THD of ac mains current. With the proper design of a buck–boost converter and a resonant inverter, the dc link voltage is maintained almost constant at 400 V, thus the lamp current remains nearly constant for a wide variation in input ac mains voltage in between 170–270 V. This in confirmed by observing the waveforms shown in Figs. 12, 13 and 14 of the input ac mains voltage (V_s), input ac mains current (I_s), dc current (I_{dc}), dc link voltage (V_{dc}), inductor current (I_{Lbb}), lamp voltage (V_{lamp}), lamp current (I_{lamp}), switches voltages (V_{M1}, V_{M2}) and switches currents (I_{M1}, I_{M2}) at ac mains voltage of 170, 220 and 270 V. For ensuring the DCM operation of the PFC buck–boost converter, the inductor current (I_{Lbb}) has also shown for 170, 220 and 270 V in Figs. 12, 13, 14. Under steady state operation, the lamp voltage (V_{lamp}) and lamp current (I_{lamp}) at ac mains voltage of 170, 220 and 270 V remain same as shown in Figs. 12, 13, 14. Both switches voltages (V_{M1} and V_{M2}) and both switches currents (I_{M1} and I_{M2}) are shown in Figs. 12, 13, 14, which confirm the ZVS operation of both solid-state power switches.

The input ac mains current waveforms along with their harmonic spectra and THD are shown in Fig. 15 at ac mains voltages of 170, 220 and 270 V, which ensures the low THD of ac mains current of proposed ballast for a wide variation in input ac mains voltages.

Table 1 shows the variations of power factor, displacement power factor (DPF), % THD of ac mains current and crest factor (CF) of PFC buck–boost converter-based electronic ballast with a large variation in ac mains voltage demonstrating the improved power quality at ac mains.

8 Conclusion

A buck–boost converter operating in DCM with low crest factor and high power factor has been proposed for an 18 W compact fluorescent lamp. The proposed electronic ballast with PFC buck–boost converter has shown improved power quality such as almost unity power factor and a crest factor of nearly 1.41 for the wide range of ac mains voltage. The current harmonics of the proposed electronic ballast have been compared with the current harmonic limits of IEC 61000-3-2 Class-C equipments and which are within the norms and also crest factor is well below the limit

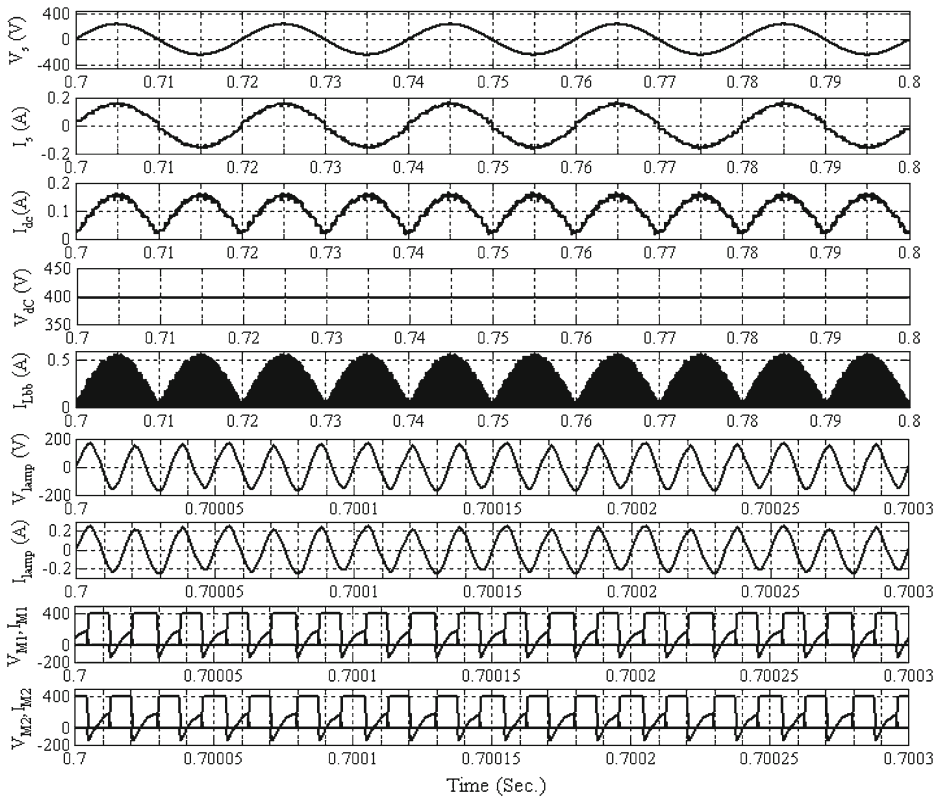

Fig. 12 Performance of proposed electronic ballast in terms of ac mains voltage (V_s), ac mains current (I_s), dc current (I_{dc}), dc link voltage (V_{dc}), buck–boost inductor current (I_{Lbb}), lamp voltage (V_{lamp}), lamp current (I_{lamp}), switch voltage (V_{M1}), switch current (I_{M1}), switch voltage (V_{M2}) and switch current (I_{M2}) at 170 V

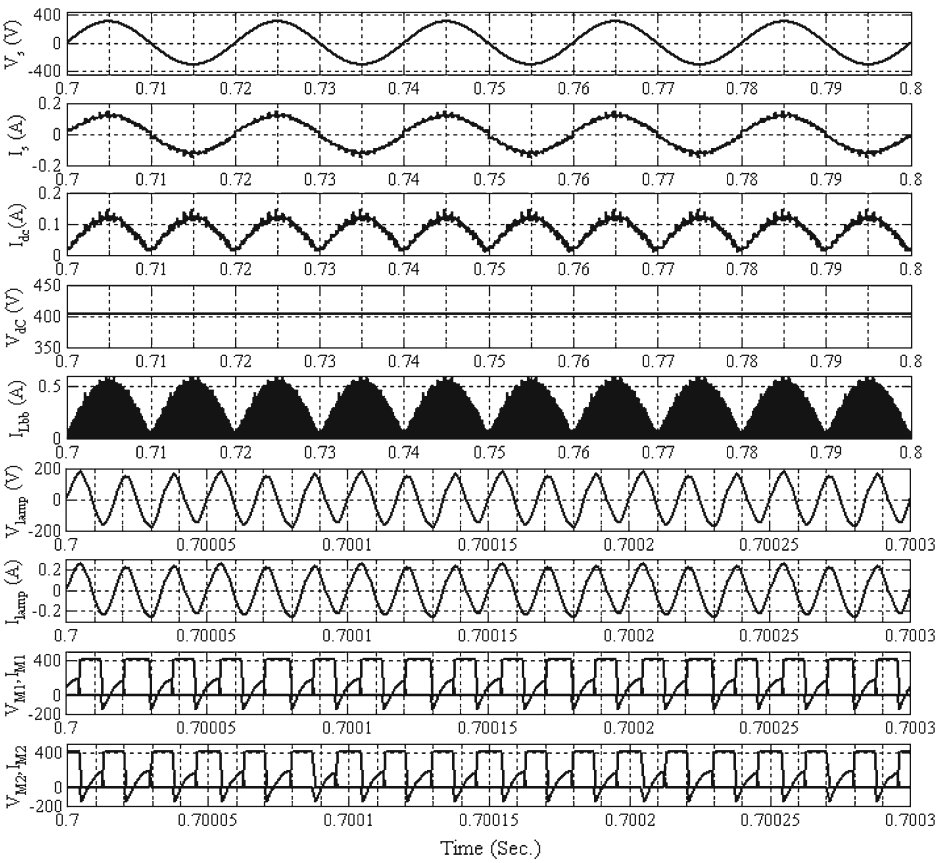

Fig. 13 Performance of proposed electronic ballast in terms of ac mains voltage (V_s), ac mains current (I_s), dc current (I_{dc}), dc link voltage (V_{dc}), buck–boost inductor current (I_{Lbb}), lamp voltage (V_{lamp}), lamp current (I_{lamp}), switch voltage (V_{M1}), switch current (I_{M1}), switch voltage (V_{M2}) and switch current (I_{M2}) at 220 V

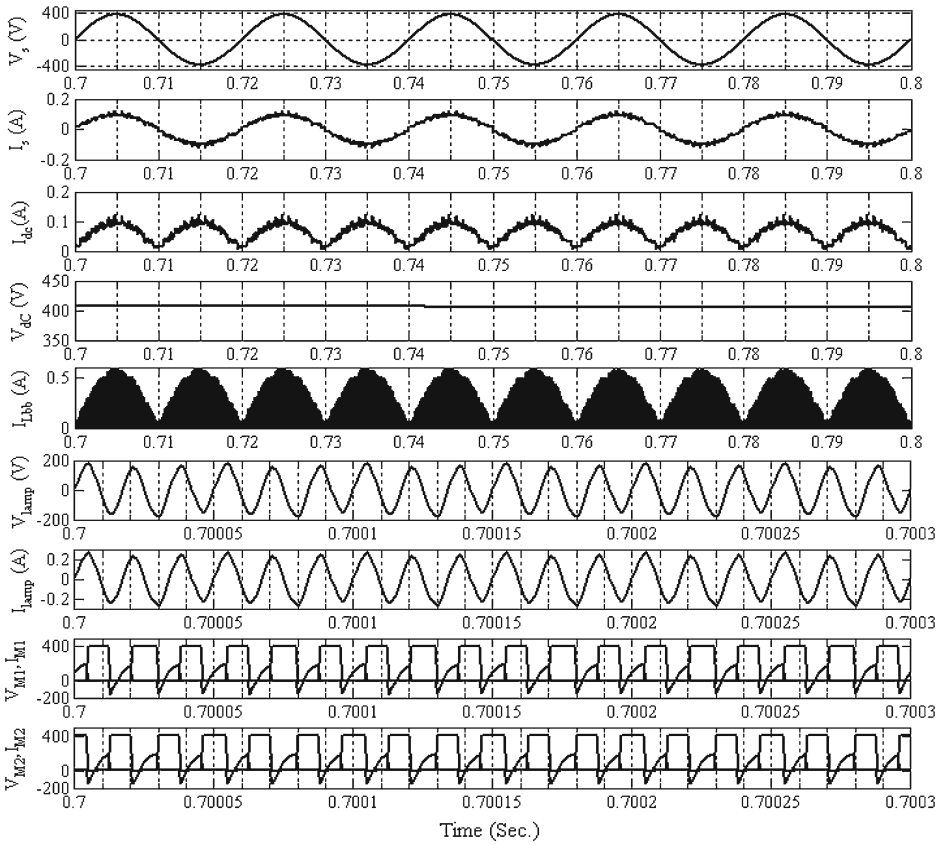

Fig. 14 Performance of proposed electronic ballast in terms of ac mains voltage (V_s), ac mains current (I_s), dc current (I_{dc}), dc link voltage (V_{dc}), buck–boost inductor current (I_{Lbb}), lamp voltage (V_{lamp}), lamp current (I_{lamp}), switch voltage (V_{M1}), switch current (I_{M1}), switch voltage (V_{M2}) and switch current (I_{M2}) at 270 V

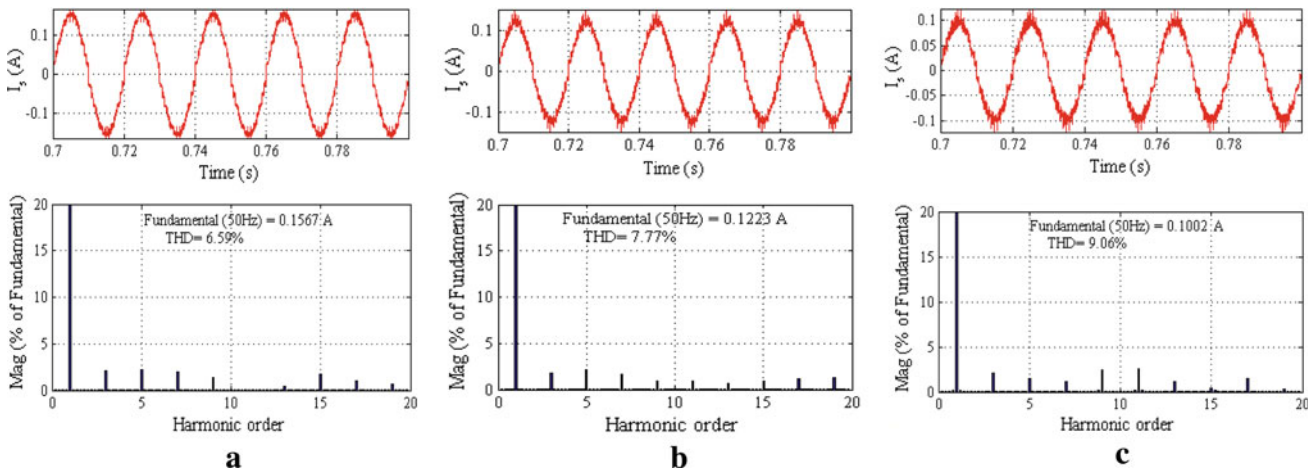

Fig. 15 Input ac mains current waveform and its harmonic spectra at ac mains voltages of **a** 170 V, **b** 220 V and **c** 270 V

of 1.7 [6]. Moreover, DCM has an advantage that it utilizes only voltage control loop as compared to multiple control loops used in CCM. With an optimum design of PFC buck–boost converter and a resonant converter, the lamp current has been maintained close to the rated value. The proposed ballast has ac mains current THD between 6.59 and 10.29 % for voltage range of 170–270 V. The ZVS of solid-state switches has been confirmed, since the series resonant inverter current lags behind the applied square voltage to the inverter. This has been achieved by keeping the switching frequency more than the resonance frequency of the half bridge inverter, which reduces the switching losses and improves the overall efficiency of the electronic ballast.

Appendix

Rated lamp power: 18 W, rated lamp current: 0.1636 A, rated lamp voltage: 110 V, switching frequency (f_s): 60 kHz,

Table 1 Performance parameters of proposed electronic ballast

V_s (V)	I_s (A)	V_{dc} (V)	V_{lamp} (V)	I_{lamp} (A)	PF	DPF	DF	THD_i (%)	CF
170	0.1110	397.5	110.4	0.1643	0.9977	0.9999	0.9977	6.59	1.41
180	0.1057	399.1	110.8	0.1649	0.9956	1	0.9956	9.12	1.406
190	0.09974	399.6	111.0	0.1651	0.9972	1	0.9972	7.29	1.41
200	0.09523	400.1	111.4	0.1658	0.9957	1	0.9957	9.01	1.409
210	0.09065	401.9	111.6	0.1661	0.9964	1	0.9964	7.95	1.41
220	0.08675	402.6	111.8	0.1664	0.9967	1	0.9967	7.77	1.409
230	0.08349	404.6	112.4	0.1672	0.9966	1	0.9966	7.61	1.41
240	0.07971	403.8	112.2	0.1669	0.9938	0.9999	0.9938	10.29	1.408
250	0.07644	404.1	112.2	0.1670	0.9952	0.9999	0.9952	9.13	1.41
260	0.07360	404.8	112.4	0.1673	0.9973	0.9999	0.9973	6.62	1.41
270	0.07090	405.3	112.6	0.1675	0.9952	0.9999	0.9952	9.06	1.41

PI controller gains (K_p): 0.0005, (K_i): 0.0021, Buck–boost inductor (L_{bb}): 4 mH, dc link capacitor (C_o): 18 μF, Resonant parameters: - resonant inductor (L_r): 3 mH, dc blocking capacitor (C_b): 45 nF, resonant capacitor (C_p): 3 nF.

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