The International Journal of Advanced Manufacturing Technology (2022) 119:3427–3435
https://doi.org/10.1007/s00170-021-08622-x

ORIGINAL ARTICLE

Application of the surface planer process to Cu pillars and wafer support tape for high-coplanarity wafer-level packaging

Fumihiro Inoue[1] · Alain Phommahaxay[1] · Yohei Gokita[2] · Berthold Möller[2] · Eric Beyne[1]

Received: 18 June 2021 / Accepted: 10 October 2021 / Published online: 7 January 2022

Abstract

We used the surface planer process to minimize the within-die and within-wafer nonuniformity caused by the nonoptimized Cu pillar and Si thinning processes. The height variation of the planarized Cu pillars was 3.5% of the within-wafer uniformity in a 300-mm wafer, which represents a substantial reduction of the post-electrodeposition height variation. In addition, the topography of the Cu pillar surface was flat and uniform after the surface planer process. The backgrind tape-laminated Cu pillar wafer exhibited a total thickness variation of 31.77 μm. This variation was reduced to 14.55 μm by the surface planer process. The bulk Si of the Cu pillar wafer with the planarized backgrind tape was thinned to 100 μm by grinding. The total thickness variation of the Si was 1.52 μm when the backgrind tape was subjected to the surface planer process, whereas it was 8.2 μm in the case where the surface planer process was not applied. These results indicate that the surface planer process is a promising method for achieving high coplanarity of a die and wafer, thereby representing an advancement toward high-yield advanced packaging.

Keywords Surface planer · Grinding · Cu pillar · Packaging electronics · Backgrind tape

1 Introduction

Advanced packaging is becoming a more viable option for high-performance devices. For example, fan-out wafer-level packaging (FOWLP) can fulfill the demand for multifunctionality, increased input/output count, smaller form factors, and cost reduction. However, compared with conventional packaging technologies, FOWLP requires greater coplanarity of the die and wafer [1–3], introducing new obstacles to achieving sufficient coplanarity in the original wafer processing, such as requiring control of the Cu pillar height and the thickness of the Si.

Cu pillar technology is used to connect a device to the redistribution layer or to other devices in advanced packaging and 3D/2.5D integration [3–6]. A Cu pillar is usually formed by electrodeposition during the semi-additive process. The height of a plated Cu pillar is typically a few tens of microns, which means it cannot be planarized by polishing afterward. Therefore, the height uniformity and the surface flatness of the Cu pillar are determined by the Cu electrodeposition process. The height uniformity directly affects the yield of electrical connections of pillars. Nevertheless, the height uniformity can vary if the electrodeposition step is not fully optimized for the pillar structure, which cannot subsequently be adjusted using conventional processes.

The Si bulk removal process plays an equally important role in maintaining the coplanarity of advanced packaging. The Si bulk removal process is usually carried out via a diamond-abrasive grinding process [7]. Si grinding, especially analyses of the removal mechanism, has been investigated for decades [8, 9]. Numerous novel approaches to achieving a high removal rate have recently been reported [10–14]. Nevertheless, further improvements in the thickness variation remain a common challenge in the device manufacturing process. For the Si removal process, minimizing the total thickness variation (TTV) of Si on the die and that of the wafer is also critical for high-accuracy thermal compression bonding, along with die placement on a carrier wafer with temporary glue for epoxy molding [3, 15, 16]. A surface protection system is required

✉ Fumihiro Inoue
inoue-fumihiro-ty@ynu.ac.jp

Alain Phommahaxay
Alain.Phommahaxay@imec.be

[1] Kapeldreef 75, 3000 Leuven, Belgium

[2] Disco Hi-Tec Europe Gmbh, Liebigstrasse 8, 85551 Kirchheim b. Muenchen, Germany

during backside thinning of the wafer [17–20]. Otherwise, the wafer surface will directly contact the chuck of the grinder. Contact between the chuck and the top surface of the wafer can introduce contaminants and mechanical stress onto the front side of the wafer. In addition, the thinned wafer becomes flexible and fragile. Furthermore, the surface topographic features of the wafer surface, such as pillars and microbumps, prevent the wafer from being held by vacuum on the chuck table of the grinding tool. Lamination of the from side using ultraviolet (UV)-releasable backgrind (BG) tape is comprehensively used to provide wafer support during the wafer thinning process. However, the tape tends to follow the surface topography, eventually leading to a large TTV of the wafer and tape. Because coplanarity between the chuck, wafer (workpiece), and wheel is key to maintaining a good TTV of the Si after grinding, the incoming thickness variation of the wafer must be minimized.

In the present study, we introduce a method to minimize the variation of the Cu pillar height and Si thickness using a surface planer process. The creep-feed fly-cut process (i.e., the so-called "surface planer" process) can create submicron-level coplanarity on the cutting surface and wafer bottom via the copying principle of the mechanical machine [21–29]. The manufacturing process with a surface planer was investigated to mitigate both the nonuniformity of the Cu pillar and the TTV of the Si after thinning. For Cu pillar planarization, the plated Cu pillar and the plating photoresist (PR) were planarized simultaneously (Fig. 1a). To control the Si thickness during thinning, the UV-releasable BG tape deformed by the surface Cu pillar was planarized before grinding to mitigate the original topography (Fig. 1b).

2 Experimental details

All wafer-scale processes were carried out using 300-mm Si wafers as the substrate. The original thickness of the Si wafers was 775 µm. The die size in the pillar mask pattern was 5.2 mm × 5.2 mm (2332 active dies in a 300-mm wafer). A passivation layer (50 nm SiN) was deposited onto the Si substrate. A 30 nm TiW barrier layer and a 150 nm Cu conductive seed layer were deposited by physical vapor deposition (PVD). Then, a 60 µm photoresist was coated and patterned onto the PVD Cu seed layer. The critical dimension of the pillars on the photoresist was 50 µm. The open area of the pillar mask in design was 11.69%. The total number of pillars in one die was 1610. After the photoresist was descummed and the Cu seed layer was exposed, Cu was electrochemically deposited onto the exposed area of the photoresist. The plating tool used in the experiment was a vertical wafer holder with an agitation system (Nexx Stratus P300). The Cu chemistry consisted of an acid–base virgin makeup solution containing the Copper Gleam PC additive from DuPont. The current density used for pillar plating was − 20 mA/cm^2. The target height of the Cu was 50 µm.

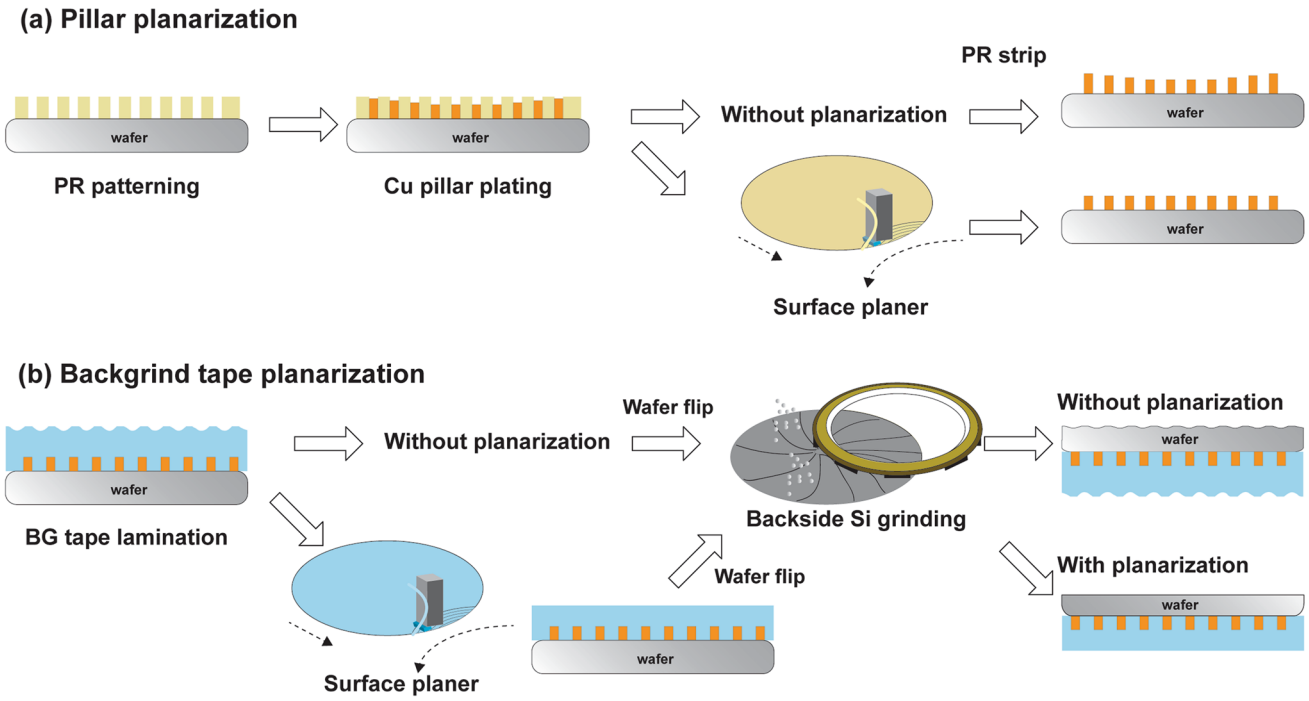

Fig. 1 Schematics of (**a**) Cu pillar planarization and (**b**) backgrind tape planarization

Planarization was carried out using a creep-feed surface planer machine (DAS8930 from Disco). Details of the process conditions and a schematic of the surface planer process are available elsewhere [21]. A diamond single crystal was used for the cutting process. The diamond was fixed onto a shank, and the shank was placed on a spindle. To maintain good balance on the spindle, a dummy shank was placed on the opposite side (180°) of the spindle. The diameter of the spindle was 320 mm. The processed wafer was held face-up on the vacuum chuck table. The cutting sequence consisted of a rough cut (high feed rate) and a final fine cut (low feed rate). The target height of the photoresist and Cu pillar after the planarization was 42 µm. The pillar height was measured using a CAMTEK Falcon 630 Plus optical system. The width of the edge exclusion was 5 mm from the bevel. Surfaces were inspected using a scanning electron microscope and an optical profiler. The photoresist, Cu seed, and TiW on the field were then removed by wet chemical etching. HT-260PG-UR10-PH2 was laminated onto the wafer's front side (pillar side) as the BG tape. The total thickness of the tape was 260 µm, where the base film was 50 µm. The grinding step was carried out using an in-feed abrasive grinder equipped with rough and fine wheels [30–33]. During the grinding process, the BG tape was made to contact the chuck table by a vacuum. The thickness of the Si wafer after grinding was measured by laser interferometry.

3 Results and discussion

3.1 Pillar planarization

In the wafer plating tool, the current is applied and distributed from the wafer edge via the metal contact of the wafer holder. Therefore, the pillar tends to be higher at the wafer edge than at the center. Figure 2a shows the pillar height distribution allocated in the whole wafer map. Immediately after the Cu plating, the mean value of the pillar height was 48.0 µm. The tallest pillar was 57.3 µm high, and the shortest was ~ 42.1 µm. The within-wafer (WiW) uniformity was calculated as follows:

$$WiW[\%] = \frac{H\mathrm{h} - H\mathrm{l}}{H\mathrm{m}} \times 100 \quad (1)$$

where H_h is the 95% highest pillar height, H_l is the 5% lowest pillar height, and H_m is the mean height of all pillars. From this calculation, the WiW uniformity after the plating was 24.6%. Because the plating chamber was not optimized for

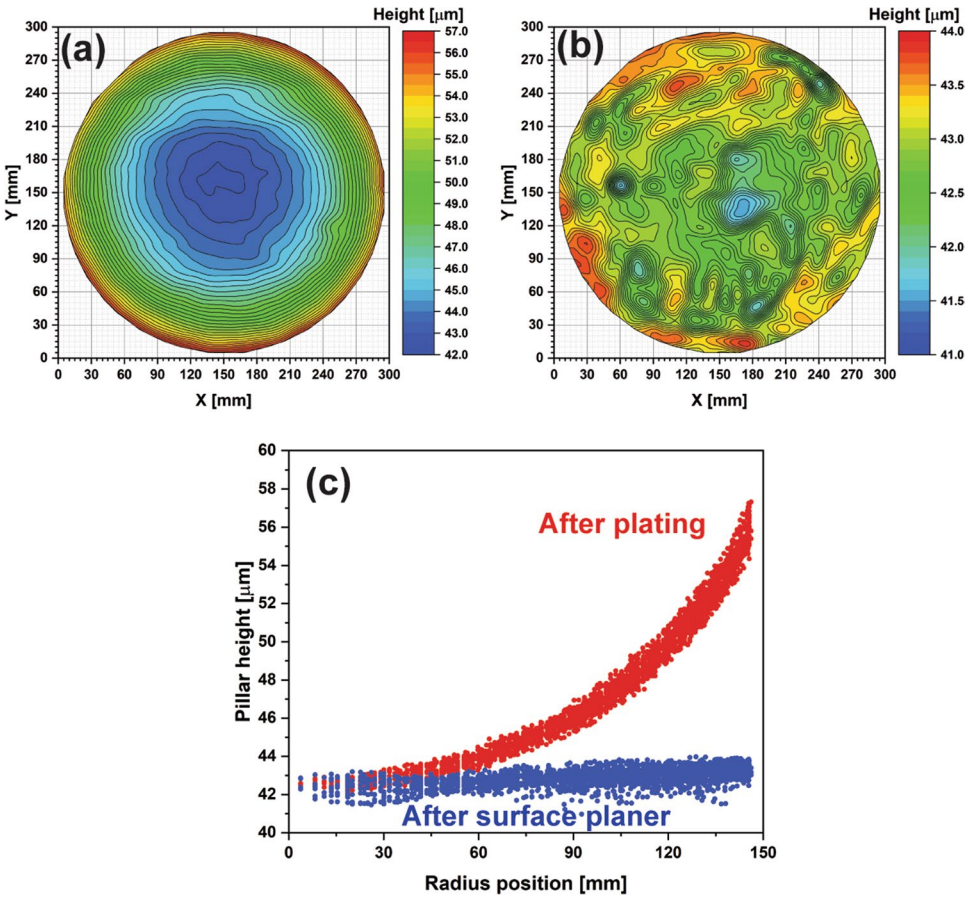

Fig. 2 The Cu pillar height distribution in a 300-mm wafer. The Cu pillar height was extracted as the mean height of a die. (**a**) Wafer map after the plating process. (**b**) Wafer map after the surface planer process. (**c**) Radius distribution after the plating and surface planer processes

the pillar plating, the uniformity exceeded the best performance of the plating tool. After the plating, the hardware, chemistry, anode shield, and agitation were optimized, and the uniformity was < 7%.

The pillar height before and after the surface planer process cannot be measured for the same wafer because the pillar height can only be measured by the optical method after the resist has been stripped. However, if the resist is stripped, the surface planer process will differ from the actual situation. Therefore, the surface planer process was applied to a different wafer obtained from the same lot as the wafer whose height was measured in Fig. 2a. All wafers in a lot were subjected to exactly the same plating process, and the wafers used in the present work were from the same lot. Thus, the pillar height after plating should be equivalent for the wafers in Fig. 2a, b. Figure 2b shows the pillar height distribution allocated in the whole wafer map after the surface planer process. The tallest pillar after the surface planer process was 44.0 µm, and the shortest was 41.0 µm. The WiW uniformity after the surface planer process was 3.5%. The surface planer process was carried out immediately after the plating process, without stripping of the photoresist. That is, the removal process was simultaneously carried out on the photoresist and Cu pillars. Approximately 18 µm of the photoresist was removed by the surface planer process. The amount removed by the fine cut was 1 µm. In a previous study, we found that the photoresist was not a good support material for the planarization of fine-pitch microbumps [21]. However, the dimensions of the pillars in the present study are much larger than those of the microbumps we reported previously [21]. Peeling stress and plastic deformation should occur only at the top of the pillars. Figure 2c shows the pillar height distribution plotted with respect to the radius position of the wafer both after plating and after the surface planer process. The WiW nonuniformity of the pillar height after plating was reduced by the surface planer process; that is, the pillar height was made uniform.

The WiW uniformity strongly influences the subsequent process. In addition, the within-die (WiD) uniformity is an equally important parameter for the packaging process (e.g., for die thermal compression bonding and die placement on the carrier wafer). Therefore, we also calculated the WiD uniformity by measuring all of the pillars in a die before and after the surface planer process. Figure 3 shows a box plot of pillar height coplanarity in a die in a wafer. The coplanarity was obtained by subtracting the highest pillar height from the lowest pillar height in a die. All of the measured dies in a wafer are plotted in the box chart. The mean value of the coplanarity in a die is 1.77 µm, and the standard deviation is 0.75 µm after the plating. The mean value is 1.53 µm, and the standard deviation is 0.64 µm after the surface planer process. In terms of WiD coplanarity, similar results are obtained both after

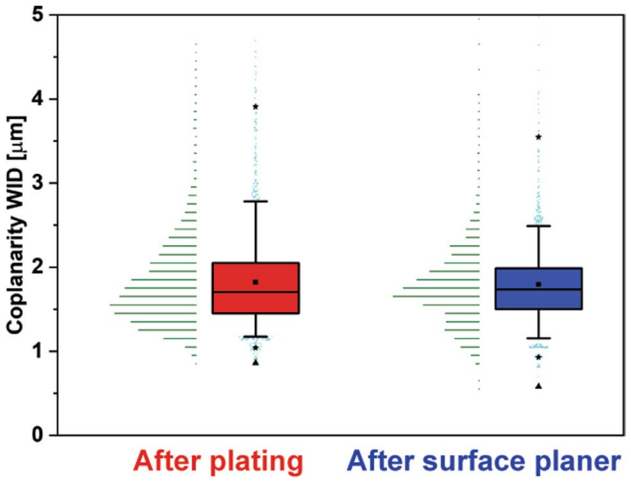

Fig. 3 Box plot of the within-die coplanarity after the plating process and after the surface planer process

the plating and after the surface planer process. The WiD coplanarity after the plating is acceptable for the packaging process. In addition, the surface planer process does not adversely affect the WiD uniformity.

The shape of the pillar might have a negative impact when the dies are stacked. The top surface should be as flat as possible to avoid slippage of the top bump unless the top surface is domed. However, voids may form if the top surface is dish-shaped. Figure 4 shows scanning electron microscopy (SEM) images of the Cu pillars after the photoresist and Cu seed/TiW barrier were removed. No defects or missing bumps are observed on the pillar after the plating (Fig. 4a, b) or after the surface planer process (Fig. 4d, e, respectively). In addition, no deformation of the Cu pillar is observed after the surface planer process. To quantify the shape of the pillar, we observed their top shapes by interferometric microscopy. Figure 4c, f show interferometric images after the plating and after the surface planer process, respectively. The height at the center of the pillar was extracted to calculate the total indicated runout (TIR) (see Fig. 4g, h). The TIR was calculated as:

$$TIR\ [\%] = \frac{Hc - He}{H\max} \times 100 \tag{2}$$

where H_c is the pillar height at the center, H_e is the average height 5 µm from the pillar edge, and H_{max} is the highest point on the pillar. The H_{max} after the plating was 0.93 µm. The TIR after plating was − 1.72%, where the negative value indicates that the top of the pillar after plating was dished at the center. The H_{max} was 0.21 µm. The TIR was − 0.169% after the surface planer process. This result indicates that the surface planer creates a nanometer-scale flat pillar surface, which reduces the risk of yield loss at the stacking.

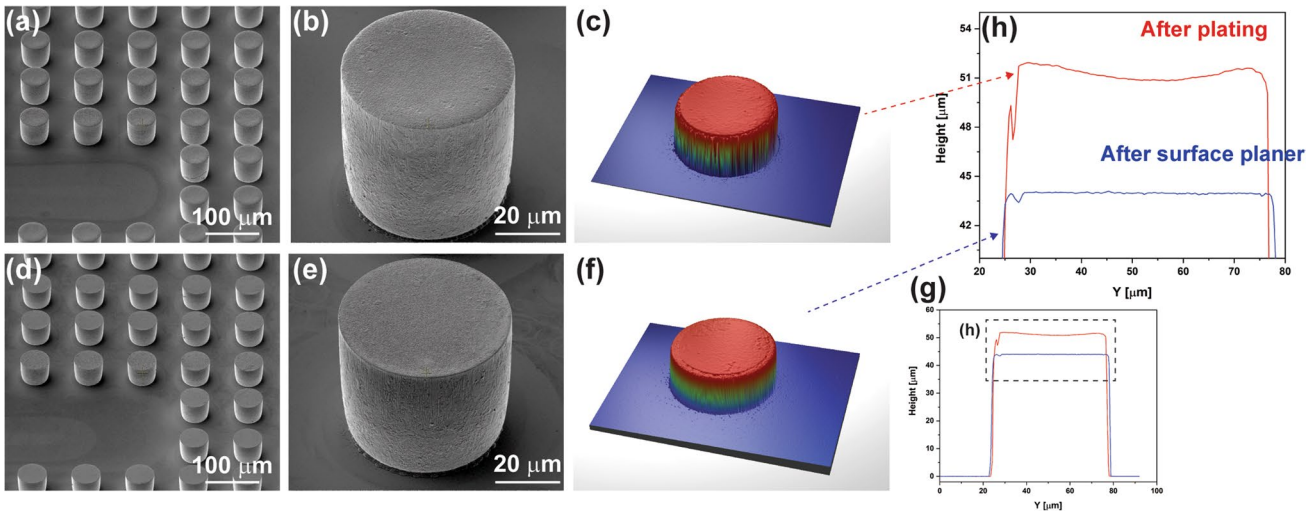

Fig. 4 Inspection results of the Cu pillar before and after the surface planer. (**a**) Tilt-view SEM image at low magnification of the Cu pillars after the plating. (**b**) Tilt-view SEM image at high magnification of a Cu pillar after the plating. (**c**) Interferometric image after the plating. (**d**) Tilt-view SEM image at low magnification of Cu pillars after the surface planer process. (**e**) Tilt-view SEM image at high magnification of a Cu pillar after the surface planer process. (**f**) Interferometric image after the surface planer process. (**g**) and (**h**) The extracted line profiles for a Cu pillar

3.2 Backgrind tape planarization

The wafer surface topography becomes high because of the presence of microbumps and/or Cu pillars, which poses a challenge for the current wafer support system, e.g., UV-releasable BG tape, which cannot maintain a good TTV because of its followability on the surface. To mitigate the variation caused by the followability of the tape on the pillar wafer, the tape side was subjected to the surface planer process. Figure 5a shows a wafer map of the

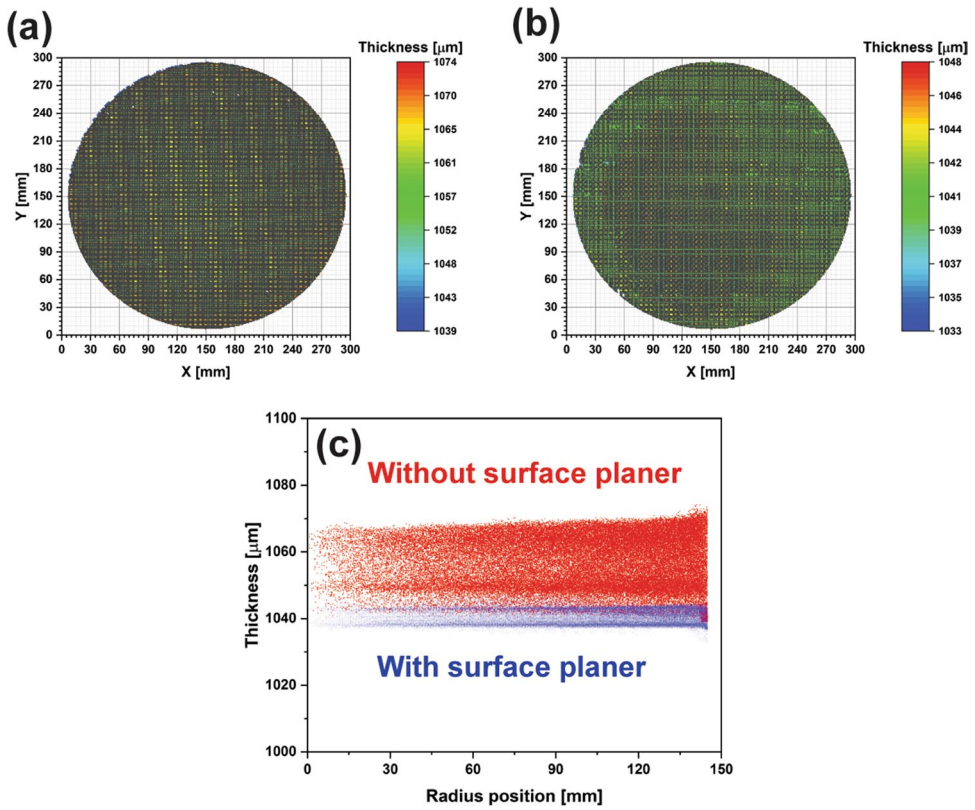

Fig. 5 Total wafer thickness in a 300-mm wafer with a Cu pillar after lamination of BG tape and application of the surface planer process to the BG tape. (**a**) Wafer map after lamination. (**b**) Wafer map after the surface planer process. (**c**) Radius distribution with and without the surface planer process

total thickness after tape lamination of the Cu pillar wafer. Surface-planarized Cu pillars 43 µm in height are observed on the wafer. The sum of the Si wafer and the tape thickness was 1035 µm. However, the measured mean thickness after lamination was 1057 µm because of the pillars on the wafer. The greatest pillar height was 1074 µm at the die center, and the lowest pillar height was 1039 µm at the dicing street. To reduce the TTV, the surface planer process was applied to the tape. The removal amount of the tape was approximately 17 µm. Figure 5b shows a wafer map of the total thickness after the tape was subjected to the surface planer process. The TTV was substantially reduced compared with the post-lamination TTV. Figure 5c shows the total thickness with respect to the radius position before and after the surface planer process. The 90% TTV (5% top and bottom excluded) was 31.77 µm after lamination and was reduced to 14.55 µm after the surface planer process.

A huge peak and valley were formed between the die center and the dicing street after lamination of the tape (Fig. 5). The cross-point of the dicing street in both cases was observed by optical interferometry. Figure 6 shows a tilt view of interferometry at the cross-point of the dicing street at the center. The cross-point of the dicing street exhibits the lowest height because there is no pillar and this point is farthest from the edge of the pillar pattern. After lamination, the *Rz* was 34.4 µm, which is similar to that observed in the wafer-level measurement. After the surface planer process, the surface planer cut lines are clearly observed. The roughness of the surface planer cuts was very small and was negligible compared with the peak and valley of the tape itself. The *Rz* after the surface planer process was 10.1 µm, which is also consistent with the result of the wafer-level TTV.

The backside Si thinning process was applied to the Cu pillar Si wafer with the BG tape. The target thickness of the Si after grinding was 100 µm. These wafers were processed using the same grinding condition, and the same chuck was used for the comparison. Before tape lamination, a 200-µm-deep and 500-µm-wide edge trimming process was applied [34, 35]. Figure 7 shows the Si thickness after grinding. The Si thickness was measured using an infrared laser tool. For the case without a surface planer, the mean thickness of the Si was 100.1 µm after grinding. However, the TTV within 90% of the surface was 8.2 µm. For the case where the surface planer process was applied to the tape, the mean thickness of the Si after grinding was 100.4 µm, and the TTV was 1.52 µm. These results indicate that the surface planer process mitigates the noncoplanarity of the tape after lamination. For the case without the surface planer process, a scattering of approximately 5 µm in the same radius position in the wafer was observed. By contrast, the wafer-level variation was ~ 1 µm for the case with the surface planer process.

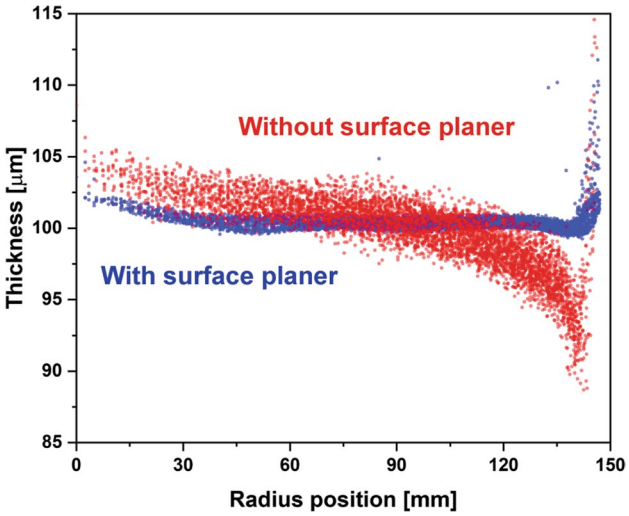

Fig. 7 Si thickness of the Cu pillar wafer after grinding toward 100 µm with and without the surface planer process

Figure 8 shows the die-level Si thickness at the middle of the wafer. In the case with (Fig. 8a) or without the surface planer process (Fig. 8b), the Si thickness at the die center is slightly greater than that at the dicing street because of the presence of the pillar. This greater Si thickness at the die center is attributed to the pillar preventing deformation of Si by vertical pressure during grinding. Figure 8c shows the cumulative frequency graph of the Si thickness in Fig. 8a,

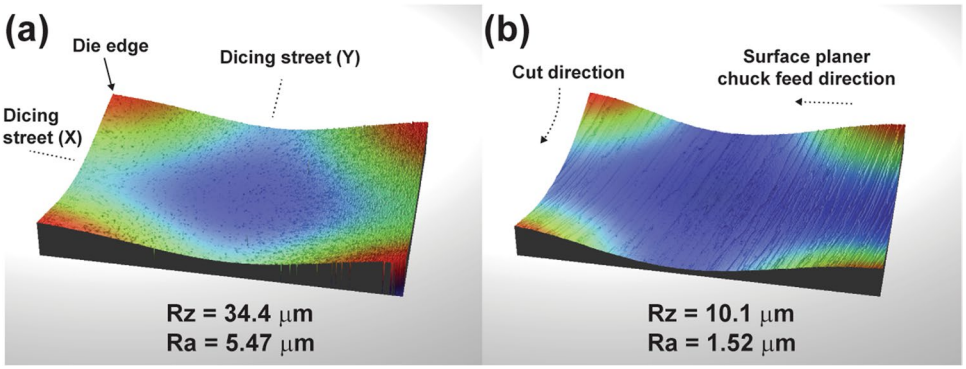

Fig. 6 Interferometric image of the BG tape surface laminated on the Cu pillar wafer. These images were taken at the cross-point of the dicing street (**a**) after lamination and (**b**) after the surface planer process

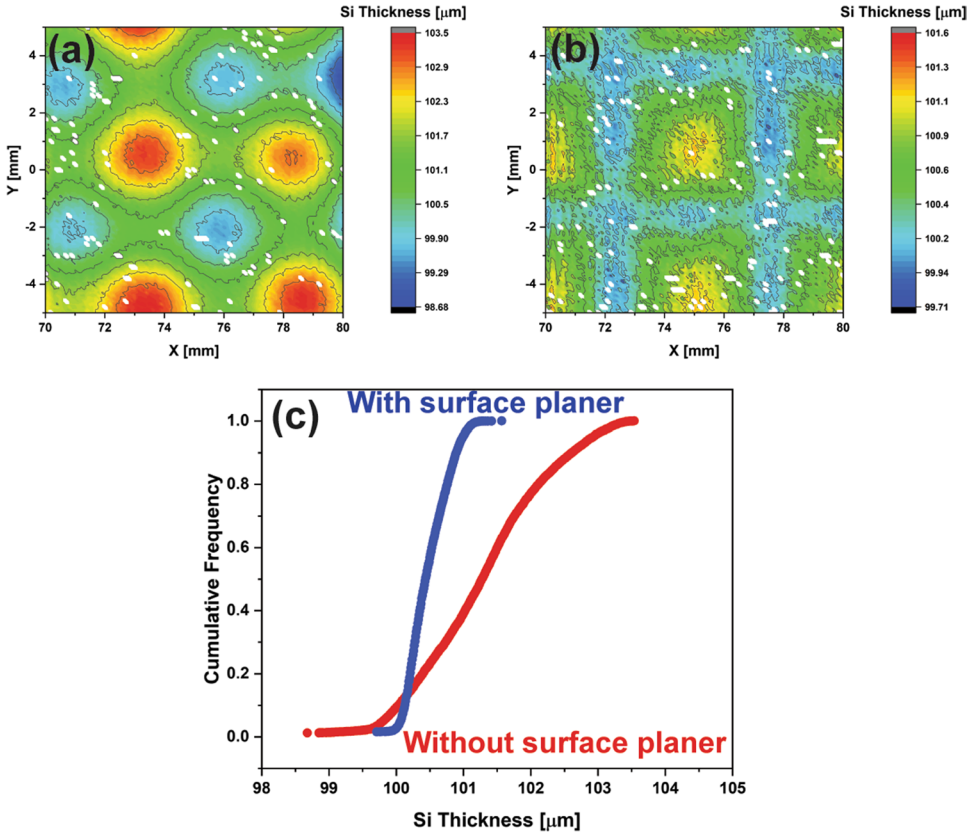

Fig. 8 Local Si thickness of a Cu pillar wafer after grinding toward 100 μm (measurement location *X*: 70 to 80 mm, *Y*: − 5 to 5 mm): (**a**) without the surface planer process and (**b**) with the surface planer process applied to BG tape. (**c**) Cumulative frequency extracted from (**a**) and (**b**)

b. In the case without the surface planer process applied to the tape, the distribution of the Si thickness was wider than 4 μm. However, the distribution of the Si thickness was only 1 μm in the case where the surface planer process was applied to the tape. In either case, the Si TTV after grinding was much smaller than the TTV of incoming total thickness (tape + wafer). This smaller TTV is attributed to the vacuum chuck table of the tool compensating for some of the topography of the tape. However, if the topography is too high, as in the case where the surface planer process was not applied (> 30 μm TTV), compensation is not possible, as evident in the TTV of the Si after the grinding process. For the advanced packaging, the Si thickness variation in a die becomes critical for stacking and molding. The surface planer process applied to the tape can mitigate the TTV of the Si after grinding.

4 Conclusions

We demonstrated planarization of Cu pillars and UV-curable BG tape to control the Cu pillar height and Si thickness of wafers. The planarized Cu pillars exhibited a WiW uniformity of 3.5% on a 300-mm wafer, which requires substantial effort for optimization when only electrodeposition is used. In addition, the planarized Cu pillars exhibited a substantially flatter shape than that after plating. Furthermore, the surface planer process compensated for the topography caused by flowability of the BG tape on the Cu pillar wafer. The TTV after Si thinning toward 100 μm was 1.52 μm. Because high coplanarity of the Cu pillars and Si thickness is required for advanced packaging, achieving wafer-level coplanarity via the surface planer process is advantageous. Thus, the surface planer process can be viewed as a potential alternative planarization process for advanced packaging.

However, the removal mechanism of the surface planer is "cutting", which has certain limitations to obtain atomic-scale flatness or nano-topography with a high throughput process. With further scaling of advanced packaging processes, planarization and its uniformity will continue to remain important. Future improvements in planarization of polymers/metals with high coplanarity will be achieved through a combination of surface planer processes (for bulk removal) and polishing (for surface finish).

Funding This study was supported by the IMEC Industrial Affiliation Program (IIAP). However, the partners had no control over the interpretation, writing, or publication of this work.

Availability of data and material All the data shown in this paper is safely stored and available.

Code availability Not applicable.

Declarations

All authors declare that (i) no support, financial or otherwise, has been received from any organization that may have an interest in the submitted work and (ii) there are no other relationships or activities that could appear to have influenced the submitted work.

Ethics approval Not applicable.

Consent to participate Not applicable.

Consent for publication All authors have agreed.

Competing interests The authors declare no competing interests.

References

1. Che F, Ho D, Ding M, Zhang X (2015) Modeling and design solutions to overcome warpage challenge for fan-out wafer level packaging (FO-WLP) technology. 17th Electronics Packaging Technology Conference, pp 2–8
2. Chang CS, Oscilowski A, Bracken R (1998) Future challenges in electronic packaging. Circuits & Devices, pp 45–54
3. Podpod A, Slabbekoorn J, Phommahaxay A, Duval F, Salahouedlhadj A, Gonzalez M, Rebibis K, Miller RA, Beyer G, Beyne E (2018) A novel fan-out concept for ultra-high chip-to-chip interconnect density with 20-µm pitch. 2018 IEEE 68th Electronic Components and Technology Conference, pp 370–378
4. Srinivasa Rao V, Tai Chong C, Ho D, Mian Zhi D, Ser Choong CS, Lim PS, Ismael D, Yong Liang Y (2016) Development of high density fan out wafer level package (HD FOWLP) with multi-layer fine pitch RDL for mobile applications. 2016 IEEE 66th Electronic Components and Technology Conference, pp 1522–1529
5. Yang Y, Chou T, Yu T, Chang Y, Huang T, Yang K, Ko C, Chen Y, Tseng T, Chen K (2017) Low-temperature Cu–Cu direct bonding using pillar–concave structure in advanced 3-D heterogeneous integration. IEEE Transactions on Components, Packaging and Manufacturing Technology 7:9
6. DeProspo B, Liu F, Nair C, Kubo A, Wei F, Chen Y, Sundaram V, Tummala RR (2018) First demonstration of silicon-like >250 I/O per mm per layer multilayer RDL on glass panel interposers by embedded photo-trench and fly cut planarization. 2018 IEEE 68th Electronic Components and Technology Conference, pp 1152–1157
7. Zihan Dong, Yuanwei Lin (2020) Ultra-thin wafer technology and applications: A review. Mater Sci Semicond Process 105:104681
8. Öztürk S, Kahraman MF (2019) Modeling and optimization of machining parameters during grinding of flat glass using response surface methodology and probabilistic uncertainty analysis based on Monte Carlo simulation. Measurement 145:274–291
9. Kahraman MF, Öztürk S (2019) Experimental study of newly structural design grinding wheel considering response surface optimization and Monte Carlo simulation. Measurement 147:106825
10. Zhang Z, Wanga B, Kang R, Zhang B, Guo D (2015) Changes in surface layer of silicon wafers from diamond scratching. CIRP Ann Manuf Technol 64:349–352
11. Zhang Z, Huo F, Zhang X, Guo D (2012) Fabrication and size prediction of crystalline nanoparticles of silicon induced by nanogrinding with ultrafine diamond grits. Scripta Mater 67:657–660
12. Wang B, Zhang Z, Chang K, Cui J, Rosenkranz A, Yu J, Lin C-T, Chen G, Zang K, Luo J, Jiang N, Guo D (2018) New deformation-induced nanostructure in silicon. Nano Lett 18:4611–4617
13. Zhang Z, Guo D, Wang B, Kang R, Zhang B (2015) A novel approach of high speed scratching on silicon wafers at nanoscale depths of cut. Sci Rep 5:16395
14. Zhang Z, Huang S, Wang S, Wang B, Bai Q, Zhang B, Kang R, Guo D (2017) A novel approach of high-performance grinding using developed diamond wheels. Int J Adv Manuf Technol 91:3315–3326
15. Inoue F, Jourdain A, De Vos J, Sleeckx E, Beyne E, Patel J, Ansell O, Ashraf H, Hopkins J, Thomas D, Uedono A (2016) Characterization of extreme Si thinning process for wafer-to-wafer stacking. 2016 IEEE 66th Electronic Components and Technology Conference, pp 2095–2102
16. Phommahaxay A, Suhard S, Bex P, Iacovo S, Slabbekoorn J, Inoue F, Peng L, Kennes K, Sleeckx E, Beyer G, Beyne E (2019) Enabling ultra-thin die to wafer hybrid bonding for future heterogeneous integrated systems. 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), pp 607–613
17. Phommahaxay A, Potoms G, Verbinnen G, Sleeckx E, Beyer G, Beyne E, Guerrero A, Bai D, Liu X, Yess K, Arnold K, Spiess W, Griesbach T, Rapps T, Lutter S (2016) Extremely low-force debonding of thinned CMOS substrate by laser release of a temporary bonding material. 2016 IEEE 66th Electronic Components and Technology Conference, pp 1685–1690
18. Gurnett K, Adams T (2006) Ultra-thin semiconductor wafer applications and processes. III-Vs REVIEW THE ADVANCED SEMICONDUCTOR MAGAZINE 19(4):38–40
19. Christian B, Bacquian S, Gomez F (2019) A study of wafer backgrinding tape selection for SOI wafers. J Eng Res Rep 6(2):1–6
20. Christian B, Bacquian S, Gomez F (2020) Effect of backgrinding tape lamination on die alignment. Journal of Engineering Research and Reports 14(4):1–4
21. Inoue F, Derakhshandeh J, Lofrano M, Beyne E (2021) Fine-pitch bonding technology with surface-planarized solder microbump/polymer hybrid for 3D integration. Jpn J Appl Phys 60:026502
22. Suzuki Y, Hichri H, Wei F, Sundaram V and Tummala R (2017) Embedded trench redistribution layers at 2– 5 µm width and space by excimer laser ablation and surface planer processes for 20–40 µm I/O pitch interposers. IEEE Transactions on Components, Packaging and Manufacturing Technology 7(6):838–845
23. Zhang W, Limaye P, Agarwal R, Soussan P (2010) Surface planarization of Cu/Sn micro-bump and its application in fine pitch Cu/Sn solid state diffusion bonding. 2010 IEEE 12th 2010 12th Electronics Packaging Technology Conference (EPTC), pp 143–146
24. Zhang SJ, Tob S, Zhu ZW, Zhang GQ (2016) A review of fly cutting applied to surface generation in ultra-precision machining. Int J Mach Tools Manuf 103:13–27
25. Agarwal R, Pham N, Cotrin R, Andrei A, Ruythooren W, Iker F, Soussan P (2009) Diamond bit cutting for processing high topography wafers. 2009 11th Electronics Packaging Technology Conference, pp 267–271
26. Liu C, Hirano H, Froemel J, Tanaka S (2017) Wafer-level vacuum sealing using AgAg thermocompression bonding after fly-cut planarization. Sensors and Actuators A 261:210–218
27. Hsiang-Yao H, Ho S-W, Siak Boon Lim S, Leong Ching W, Ser Choong C, Lim S, Siang P, Yong H, Tai Chong C (2019) Ultra-thin FO package-on-package for mobile application. 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), pp 21–27
28. Sakai T, Imaizumi N, Sakuyama S (2016) Hybrid bonding technology with CU-CU/adhesives for high density 2.5D/3D

integration. 2016 Pan Pacific Microelectronics Symposium (Pan Pacific)
29. He R, Fujino M, Akaike M, Sakai T, Sakuyama S, Suga T (2017) Combined surface activated bonding using H-containing HCOOH vapor treatment for Cu/adhesive hybrid bonding at below 200 °C. Appl Surf Sci 414:163–170
30. Inoue F, Jourdain A, Peng L, Phommahaxay A, De Vos J, June Rebibis K, Miller A, Sleeckx E, Beyne E, Uedono A (2017) Influence of Si wafer thinning processes on (sub)surface defects. Appl Surf Sci 404:82–87
31. Inoue F, Podpod A, Peng L, Phommahaxay A, June Rebibis K, Uedono A, Beyne E (2020) Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer. J Manuf Process 58:811–818
32. Yang Y, De Munck K, Teixeira RC, Swinnen B, Verlinden B, and De Wolf I (2008) Process induced sub-surface damage in mechanically ground silicon wafers. Semicond Sci Technol 23:7
33. Pei ZJ, Fisher GR, Liu J (2008) Grinding of silicon wafers: a review from historical perspectives. Int J Mach Tools Manuf 48(12–13):1297–1307
34. Inoue F, Jourdain A, Visker J, Peng L, Moeller B, Yokoyama K, Phommahaxay A, June Rebibis K, Miller A, Beyne E, Sleeckx E (2017) Edge trimming for surface activated dielectric bonded wafers. Microelectron Eng 167:10–16
35. Inoue F, Jourdain A, Peng L, Phommahaxay A, Kosemura D, De Wolf I, June Rebibis K, Miller A, Sleeckx E, Beyne E (2018) Edge trimming induced defects on direct bonded wafers. J Electron Packag 140(3):031004