Int J Adv Manuf Technol (2016) 84:249–260
DOI 10.1007/s00170-015-7803-x

ORIGINAL ARTICLE

A new approach for data processing in supply chain network based on FPGA

Xiaofu Zou[1] · Fei Tao[1] · Penglong Jiang[2] · Shixin Gu[1] · Kan Qiao[3] · Ying Zuo[1] · Lida Xu[4]

Received: 21 May 2015 / Accepted: 2 September 2015 / Published online: 11 September 2015

Abstract With the development of the supply chain network (SCN) and big data processing, a simple view at above two technologies separately has become unadvisable; this mainly reflected on the growing amount of data in the SCN nodes. Since the data processing is not timely, the potential risks may spread like dominoes to the entire network. There are many small nodes in the SCN, in which it requires data processing equipment that have characteristics of high integration and miniaturization. For the phenomenon that large shape and real-time shortage exists in designing underlying data processing equipment in SCN with the traditional special large computers and general embedded processor, this paper considering the advantage of parallel character of FPGA (field programmable gate array), a new method, which uses FPGA to design embedded device to execute related algorithms in parallel for underling data processing to reduce risks which caused by time-delay in SCN, is proposed. To verify effectiveness of the proposed method, a FPGA-based design method for Kalman filter algorithm and median filter algorithm is proposed. The performance and advantage of the proposed method are analyzed by comparing with traditional methods. The results shown that the proposed method have high real-time and accuracy in complex algorithm execution for SCN underling data processing, which can reduce the potential risk and improve the performance of entire SCN.

Keywords Supply chain network (SCN) · Risk · Field programmable gate array (FPGA) · Kalman filter · Median filter · Real-time · Big data

✉ Xiaofu Zou
windyfuzi5311@163.com

Fei Tao
ftao@buaa.edu.cn

Shixin Gu
15652915869@163.com

Ying Zuo
zuoying226@126.com

Lida Xu
lxu@odu.edu

[1] School of Automation Science and Electrical Engineering, Beihang University, Beijing 100191, China

[2] Beijing Aerospace Automatic Control Institute, Beijing 100854, China

[3] Google Kirkland, Kirkland, WA 98033, USA

[4] Old Dominion University, Norfolk, VA 23529, USA

1 Introduction

With the progress of society, the development of traditional commodity exchange is facing many bottlenecks; one of them is how to build an effective network which combines with raw materials, intermediate products, final products, suppliers, manufacturers, distributors, and users thatbecome a problem which must be solved. The emergence of supply chain network (SCN) and its development is a potential effective approach to solve the above issue. By using SCN, the information flow, logistics, funds, and enterprise management can be effectively controlled. In recent years, SCN has been rapidly developed and widely applied, and the typical cases are Boeing and Apple. Boeing can reasonably and dynamically select parts suppliers by using SCN to guarantee aircraft's normal production. Apple can guarantee phone's normal production and sales when parts of suppliers encounter various emergencies by SCN management. So studying SCN not only has theoretical significance but also has great social value.

With the development of society, big data era has come, as McKinsey said "data has penetrated into every area of today's industries and business functions, and has become an important production factor." Whether the internet of things (IoT), cloud computing (CC), enterprise information system (EIS), or SCN,

data is the foundation; we can extract useful information from these data, so the key is how to correctly handle these data. Li et al. [1] firstly briefly introduced the concept, characteristics, and applications of "big d," and then discussed the existing applications and potential applications of big data in PLM (product lifecycle management). Lu et al. [2] researched the efficient and privacy-preserving computing in big data era; the article pointed out that if data are not authentic, new mined knowledge will be unconvincing. Gu et al. [3] researched the cost minimization for big data processing and pointed out that big data services is the tight coupling between data and computation. Xu et al. [4] discussed the information security in big data and studied privacy preserving data mining (PPDM). Slavakis et al. [5] discussed modeling and optimization for big data analytics. Liu et al. [6] discussed the issues and challenges of big data development in China.

At the same time, supply chain network (SCN) is continuously expanding; accompanying this change, the amount of data in SCN is increasing with a fast speed. There are more and more data has to be processed in a small node in SCN. As a result, the risks in SCN will increase if the data cannot be processed timely. What's more, the risks will be like a domino and quickly threat to entire network from small network node. There are many scholars that have carried out related studies about risks reduce of big data; Lu et al. [7] firstly researched the security issues in ICT (Information and Telecommunication) supply chain, and then several international models both on physical supply chain and ICT supply chain were introduced. Robak et al. [8] studied the capabilities of big data technology architectures with cloud computing in SCN and then introduce a process case. Zage et al. [9] proposed a method which using big data to improve the security of SCN and related literature survey and system tutorial for big data analytics platforms have been researched in literature [10]. Risk intelligence in big data era is a big topic, the research priority of this paper is using a new method to deal with underlying data in SCN, and the aim is to improve the real-time of data processing to reduce the risks which caused by time-delay processing.

Recently, a lot of works have been carried out on SCN, such as network risk analysis, network evaluation, and optimization. However, as the bottom of SCN, data collection and processing have not been paid full attention. How to ensure the correctness and effectiveness of data collecting and processing at the bottom layer of SCN is a key issue which relates to the further development of SCN. Many scholars study SCN from a macro level, such as policy level, high-level resource optimal scheduling, and so on. However, any network, including SCN, is constructed by various nodes. It is well known that there are many embedded devices that are deployed in these nodes of SCN and used for data collection and processing. The real time of data processing will directly affect the safety of SCN. In most cases, these devices were designed by DSP (digital signal processor) technology, but DSP is usually in serial mode when it executes the program codes; it will increase risk in SCN by reducing real time of data processing. So we need to look for a parallel computing method to design related algorithms in SCN to improve its real time. For example, there is an issue of image filtering when acquiring a product's label; if filtering is not in real time or has no error, then the risks will be like a domino, quickly threatening the entire network from small network node. The traditional methods to carry out image filtering are using general-purpose processor, such as DSP. Due to its own constraints, for example, it will be in serial mode when it executes program codes. That is to say, codes will be executed in order, so this serial mode seriously affected the real time of data processing. Meanwhile, these embedded devices in SCN pursuit miniaturization, so the computer cannot perform competently. FPGA (field programmable gate array) is an effective method to solve real time of data processing because of its parallel execution characteristics. FPGA's interior is like a "white paper," chip is composed by thousands of logic gates, and user completes program by wire these dispersive logic gates. FPGA jumps from serial mode to parallel execute program, and different parts of user's program can generate different hardware circuits; these different hardware circuits can be independent with each other.

This paper studies a method at the micro level to improve the data preprocessing performance in SCN. Using the parallel technology of FPGA to design filter in the SCN, such as filtering the image noise data, this can improve real time of underlying data processing, and further improve the performance of the SCN.

The rest of this paper is organized as follows. Section 2 reviews the related work in SCN. Section 3 introduces the proposed method and its implementation. Simulation and experiment are carried out in Section 4. Section 5 concludes this paper.

2 Literature review

2.1 Supply chain network

This section surveys modeling, topology, performance analysis, and application of SCN and focuses on underlying embedded device and data processing method in SCN.

2.1.1 Modeling and topology of SCN

Tu and Piramuthu [11] developed a decision support model to support timely processing and filtering for data collected by RFID. Liu and Hipel [12] proposed a hierarchical decision model to select quality-control strategies for a complex product. Lau et al. [13] established a SCN model based on agent to support distributed scheduling. Kelepouris et al. [14] proposed a model that uses the data provided by tracking systems to deliver enhanced tracking information to the final user. Zhao et al. [15] studied how different network topologies, which are created from different growth models, affect the network's resilience against both random and targeted disruptions. Wang and Hu [16]

analyzed topology on value creation of logistics financial management in SCN. The SCN has also been studied in some advanced manufacturing system such as manufacturing grid and cloud manufacturing to enhance the manufacturing resource and service sharing. For example, Tao et al. [17] proposed a manufacturing grid resource service composition and optimal-selection method based on the principles of particle swarm optimization (PSO). A parallel method for service composition optimal-selection in cloud manufacturing system was studied by Tao et al. [18]. In addition, another researches about cloud manufacturing, cloud computing, and internet of things (IoT) can be seen in references [19–29].

2.1.2 Supply chain performance analysis

Jazemi et al. [30] declared that optimizing the whole SCN performance is a key success factor in forming long-term relationships in SCN, and proposed a method by using information sharing benefits to study SCN benefit in supplier selection problem. A fuzzy logic-based approach and a hybrid dynamic framework for supply chain performance (SCP) analysis and management were proposed by Agami et al. [31, 32]. Wu et al. [33] discussed a maxi-min efficiency multi-stage supply chain model which is capable of measuring supply chain members performance and overall SCP.

2.1.3 Application of SCN

SCN has been widely used in many fields. For example, Chan [34] summarized recent trends of SCN both in research and applications. Hill et al. [35, 36] studied the application of SCN in food. Cunningham et al. [37, 38] investigated the application of SCN in industry field. Wu et al. [39, 40] researched supply chain logistics in iron, steel enterprise, and cost management. In addition, many researchers carried out some works on the application of SCN in manufacturing, e.g., Kumar and Mishra [41] studied a multi-agent self-correcting architecture for distributed manufacturing supply chain.

2.1.4 Underlying embedded device and data processing in SCN

As mentioned above, the theory and method of modeling, topology, performance analysis, and application of SCN have been studied by researchers. Any network not only includes SCN superstructure but also includes underlying data processing unit. If one wants SCN to have a good entirety performance, underlying data processing unit must be well constructed. Since data is processed by embedded device, more attention should be paid on the design of embedded device.

To some extent, the development of RFID technology represents the development of SCN nowadays, and research to RFID has also been paid wide attention by many scholars. For example, Gaukler [42] presented a model to evaluate the impact of an introduction of item-level RFID in a retail environment where stock-out-based substitution is common. Ondemir et al. [43] studied an advanced repair-to-order and disassembly-to-order model to deal with the products that are embedded with sensors and RFID tags, and its aim was optimal end-of-life management in closed-loop supply chains using RFID and sensors. Chalasani and Boppana [44] focused on data architectures of RFID transactions. Lee et al. [45] has given out an efficient method which uses a path encoding scheme to processing RFID data. Piramuthu [46] discussed the effect of lightweight cryptographic authentication in RFID-tagged systems. Hsu et al. [47] discussed the way to use enterprise databases, wireless sensor networks, and RFID systems to complete enterprise collaboration.

From the above investigation, it is evident that many scholars pay more attention on the upper strata of SCN, such as using certain strategies to optimize modeling, topology, and performance of SCN. Even for aspect of underlying embedded device and data processing in SCN, they are more concerned about RFID's application, not device's improvement. RFID commonly uses serial processor, such as a single-chip microcomputer (SCM), DSP, or ARM. Admittedly, we have to admit they have some advantages in some ways, but in the face of massive data processing, FPGA, which is born with parallel characteristics, will have excellent performance. If underlying data in SCN does not get good processing, the risks will quickly step-by-step threat to the entire network; at that time, they adopt various optimize methods to improve SCN's performance as mentioned above which will be meaningless. So underlying data processing in SCN is very important and it is this paper's research focus.

2.2 SCN risk analysis and its solution approaches

The researches and applications of SCN greatly promote the development of society. But we have to admit that there are many risks in SCN. Fortunately, these risks have attracted scholars' attention, and a lot of works have been done for risk analysis. For example, Olson [48] mentioned that international trade is the access to lower cost production opportunities through outsourcing, but according to supply partners, there are many potential risks, such as tsunamis, earthquakes, political unrest, and economic turbulence.

The risks in SCN are caused by many reasons which can be classified into the following two aspects:

1. Internal factors. For example, logistics operation risk, the difference between enterprise culture, production and procurement risk, etc.
2. External factors. For example, policy risk, law risk, market demand uncertainty risk, unexpected disaster risk, etc.

Wang et al. [49] focused on reducing risks in location decisions and proposed a two-stage fuzzy facility location problem with value-at-risk (VaR). Shen et al. [50] discussed the performances of markdown money policy (MMP) in fashion supply chains with a risk-averse supplier. Zhang et al. [51] proposed an interactive decision support method for measuring risk in a complex SCN. Groza and Murvay [52] studied efficient protocols for secure broadcast in controller area networks. A comprehensive method for assessing the risk of timing failure by evaluating the software design has been proposed in [53]. Lao et al. [54] investigated decision support system for food receiving operations assignment based on RFID. With more and more complex of SCN, data interaction between network notes becomes more and more frequently, and the following question is how to guarantee the real time of data interaction. In order to answer the question, Wang and Gopalakrishnan [55] proposed a real-time crossbar switch design to improve the real time in industrial control systems. LoBello and Toscano [56] investigated an adaptive approach for topology management in large and dense real-time wireless sensor networks. Neghab et al. [57] discussed integrated risk analysis method and suggested a process to combine quantitative risk analysis. Lazzerini and Mkrtchyan [58] given out a framework to analyze risks using E-FCMs (extended fuzzy cognitive maps). Meanwhile, the threat of uncertainty elements in power systems was a hotspot of research [59].

Many scholars have studied various methods to solve risks in SCN as mentioned above, and many achievements have been achieved. But after analysis, it if found that the above solutions do not consider the risk from bottom of SCN. For example, if underlying sensor data is not properly collected and timely processed, then the wrong data will cause other executive agencies to make a wrong action. Similarly, an inferior product will not be eliminated by image recognition technology if the image processing algorithms are not timely executed. If the risks like the abovementioned emerge, it will be like a domino quickly threatening the entire network from underlying network node and will cause other risks. So this paper pays full attention on underlying data correction and timely processing to reduce the risks which caused by time-delay and wrong processing.

2.3 FPGA technology and its potential in SCN

With the rapid development and application of SCN, a lot of data is generated. Therefore, the effective and real-time data processing method to these data is especially important. At the same time, DSP technology is widely used in many fields including SCN. For example, Kazmierkowski et al. [60] used DSP to develop and implemented direct power control with space vector modulation (DPC-SVM) algorithm to improve the real-time operated DPC-SVM scheme. Mastromauro et al. [61] discussed control issues in single-stage photovoltaic systems (PVS) and used DSP to design controller to control current/voltage in PVS. Nabulsi and Dhaouadi [62] presented a new digital control scheme for a standalone photovoltaic (PV) system using fuzzy-logic and a dual maximum power point tracking (MPPT) controller, and then used DSP to validate the proposed control scheme performance. But in the above method by using DSP, it is in serial mode when program codes are executed, which results in its real time and cannot be guaranteed. Therefore, parallel method is required and studied.

FPGA (field programmable gate array) is a chip technology between ASIC (application specific integrated circuit) chip and general-purpose chip. The development of FPGA has a great difference with computer (both Von Neumann and Harvard architecture) and SCM (single-chip microcomputer). There are many logic resources in FPGA; we program directly to form hardware circuit by combining these logic resources before FPGA running. Parallel characteristic of FPGA is an effective technical method to improve the real time of data processing at the bottom of SCN. Therefore, many scholars are studying the applications of FPGA. The application of FPGA technology to industrial control systems [63, 64] is one of the hot topics. FPGA is usually used to control the PWM wave in electric drive and power electronics systems [65], so as to build a SoC (system on a chip) [66] and designed fuzzy logic controller [67]. From investigation, one can notice some advantages of FPGA as a logic controller. But the advantage of FPGA in dealing with complex algorithm to reduce risks which caused by time-delay in some small nodes so as to improve the whole performance of SCN has not been paid full attention.

For example, image processing for product label discrimination is a necessary part of SCN, and filtering is an important part in the image processing algorithm. At present, Kalman filter and median filter are widely used in filtering field and also attracted many scholars' interest [68, 69].

In this paper, a doubt has been proposed: since there have many risks which caused by time-delay at the bottom of SCN and FPGA has great ability in parallel computing, so why not combine the risks reduction and FPGA? This paper's main goal is to design Kalman filter and median filter based on FPGA and to verify FPGA has great advantage in algorithm parallel design by comparing with DSP and Matlab; at last, a new method has been put forward to reduce some risks in SCN which using FPGA to design embedded device in the bottom of SCN to parallel execute related algorithm to improve its real time.

3 The proposed method and its implementation

This section uses FPGA-based parallel technology to design underlying processing unit of data filter in SCN and uses cases

and simulation experiments to illustrate the advantages of this technology. This will avoid some risks which are caused by time-delay of data processing in SCN. This paper completes Kalman filter and median filter based on Matlab, DSP, and FPGA and does contrastive analysis at last.

3.1 FPGA-based parallel computing

FPGA (field programmable gate array) is a chip technology, and the principal difference from other general-purpose chips (such as ARM, DSP) is its implementation of user's program. In FPGA, the user codes are written into the chip before it works, and then it combines these thousands of FPGA internal logic gates. Finally, these logic gates form fixed hardware circuits which follows the users' intentions. These hardware circuits are the performance of user program. But other chip technologies (such as ARM, DSP) is initially translating user's code section into machine language through CPU, and then it turns the result into hardware circuits and executes these codes at last. Adjacent codes are executed in order. So the process of FPGA's executing codes only needs combining these electrical logic gates at first, and then the "thoughts" of the user are realized in FPGA, so it dos not need to translate users' codes when the chip is running. Since FPGA has such a function, it can execute user codes in parallel. If there is no communication between two codes, these two codes can be executed completely independently; if there is data communication between them, they only need to wait for each other's sync signal after performing separately. In conclusion, we can say that FPGA has higher real-time performance than general-purpose processing chip with serial implementation even if it needs sync signal (Fig. 1).

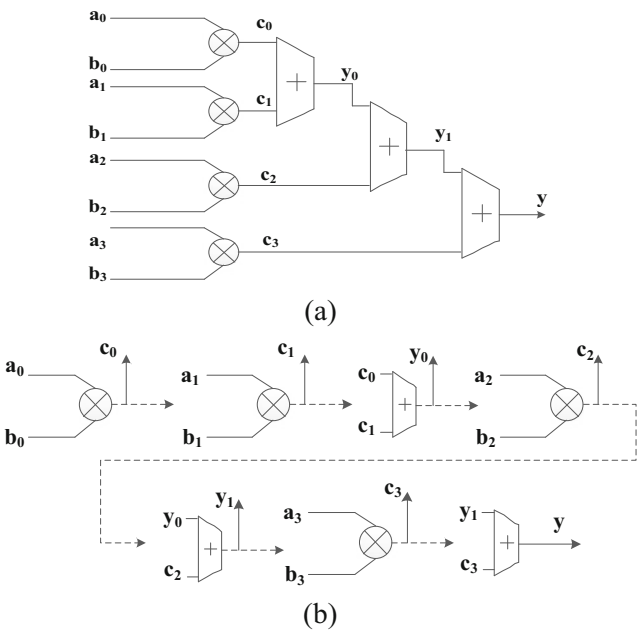

Fig. 1 FPGA parallel computing schematic

The above picture shows how the function $y=a_0*b_0+a_1*b_1+a_2*b_2+a_3*b_3$ is executed in FPGA and other processor (such as DSP). FPGA carries out the function in parallel mode that is shown in picture (a), which is carrying out a_0*b_0, a_1*b_1, a_2*b_2, and a_3*b_3 in parallel within the first clock period. There is just need of three clock cycles at minimum to complete the function's operation for FPGA.

But other processors (such as DSP) execute above formulas in a serial manner that is shown in picture (b): (1) calculate a_0*b_0, (2) calculate a_1*b_1, (3) calculate $a_0*b_0+a_1*b_1$, (4) calculate a_2*b_2, (5) calculate $a_0*b_0+a_1*b_1+a_2*b_2$, (6) calculate a_3*b_3, and (7) calculate $a_0*b_0+a_1*b_1+a_2*b_2+a_3*b_3$. Therefore, there is a need of seven clock cycles at least to complete the function's operation for DSP, and its execution time is two times more than FPGA. So we can say that FPGA has a born ability in algorithm parallel designing.

3.2 FPGA-based design Kalman filter algorithm

This paper uses FPGA and Kalman filter to prove its advantage in complex algorithm parallel design and the value of FPGA-based design underlying data processing unit in SCN, namely reduce the potential risks in the whole network in micro-level.

Kalman filter is widely used in industry, it is an optimal recursive filtering algorithm based on the state-space domain formula. The algorithm can be divided into time update and measurement update.

$$\hat{X}_{k/k-1} = \Phi_{k,k-1}\hat{X}_{k-1} \tag{1}$$

$$P_{k/k-1} = \Phi_{k,k-1}P_{k-1}{\Phi^T}_{k,k-1} + \Gamma_{k-1}Q_{k-1}{\Gamma^T}_{k-1} \tag{2}$$

$$K_k = P_{k/k-1}H_k^T\left(H_kP_{k/k-1}H_k^T + R_k\right)^{-1} \tag{3}$$

$$\hat{X}_k = \hat{X}_{k/k-1} + K_k\left(Z_k - H_k\hat{X}_{k/k-1}\right) \tag{4}$$

$$P_k = (I - K_kH_k)P_{k/k-1} \tag{5}$$

Formula (1) and (2) are time update formula, and the others are measurement update formula. When using Matlab and other general chips (DSP) to realize above formulas, they are converted into codes step by step and the processor executes it step by step, which largely lowered execution efficiency. Now, the normal way to solve this problem is to increase clock frequency of the general chip. But subject to the manufacturing process, the clock frequency cannot be raised unlimitedly. Meanwhile, using advanced chips will increase the cost of network. Aiming at solving these problems, using FPGA to design complex algorithm is a good choice. Divide the complex algorithm into different paragraphs and execute in parallel mode in FPGA, the problems will be better solved. If data communication is needed between these paragraphs, they only need to wait for each other's sync signal after completing their

own operations. This parallel processing method not only can increase the real time of data processing and decrease system risks but also can lower system costs.

In this paper, we analyze the five formulas of Kalman algorithm firstly, and then we find that these five formulas can be parallel executed, although they look like a serial mode. Namely the above five formulas are executed in parallel and do data synchronous among each other (Fig. 2).

The above picture (a) shows the five formulas' serial execution in general purpose processor (like DSP), and picture (b) shows the five formulas' parallel execution in FPGA.

This paper also uses FPGA to design square root Kalman filter algorithm (improved version of classical Kalman algorithm). As shown in Fig. 3a, round error accumulation in filter iterative calculation will let P_k and $P_{k/k-1}$ lose non-negative definiteness, and result in calculating distortion of K_k, and finally make the filter unable to converge. As shown in Fig. 3b, square root Kalman filter uses matrix D of covariance matrix P's square root to take part in iterative calculation,

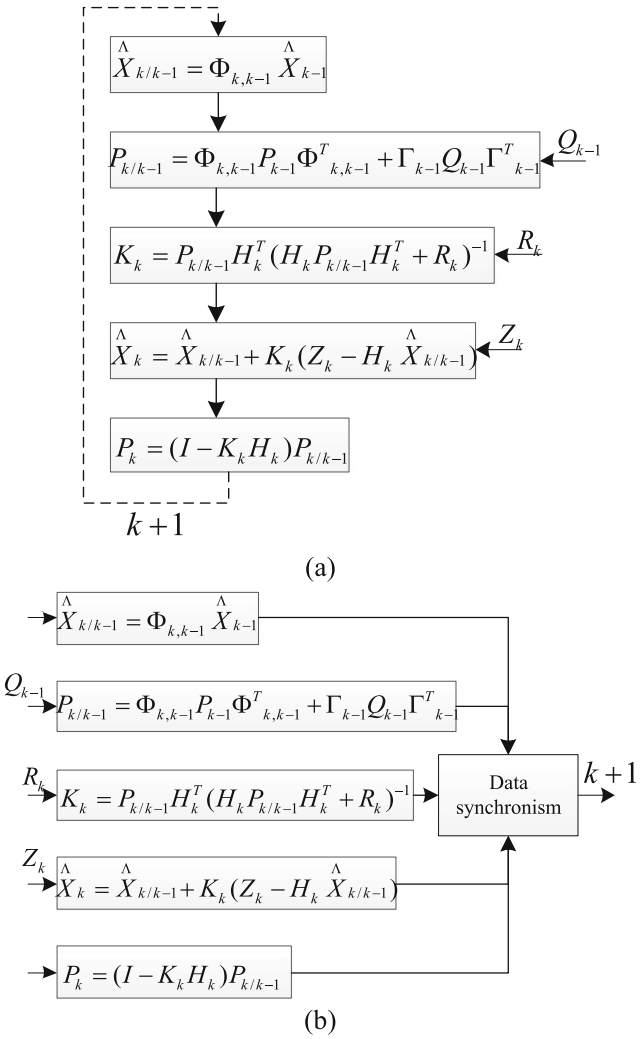

Fig. 2 Kalman filter algorithm serial and parallel execution

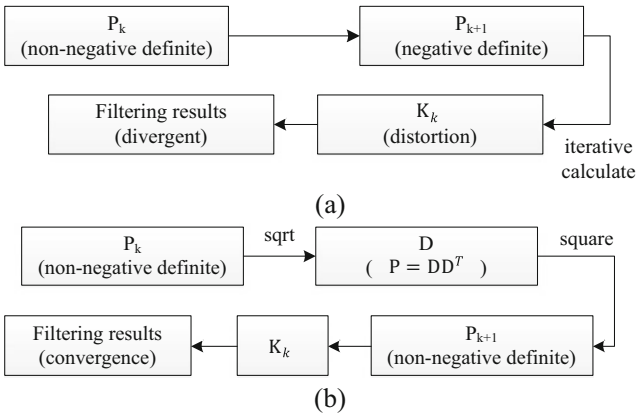

Fig. 3 Kalman filter's problems and square root filter schematic

which can ensure the non-negative qualitative of covariance matrix P.

3.3 FPGA-based design median filter algorithm

As we know, median filtering algorithm is widely used in image filtering; its basic principle is sorting a number of pixel data of pictures, and then replacing the rest of data using the middle data. The key work when designing median filter program is how to sort pixels. For example, we use the default three-by-three neighborhood to design codes. It will consume a lot of time to sort these 9 pixels for DSP, but for FPGA, these times will be greatly reduced because of its parallel characteristics.

Basic principle of sorting pixels (take 9 pixels for example) is as follows: firstly, sort the first three data to find maximum data, middle data, and minimum data; secondly, sort the second three data and the third three data; thirdly, sort above each group's maximum data, middle data, and minimum data; and lastly, sort the data whith minimum in maximum group, the data whith middle in middle group, and the data whith maximum in minimum group, and then the middle output is middle data among the above nine data. According to the above steps, we can see that iterative calculation in median filtering algorithm will cost much time, so we need to use FPGA to parallel execute above iterative calculation to improve real time (Fig. 4).

In the above picture, the program execution order is 1>2>3>4>5>6>7 in DSP because of its serial characteristic, but for FPGA, the order is 1, 2, 3>4, 5, 6>7 because of its parallel characteristic, that is, unit 1, unit 2, and unit 3 can be executed at the same time, so can unit 4, unit5, and unit 6.

4 Simulation and experiment

As the SCN continuously increased, it contained more and more data in its intern. This mainly reflects that the amount

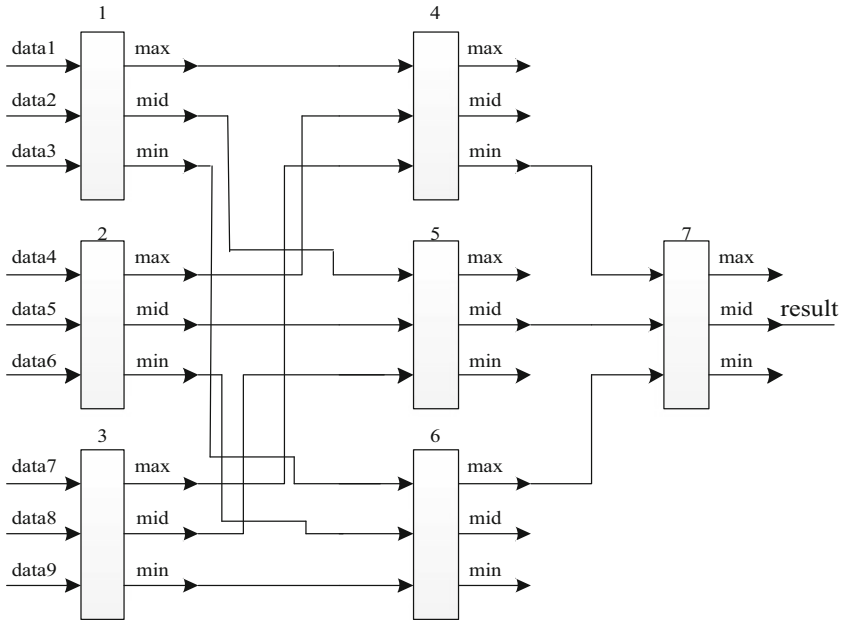

Fig. 4 Data sorting operation diagram in median filter

of data increases, which should be manipulated in network nodes. Therefore, it is literally necessary to combine SCN and big data to analyze the optimization of SCN. The risks in nodes will influence the entire SCN like domino, for example, we need to collect goods label in a fast assembly line; if the collecting equipment, like RFID or image processing equipment, have a slow speed, some goods' quantity, origin, and property will miss, and it could cause bullwhip effect.

The Boeing Company spends more than 20 billion dollars every year to buy parts and raw materials, and their parts and raw materials suppliers are around the world, so the stability and optimization of SCN directly affect the Boeing Company's development. This article, different from other scholars' optimization research of SCN in topology, models and other aspects, analyzes the impact of real time of SCN underlying data processing on SCN upper layer in a micro perspective view (Fig. 5).

From the above diagrams, we can find that there inevitably exists data processing of underlying data in supply chain. Take the SCN of the Boeing Company as an example; if one component quality has problems, it will have a significant impact on the safety of aircraft. So how to avoid this risk is the urgent need for the research. In all aspects of the underlying parts production, using digital image processing and RFID technology to identify the quality of each component in real time, and establish a quality traceability system, which can immediately locate the fault link when there has quality problems, is totally wise. The traditional digital image processing and RFID technology mainly use large and special computer or embedded DSP/ARM processor to design. Due to the condition that using large and special computer or embedded DSP/ARM processor in the process of data processing has a relatively low real-time, this paper purposes to design SCN underlying data device by using FPGA, in order to take advantage in the aspects of real time of data processing, high equipment integration, and miniaturization. To test this kind of advantage, a Kalman filtering algorithm and median filtering algorithm based on FPGA are designed, and the feasible and valuable of the proposed method are verified by carried out simulation experiment and comparative analysis with Matlab and DSP at last.

4.1 Kalman filtering results comparison based on Matlab, DSP, and FPGA

According to classical Kalman filter algorithm and square root Kalman filter algorithm, this paper has carried out filtering time consuming simulation based on FPGA, Matlab, and DSP, and eventually made a comparative analysis (Tables 1 and 2).

According to the above experiments, we should notice that compared to DSP which has the same operating frequency, FPGA has a far faster computing speed. Because frequency of computer is 20–30 times than FPGA, its calculating speed is faster than FPGA, but if they are under the same frequency, FPGA is definitely faster than Matlab. Moreover, in supply chain, such as smart handheld test equipment, miniature RFID detection, a huge computer cannot be used as a processor. So embedded micro-processors are needed, and in this way, FPGA is very useful.

The following is needed to validate filtering precision based on FPGA. Normally, we consider Matlab has high operating precision, Because FPGA also has 64 bit floating point arithmetic like Matlab, it also has a high precision like Matlab (Table 3).

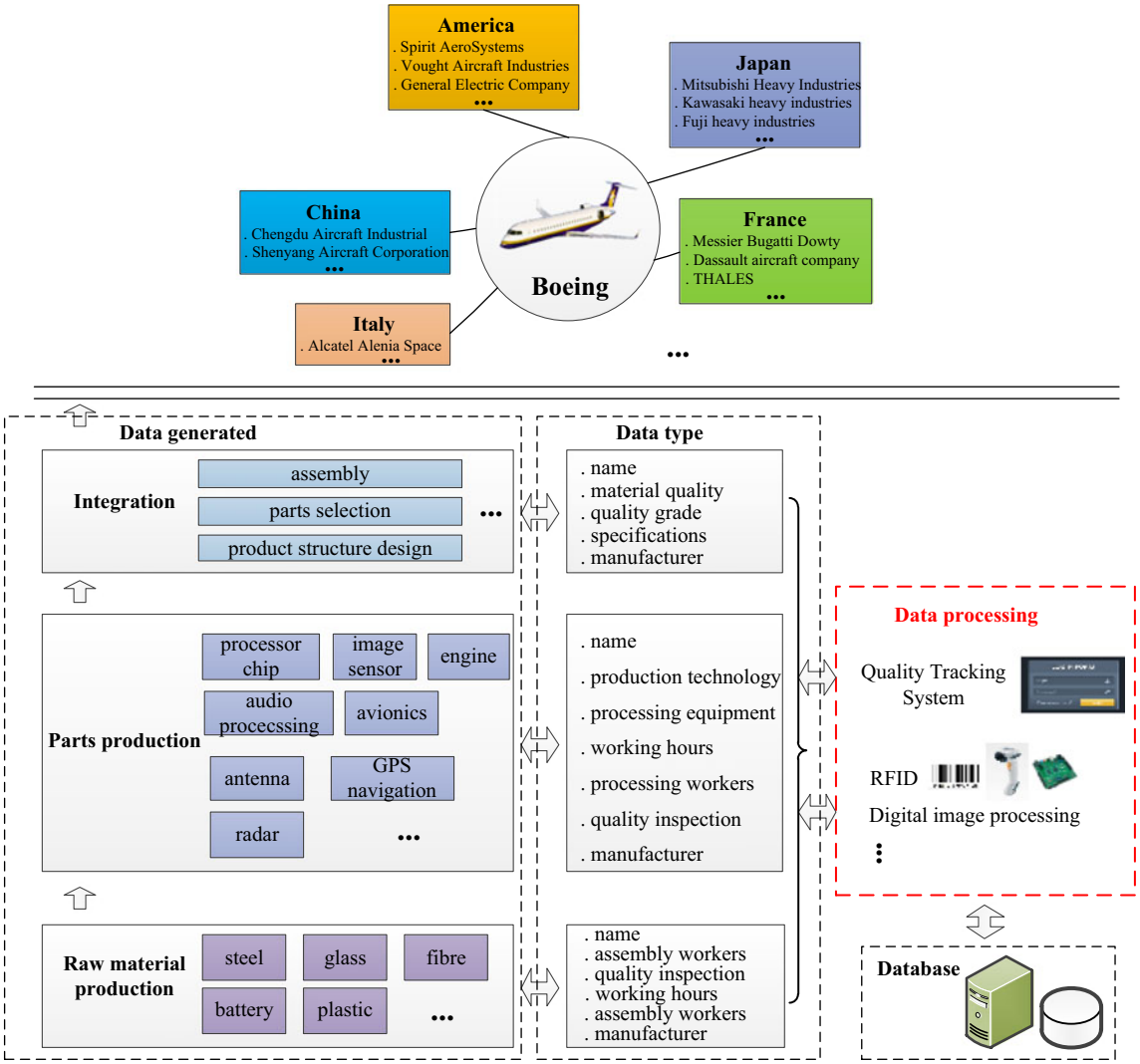

Fig. 5 Data flow diagram of SCN

From the above table, we can see that FPGA-based filter's output has the same precision with Matlab-based filter with the increase of iterations.

Next, we should prove the correctness of FPGA-based Kalman filter calculating results (Fig. 6).

In the above pictures, (a) is ideal waveform and (b) is the waveform with white noise. Picture (c) is the waveform after FPGA filtering, the amplitude of curve after filtering has little attenuation, and this situation perhaps is caused by hardware circuit, but it did not make a difference on proving real time and high precision of FPGA-based filter.

4.2 Median filtering results comparison based on Matlab, DSP, and FPGA

As already mentioned above, median filtering algorithm is widely used in image filtering. In this section, according to the bar code of commodity in SCN, we design a filter based on Matlab, DSP, and FPGA; the aim is also to verify real time and precision of FPGA-based filter, to illustrate FPGA-based embedded devices designed in SCN have great potential advantages. This paper uses a bar code picture with 130*400 pixels to do experiment, the time consumed among Matlab, DSP, and FPGA shown below (Table 4):

At the same time, median filtering results are as follows (Fig. 7):

As shown in above pictures, (a) is original picture; (b) is picture with salt and pepper noise; (c) is picture after filtering by Matlab; (d) is picture after filtering by FPGA; and (e) is picture after filtering by DSP. We can see that with the advantage in real time, FPGA also has great filtering precision, and the filtering results of three methods are almost the same.

The experiment results show the rapidness of FPGA dynamic reconfiguration. And since the reconfiguration does not interrupt the running of other codes, it is very suitable in the occasions which have high demand of the real-time function and continuity of data processing.

Table 1 Classical Kalman filtering time comparison

Dimension	Time consumption per iteration (unit: ms)		
	Matlab	FPGA	DSP
1	0.27	0.00045	0.019
2	0.32	0.020	0.069
4	0.33	0.21	0.36
9	0.34	0.56	3.17
13	0.35	1.59	8.98
15	0.36	2.39	13.56
20	0.41	5.59	31.26

Matlab is running in a computer, and its configuration is as follows: Lenovo G460, Intel(R) Core(TM) i3 CPU M380@2.53GHz, 2G memory, Windows 7 of 32 bits. FPGA is using VHDL language to design Kalman filter, FPGA's operating frequency is 100 MHz. DSP is using C language to design Kalman filter, DSP's operating frequency is 100 MHz. Filter's dimension is the dimension of state matrix $\hat{x}$. In this paper, FPGA is belonging to Xilinx Co. Ltd., and model is XC5VLX50T, and at the same time, the integrated development software is ISE, version is 14.1; Matlab's version is 7.9.0; DSP is belonging to Texas Instruments Co. Ltd., and model is TMS320F28335, its integrated development software is CCS, version is 4.1.2.

5 Conclusion and future works

In order to research risks reduction in big data, this paper pays full attention on underlying data processing in SCN. To improve real time of underlying data processing by reducing potential risks caused by time-delay in SCN, this paper uses the parallel characteristic of FPGA to design Kalman filter and median filter. Based on comparisons with Matlab and DSP, the advantage of FPGA-based designed complex algorithm has been proved, and also it has confirmed that using this method to design embedded devices in collecting and preprocessing underlying data in SCN has great potential advantages.

Table 2 Square root Kalman filtering time comparison

Dimension	Time consumption per iteration (unit: ms)		
	Matlab	FPGA	DSP
5	0.093	0.076	0.58
8	0.11	0.29	1.95
10	0.14	0.54	3.27
13	0.17	1.16	7.56
15	0.18	1.77	11.36
16	0.19	2.14	13.48
17	0.20	2.56	16.25
18	0.21	2.93	19.16
19	0.27	3.55	22.39
20	0.29	4.13	25.98

Matlab is running in a computer, and its configuration is as follows: Lenovo Win7 PC, Intel(R) Core(TM) i5 CPU @3.10GHz,4G memory, Windows 7 of 32 bits. FPGA is using VHDL language to design Kalman filter, FPGA's operating frequency is 100 MHz. DSP is using C language to design Kalman filter, DSP's operating frequency is 100 MHz. Filter's dimension is the dimension of state matrix $\hat{x}$. In this paper, FPGA is belonging to Xilinx Co. Ltd., and model is XC5VLX50T, at the same time, the integrated development software is ISE, version is 14.1; Matlab's version is 7.9.0; DSP is belonging to Texas Instruments Co. Ltd., and model is TMS320F28335, its integrated development software is CCS, version is 4.1.2.

Table 3 Kalman filtering precision comparison based on FPGA and Matlab

Iterations	Result	
	Matlab	FPGA
1	0.12660175474887	0.12660175474887
10	0.13573508184915	0.13573508184915
100	0.13448977127033	0.13448977127033
200	0.13443986005701	0.13443986005701
300	0.13442560983223	0.13442560983223
500	0.13441493273449	0.13441493273449
800	0.13440918727749	0.13440918727749
1000	0.13440731177792	0.13440731177792

Matlab is running in a computer, and its configuration is as follows: Lenovo Win7 PC, Intel(R) Core(TM) i5 CPU @3.10GHz,4G memory, Windows 7 of 32 bits. FPGA is using VHDL language to design Kalman filter, FPGA's operating frequency is 100 MHz. In this paper, FPGA is belonging to Xilinx Co. Ltd., and model is XC5VLX50T, at the same time, the integrated development software is ISE, version is 14.1; Matlab's version is 7.9.0.

But the author has to admit that parallel characteristic of FPGA is fully at the cost of occupying most of the FPGA's resource; for an internal region of FPGA, it only can execute a function, so user's codes will cost so many regions, for example, just one Kalman filter in this paper occupied nearly half of FPGA chip resource. So there will need more than one FPGA chip to execute user's large codes, This method will inevitably increase the cost, and its hardware architecture will become bloated and is not completely suitable for the occasions which have strict limits on volume, such as smart handheld devices, micro-robotics, and micro RFID equipment. According to this situation, there are two methods to solve it: using dynamic reconfiguration function of FPGA or using SoC technology.

The main idea of dynamic reconfiguration of FPGA is time division multiplexing. Making one internal region of FPGA can execute more than one function, and the other region is running normally when this region's function switches.

With the scale sharp increasing of SCN, there is more and more data needed to be processed. And there are higher demands of timely and effective processing for these data. Due to constraints by manufacturing technique and other factors, the frequency of FPGA cannot unlimitedly increase, even if using FPGA parallel computing technology. We need to seek for other ways to solve this problem. On the basis of this paper, the author is going to do more researches about SoC

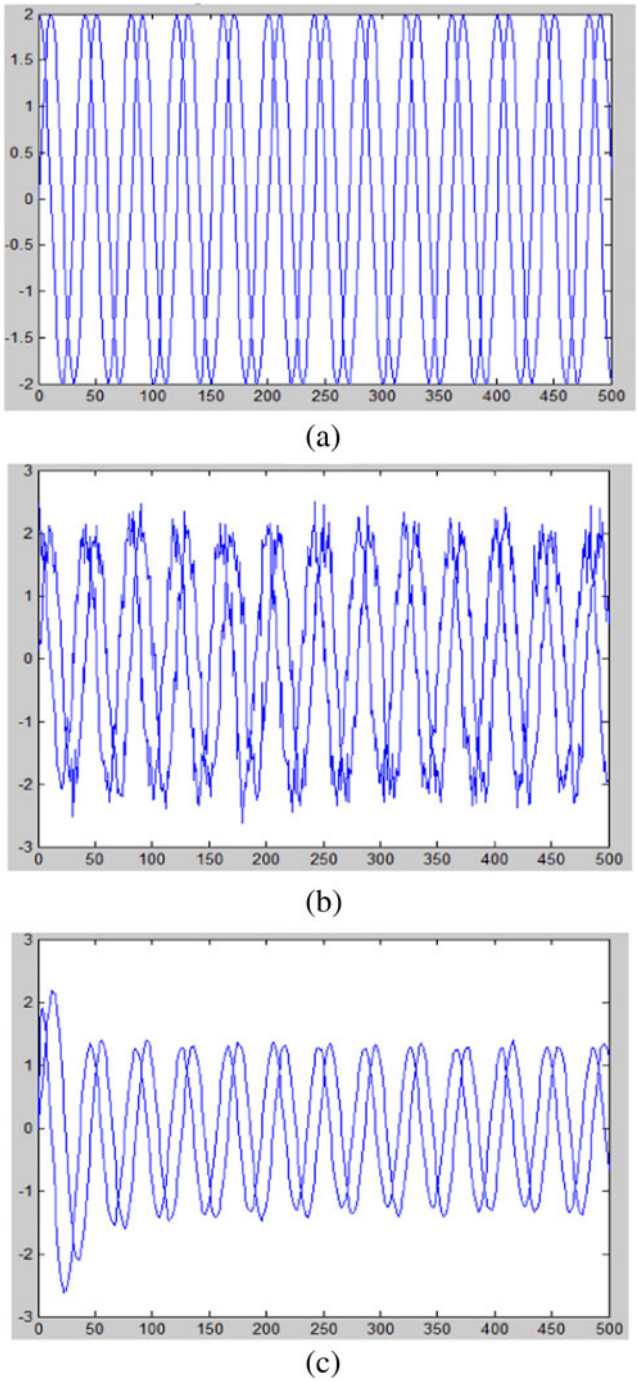

Fig. 6 Filtering curve comparison based on FPGA

technology. SoC (system on chip) is system-level chip technology, multiple FPGA and DSP are integrated in one SoC chip, and it is easy to build multi-core system, so SoC not only has FPGA's parallel computing but also have DSP's advantage in resource consume, and it finds equilibrium point between real-time and resource consume.

According to potential risks in SCN, this paper starts to find an appropriate method in micro level; the author notices that the real time of underlying data processing in network does not cause enough attention, and the author strongly considers that time-delay problem will be like a domino quickly threatening the entire network from small network node. So this paper proposes using parallel characteristic of FPGA to design

Table 4 Median filtering time comparison (unit: ms)

Matlab	FPGA	DSP
5.25	3.88	304.97

Matlab is running in a computer, and its configuration is as follows: DELL Win7 PC, Intel(R) Core(TM) i7-3537 CPU @2.00GHz,8G memory, Windows 7 of 64 bits. FPGA is using VHDL language to design Kalman filter, FPGA's operating frequency is 100 MHz. DSP is using C language to design Kalman filter, DSP's operating frequency is 100 MHz. In this paper, FPGA is belonging to Xilinx Co. Ltd., and model is XC7A100TCSG324-1, at the same time, the integrated development software is ISE, version is 14.4; Matlab's version is 7.9.0; DSP is belonging to Texas Instruments Co. Ltd., and model is TMS320F28335, its integrated development software is CCS, version is 4.1.2.

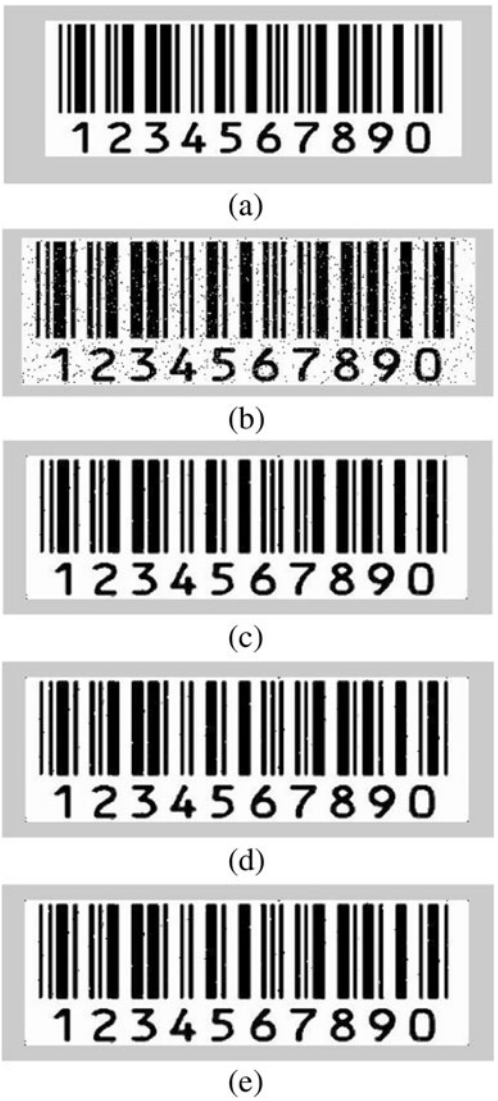

Fig. 7 Median filtering results

embedded device to process original sensor data in the bottom of network. The author will continue to search for related method to solve potential problems in network by using hardware technology.

Acknowledgments This work is partly supported by National Natural Science Foundation of China (Grants No. 51522501 and No. 51475032), Beijing Natural Science Foundation (No. 4152032), and the 863 Program project in China (No. 2013AA041302).

References

1. Li JR, Tao F, Cheng Y, Zhao LJ (2015) Big data in product lifecycle management. Int J Adv Manuf Technol. doi:10.1007/s00170-015-7151-x
2. Lu RX, Zhu H, Liu XM, Liu JK, Shao J (2014) Toward efficient and privacy-preserving computing in big data era. IEEE Netw 28(4):46–50
3. Gu L, Zeng DZ, Li P, Guo S (2014) Cost minimization for big data processing in geo-distributed data centers. IEEE Transactions on Emerging Topics in Computing 2(3):314–323
4. Xu L, Jiang CX, Wang J, Yuan J, Ren Y (2014) Information security in big data: privacy and data mining. IEEE Access 2:1149–1176
5. Slavakis K, Giannakis GB, Mateos G (2014) Modeling and optimization for big data analytics: (statistical) learning tools for our era of data deluge. IEEE Signal Process Mag 31(5):18–31
6. Liu Y, He J, Guo MJ, Yang Q, Zhang XS (2014) An overview of big data industry in China. China Communications 11(12):1–10
7. Lu TB, Guo XB, Xu B, Zhao LL, Peng Y, Yang HY (2013) Next Big Thing in Big Data: The Security of the ICT Supply Chain. International Conference on Date of Conference:1066–1073
8. Robak S, Franczyk B, Robak M (2013) Applying big data and linked data concepts in supply chains management. Federated Conference on Computer Science and Information Systems (FedCSIS):1215–1221
9. Zage D, Glass K, Colbaugh R (2013) Improving supply chain security using big data. IEEE International Conference on Intelligence and Security Informatics (ISI):254–259
10. Hu H, Wen YG, Chua TS, Li XL (2014) Toward scalable systems for big data analytics: a technology tutorial. IEEE Access 2:652–687
11. Tu YJ, Piramuthu S (2011) A decision-support model for filtering RFID read data in supply chains. IEEE Trans Syst Man Cybern Part C Appl Rev 41(2):268–273
12. Liu Y, Hipel KW (2012) A hierarchical decision model to select quality control strategies for a complex product. IEEE Trans Syst Man Cybern Syst Hum 42(4):814–826
13. Lau JSK, Huang GQ, Mak KL, Liang L (2006) Agent-based modeling of supply chains for distributed scheduling. IEEE Transactions on Systems, Man, and Cybernetics—Part A: Systems and Humans 36(5):847–861
14. Kelepouris T, Harrison M, McFarlane D (2011) Bayesian supply chain tracking using serial-level information. IEEE Trans Syst Man Cybern Part C Appl Rev 41(5):733–742
15. Zhao K, Kumar A, Harrison TP, Yen J (2011) Analyzing the resilience of complex supply network topologies against random and targeted disruptions. IEEE Syst J 5(1):28–39
16. Wang Y, Hu W (2011) The topology analysis on value creation of logistics financial management in supply chain system. International Conference on Business Management and Electronic Information (BMEI):243–248
17. Tao F, Zhao D, Hu YF, Zhou ZD (2008) Resource service composition and its optimal-selection based on particle swarm optimization in manufacturing grid system. IEEE Trans Ind Inf 4(4):315–327
18. Tao F, LaiLi YJ, Xu L, Zhang L (2013) FC-PACO-RM: a parallel method for service composition optimal-selection in cloud manufacturing system. IEEE Trans Ind Inf 9(4):2023–2033
19. Tao F, Zhang L, Laili YJ (2015) Configurable Intelligent Optimization Algorithms: Design and Practice in Manufacturing. Springer, ISBN: 978-3-319-08839-6
20. Tao F, Zhang L, Hu YF (2011) Resource Services Management in Manufacturing Grid System. Wiley-Scrivener Publishing (Scrivener-Wiley bookstore), ISBN: 978-1-118-12231-0
21. Tao F, Zuo Y, Xu L, Lv L, Zhang L (2014) Internet of things and BOM based life cycle assessment of energy-saving and emission-reduction of product. IEEE Trans Ind Inf 10(2):1252–1264
22. Tao F, Laili YJ, Liu YL, Feng Y, Wang Q, Zhang L, Xu L (2014) Concept, principle and application of configurable intelligent optimization algorithm. IEEE Syst J 8(1):28–42
23. Tao F, Zuo Y, Xu L, Zhang L (2014) IoT-based intelligent perception and access of manufacturing resource toward cloud manufacturing. IEEE Trans Ind Inf 10(2):1547–1557
24. Tao F, Cheng Y, Xu L, Zhang L, Li B (2014) CCIoT-CMfg: cloud computing and internet of things based cloud manufacturing service system. IEEE Trans Ind Inf 10(2):1435–1442
25. Tao F, Li C, Liao TW, Laili YJ (2015) BGM-BLA: a new algorithm for dynamic migration of virtual machines in cloud computing. IEEE Trans Serv Comput. doi:10.1109/TSC.2015.2416928
26. Tao F, Zhang L, Liu YK, Cheng Y, Wang LH, Xun X (2015) Manufacturing service management in cloud manufacturing: overview and future research directions. J Manuf Sci Eng 137(4): 040912-1-040912-11
27. Tao F, Cheng Y, Zhang L, Nee AYC (2015) Advanced manufacturing systems: socialization characteristics and trends. J Intell Manuf. doi:10.1007/s10845-015-1042-8
28. Tao F, Zhang L, Lu K, Zhao D (2012) Research on manufacturing grid resource service optimal-selection and composition framework. Int J Enterp Inf Syst 6(2):237–264
29. Tao F, Zhang L, Venkatesh VC, Luo YL, Cheng Y (2011) Cloud manufacturing: a computing and service-oriented manufacturing model. Proc IMechE B J Eng Manuf 225(10):1969–1976
30. Jazemi R, Ghodsypour SH, Kheljani JG (2011) Considering supply chain benefit in supplier selection problem by using information sharing benefits. IEEE Trans Ind Inf 7(3):517–526
31. Agami N, Saleh M, Rasmy M (2014) An innovative fuzzy logic based approach for supply chain performance management. IEEE Syst J 8(2):336–342
32. Agami N, Saleh M, Rasmy M (2012) A hybrid dynamic framework for supply chain performance improvement. IEEE Syst J 6(3):469–478
33. Wu DD, Luo CC, Olson DL (2014) Efficiency evaluation for supply chains using maximin decision support. IEEE Trans Syst Man Cybern Syst Hum 44(8):1088–1097
34. Chan HK (2011) Supply chain systems—recent trend in research and applications. IEEE Syst J 5(1):2–5
35. Hill CA, Zhang GP, Scudder GD (2009) An empirical investigation of EDI usage and performance improvement in food supply chains. IEEE Trans Eng Manag 56(1):61–75
36. Cuiñas I, Newman R, Trebar M, Catarinucci L, Melcon AA (2014) Wireless corner: RFID-based traceability along the food-production chain. IEEE Antennas Propag Mag 56(2):196–207
37. Cunningham SP (2009) Special section on supply chain management in the semiconductor industry. IEEE Trans Semicond Manuf 22(1):153

38. Ulieru M, Cobzaru M (2005) Building holonic supply chain management systems: an e-logistics application for the telephone manufacturing industry. IEEE Trans Ind Inf 1(1):18–30
39. Wu XZ, Shao ZY, Zhang XM, Gao J, Jin GL (2010) The operation of supply-chain logistics in iron and steel enterprises. International Conference on Education Technology and Computer (ICETC): 103–106
40. Zhou CY, Fan HR, Jiang W (2011) An model for supply chain logistics cost management based on analytic hierarchy process. International Conference on Business Management and Electronic Information (BMEI):269–273
41. Kumar V, Mishra N (2011) A multi-agent self correcting architecture for distributed manufacturing supply chain. IEEE Syst J 5(1): 6–15
42. Gaukler GM (2011) Item-level RFID in a retail supply chain with stock-out-based substitution. IEEE Trans Ind Inf 7(2):362–370
43. Ondemir O, Ilgin MA, Gupta SM (2012) Optimal end-of-life management in closed-loop supply chains using RFID and sensors. IEEE Trans Ind Inf 8(3):719–728
44. Chalasani S, Boppana RV (2007) Data architectures for RFID transactions. IEEE Trans Ind Inf 3(3):246–257
45. Lee CH, Chung CW (2011) RFID data processing in supply chain management using a path encoding scheme. IEEE Trans Knowl Data Eng 23(5):742–758
46. Piramuthu S (2008) Lightweight cryptographic authentication in passive RFID-tagged systems. IEEE Trans Syst Man Cybern Part C Appl Rev 38(3):360–376
47. Hsu C, Levermore DM, Carothers C, Babin G (2007) Enterprise collaboration: on-demand information exchange using enterprise databases, wireless sensor networks, and RFID systems. IEEE Transactions on Systems, Man, and Cybernetics—Part A: Systems and Humans 37(4):519–532
48. Olson DL (2012) Supply Chain Risk Management. Business Expert
49. Wang S, Watada J, Pedrycz W (2009) Value-at-risk-based two-stage fuzzy facility location problems. IEEE Trans Ind Inf 5(4):465–482
50. Shen B, Choi TM, Wang YL, Lo CKY (2013) The coordination of fashion supply chains with a risk-averse supplier under the markdown money policy. IEEE Transactions on Systems, Man, and Cybernetics: Systems 43(2):266–276
51. Zhang AN, Goh M, Terhorst M, Lee AJL, Pham MT (2013) An Interactive Decision Support Method for Measuring Risk in a Complex Supply Chain under Uncertainty. IEEE International Conference on Systems, Man, and Cybernetics:633–638
52. Groza B, Murvay S (2013) Efficient protocols for secure broadcast in controller area networks. IEEE Trans Ind Inf 9(4):2034–2042
53. Bernardi S, Campos J, Merseguer J (2011) Timing-failure risk assessment of UML design using time petri net bound techniques. IEEE Trans Ind Inf 7(1):90–104
54. Lao SI, Choy KL, Tsim YC, Poon TC (2010) A RFID-based decision support system for food receiving operations assignment. International Conference on Supply Chain Management and Information Systems (SCMIS):1–7
55. Wang Q, Gopalakrishnan S (2010) Adapting a main-stream internet switch architecture for multihop real-time industrial networks. IEEE Trans Ind Inf 6(3):393–404
56. LoBello L, Toscano E (2009) An adaptive approach to topology management in large and dense real-time wireless sensor networks. IEEE Trans Ind Inf 5(3):314–324
57. Neghab AP, Siadat A, Moghaddam RT, Jolai F (2011) An Integrated Approach for Risk-Assessment Analysis in a Manufacturing Process Using FMEA and DES. Proceedings of the 2011 I.E. ICQR:366–370
58. Lazzerini B, Mkrtchyan L (2011) Analyzing risk impact factors using extended fuzzy cognitive maps. IEEE Syst J 5(2):288–297
59. Mousavi OA, Cherkaoui R (2013) Discussion on Uncertainty Management in Power Systems. IREP Symposium-Bulk Power System Dynamics and Control –IX (IREP)
60. Kazmierkowski MP, Jasinski M, Wrona G (2011) DSP-based control of grid-connected power converters operating under grid distortions. IEEE Trans Ind Inf 7(2):204–211
61. Mastromauro RA, Liserre M, Aquila AD (2012) Control issues in single-stage photovoltaic systems: MPPT, current and voltage control. IEEE Trans Ind Inf 8(2):241–254
62. Nabulsi AA, Dhaouadi R (2012) Efficiency optimization of a DSP-based standalone PV system using fuzzy logic and dual-MPPT control. IEEE Trans Ind Inf 8(3):573–584
63. Gora MA, Maiti A, Schaumont P (2010) A flexible design flow for software IP binding in FPGA. IEEE Trans Ind Inf 6(4):719–728
64. Gomperts A, Ukil A, Zurfluh F (2011) Development and implementation of parameterized FPGA-based general purpose neural networks for online applications. IEEE Trans Ind Inf 7(1):78–89
65. Naouar MW, Monmasson E, Naassani AA, Belkhodja IS (2013) FPGA-based dynamic reconfiguration of sliding mode current controllers for synchronous machines. IEEE Trans Ind Inf 9(3):1262–1271
66. Campo I, Basterretxea K, Echanobe J, Bosque G, Doctor F (2012) A system-on-chip development of a neuro–fuzzy embedded agent for ambient-intelligence environments. IEEE Trans Syst Man Cybern B Cybern 42(2):501–512
67. Fu Y, Li H, Kaye ME (2010) Hardware/software codesign for a fuzzy autonomous road-following system. IEEE Trans Syst Man Cybern Part C Appl Rev 40(6):690–696
68. Xu TL, You WH, Cui PY (2005) INS/GPS integrated navigation system algorithm research based on fuzzy adaptive Kalman filtering. J Aerosp 5:571–575
69. Esakkirajan S, Veerakumar T, Subramanyam AN, PremChand CH (2011) Removal of high density salt and pepper noise through modified decision based unsymmetric trimmed median filter. IEEE Signal Process Lett 18(5):287–290