Int J Adv Manuf Technol (2015) 78:1651–1663
DOI 10.1007/s00170-014-6732-4

ORIGINAL ARTICLE

Experimental study on improving μ-WEDM and μ-EDM of doped silicon by temporary metallic coating

Tanveer Saleh · Aous Naji Rasheed · Asan G. A. Muthalif

Received: 4 August 2014 / Accepted: 17 December 2014 / Published online: 13 January 2015

Abstract Wire electro-discharges machining (WEDM) is a variant of electro-discharge machining (EDM) based method for non-contact machining that uses wire as the machining tool. Micro-EDMing/micro-WEDMing (where discharge energy is very low and tool size in micrometer range) operation of silicon (Si) can achieve features with very complex shapes, which have many useful applications in microelectro-mechanical system (MEMS). However, Si is a semiconductor material with high resistivity, and it is difficult to create electrical sparks during μ-WEDM/μ-EDM process. Thus, the machining of Si can be enhanced if it is possible to increase the conductivity of this semiconductor. This study aims to develop and characterize the process of improved μ-WEDM and μ-EDM of Si by temporarily coating Si with a high conductive metal (gold in this study). Micro-WEDM process stability was found to be improved (~100× for different machining condition) if coated Si wafer is used as compared to uncoated Si workpiece. Material removal rate (MRR) was also found to be increased by a good margin (~30 % average) for coated Si wafer. Machined slots were found to be more uniform though kerf width was slightly larger for coated Si wafer. In case of μ-EDM operation, gold-coated Si also enhanced the machining as compared to uncoated Si. In this case, MRR was increased by up to seven times for coated samples. Overall, this new method of μ-WEDM and μ-EDM technique of polished Si wafer has been found to be more efficient and useful. Removal of the conductive coating without damaging the substrate is a challenge for this process, which was carried out successfully by selective etching method.

T. Saleh (✉) · A. N. Rasheed · A. G. A. Muthalif
Smart Structures, Systems & Control Research Lab., Department of Mechatronics Engineering, International Islamic University Malaysia, Jalan Gombak, Kuala Lumpur, Malaysia
e-mail: tanveers@iium.edu.my

A. N. Rasheed
Engineering Affairs Department, Tikrit University, Tikrit, Iraq

Keywords μ-WEDM · μ-EDM · Polished Si · Conductive coating

1 Introduction

Electrical discharge machining, commonly termed as EDM, is a nonconventional machining processes where material removal is taken place by means of thermal energy generated from electrical discharges between conductive tool and workpiece without any physical contact [1]. In wire EDM (WEDM), a flexible metallic wire is used instead of rigid tool in EDM operation [2]. EDM and WEDM are mostly used for conductive material because of their working principle as mentioned above. Micro-EDM and micro-WEDM (μ-EDM/μ-WEDM) is a promising machining technology to produce features in meso- and micrometer scale for different engineering applications [1, 2]. In μ-EDM, discharge energy that is used for machining is in μ-Joule level. Therefore, in order to maintain desired material removal rate (MRR), it is necessary to generate high frequency pulses for μ-EDM process. Machines conducting this manufacturing operation are required to have high rigidity with micrometer range resolution, accuracy, and precision [3]. Since 1990s, μ-EDM has become a very useful fabrication method in the field of micro-mold and complex 3D structures fabrication [4, 5]. In 1998, Yu et al. [4] developed a mold for a micro-car (500-μm long) by μ-EDM technique. Later, a CAD/CAM system was developed by Rajurkar et al. [5] for fabricating complex 3D features by scanning μ-EDM method. This method has also been used for patterning other conducting materials such as carbon nanotube forest (CNT forest) and conductive polymers [6–9]. Anwar et al. [6] also used μ-EDM to pattern conductive

polymer for biomedical application. Recently, same technique has been used to create 3D patterns on CNT forest for MEMS-based applications [7–9].

Silicon (Si) is a common engineering material, which is used in the field of MEMS and electronics. However, machining semiconductor material like Si by μ-EDM is very challenging, and not many efforts were made so far in this regard. High surface resistance of Si compared to its bulk body resistance is considered to be biggest hurdle for machining silicon by EDM. Reynaerts et al. [10] proposed to adjust the polarity of doped silicon in such a way so that, for p-type silicon, electrode is negative and silicon is positive and vice versa for n-type silicon to overcome the surface potential barrier. Another solution proposed by Reynaerts et al. [10] is to use of conductive plating on the silicon workpiece. Luo et al. [11] studied slicing of Si wafer from the silicon ingot by WEDM. In order to achieve best cutting performance, nickel plating of the silicon was carried out. In his study, Luo et al. [11] used high current for the machining, which is in a range of 6–14 A to slice silicon wafer from silicon ingots. This technique was further investigated by Peng et al. [12], and they concluded that it is not efficient to use WEDM method for machining pure silicon ingot (without doping). However, another study carried out by Wang et al. [13] used hybrid oil/aqueous electrolyte for slicing Si. This approach is based on wire electrolytic-spark slicing strategy using hybrid oil/aqueous electrolyte. Okamoto et al. [14] developed a multiwire EDM method to slice wafer from silicon ingot, which increased the productivity of the process. Research carried out by Crawford from MIT [15] aimed to characterize EDM and WEDM process for machining highly doped Si substrate. This research data is useful for rapid prototyping of silicon-based MEMS devices. Contouring of doped silicon wafer by WEDM to produce microstructures were investigated by Staufert et al. [16]. In their study, Staufert et al. [16] used relaxation-type EDM power supply with capacitor value ranges from 500 to 10000 pf, which is significantly above the range of capacitor value used in μ-WEDM. Rakwal et al. [17] used μ-WEDM technology to fabricate high aspect ratio silicon microelectrode array of different shapes. Arrays with 144 electrodes on a 400-μm pitch were fabricated on 6 and 10 mm thick p-type silicon wafers to a length of 5 and 9 mm, respectively. Yu et al. [18] proposed use of auxiliary power supply in slicing of polycrystalline silicon by WEDM, which improves the machining efficiency as they reported. Zhidong et al. [19] proposed a new automatic servo control mechanism for WEDM processing of silicon using current pulse probability detection to overcome the problem of inaccurate detection of open circuit, normal discharge, and short circuit. Jahan et al. [20] carried out a parametric study on micro-machining of p-type Si wafer by μ-EDM. They investigated the machining performance for different types of geometrical structures, namely, micro-holes, blind slots, and thru slots. Song et al. [21] also investigated μ-EDM performance on highly doped p-type Si wafer. They found that material removal mechanism during μ-EDMing of silicon wafer is different compared to conventional metal μ-EDM. They concluded that, to get micro-crack-free smooth EDMed silicon surfaces, the discharge energy needs to be controlled to low levels, which are significantly lower than metal μ-EDM.

Polished silicon mirrors have vast applications in sensors and optical industries. Wire electro-discharge machining (WEDM) can be used for fabricating complex-shaped silicon mirrors with various contours. The technology was first proposed by Takino et al. [22, 23]. They used conventional EDM power (5–30 A) in their pioneering research. However, the degradation of the polished surface due to the spark energy should be kept as minimum as possible in order to maintain required optical quality. This can be achieved more efficiently if μ-EDM is used instead of conventional EDM to machine polished silicon. The main challenge to use μ-EDM for machining Si is the surface resistance, which cannot be easily overcome with μ-Joule discharge energy. An initial study conducted by Rasheed et al. [24] showed temporary conductive coating enhances μ-WEDM performance of doped Si wafer.

In this paper, authors have reported detail study on a new μ-WEDM and μ-EDM machining of polished Si wafer (p-type and 1–50 Ω cm resistivity) using temporary metallic coating. Moreover, this paper describes thoroughly how the process zone resistance is affected by the coating process with proper electrical equivalent model for both WEDM and EDM operation, which cannot be found in previously reported works conducted by other researchers. This method is very useful for rapid prototyping of Si-based MEMS devices before going for costly and complicated lithography based mass fabrication process. In this work, authors coated the silicon wafer with conductive material (gold for this study), in order to produce high conductive gold–silicon–gold composite. However, it is also equally possible to use less expensive temporary metallic coating such as Cu to achieve high conductive Cu–Si–Cu for μ-WEDM/μ-EDM operation of Si. This enhances the machining rate quite significantly both in WEDM and EDM process, and later, the coating can be easily removed by simple wet etching method without having any detrimental effect on the polished surface. Machining performance of gold-coated silicon by μ-WEDM/EDM was studied in this research work, which has been reported thoroughly in the subsequent sections of this paper.

2 Hypothesis of μ-WEDM/EDM of gold-coated Si wafer

This section of the paper explains hypothesis about EDM/WEDM of gold-coated Si wafer. In the case of μ-WEDM operation, the basic idea behind the coating of polished silicon

wafer with conductive material is to reduce the specific resistivity of the resultant composite. In order to understand the theory of the proposed concept, a simple model of the actual WEDM zone is developed as shown in Fig. 1a. The analogous electrical circuit model is shown in Fig. 1b. The equivalent resistance of the modified workpiece can be determined from the following formulation.

$$\begin{aligned} R_{eq} &= R_{gold} || R_{Si} || R_{gold} \\ \Rightarrow \frac{1}{R_{eq}} &= \frac{1}{R_{gold}} + \frac{1}{R_{si}} + \frac{1}{R_{gold}} \\ \Rightarrow R_{eq} &= \frac{R_{gold} \times R_{si}}{2R_{si} + R_{gold}} \end{aligned}$$

Putting the standard relationship between bulk resistance and resistivity, i.e., $R = \rho \frac{L}{A}$, the following equation can be determined,

$$\Rightarrow R_{eq} = \frac{\rho_{gold} \times \rho_{Si} \times L}{2A_{gold}\rho_{Si} + A_{Si}\rho_{gold}} \quad (1)$$

where,

R_{eq} is the equivalent resistance of the Au–Si–Au composite in (Ω)
ρ_{gold} is the resistivity of gold coating (Ω m)
ρ_{Si} is the resistivity of the silicon wafer (Ω m)
L is the workpiece length as shown in Fig. 1a (m)
A_{gold} is the cross-sectional area of the gold coating (m^2)
A_{Si} is the cross-sectional area of the silicon (m^2).

The following equation is also true for the new gold–Si–gold composite.

$$R_{eq} = \frac{\rho_{eq} L}{2A_{gold} + A_{Si}} \quad (2)$$

where ρ_{eq} is the equivalent resistivity of gold–Si–gold composite (Ω m).

By equating Eqs. 1 and 2, the equivalent resistivity of the gold–Si–gold composite can be deduced as follows,

$$\rho_{eq} = \frac{(2A_{gold} + A_{Si})\rho_{gold} \times \rho_{Si}}{2A_{gold}\rho_{Si} + A_{Si}\rho_{gold}} \quad (3)$$

Following relationship between ρ_{Au} and ρ_{Si} can be assumed,

$$\rho_{gold} = K_1 \rho_{Si}$$

where K_1 is a multiplying factor, and its value is $0<K_1<1$.

Further, ratio between thickness of the gold layer t_{gold}, and the Si wafer t_{Si} can also be written as follows:

$$\frac{t_{gold}}{t_{Si}} = K_2 = \frac{A_{gold}}{A_{Si}}, \text{ as the width of the sample is constant.}$$

where K_2 is another factor and has value between $0<K_2<\infty$.

Equation 3 can be rewritten as follows after introducing K_1 and K_2,

$$\rho_{eq} = \frac{(2K_2 + 1)}{2K_2 + K_1} K_1 \rho_{Si} \quad (4)$$

Equation 4 has two limiting factors. In the first case, the conductive layer thickness is zero, so K_2 is 0, whereas in the second case, the conductive layer thickness is infinity, therefore, the value of K_2 is also infinity. By considering these two values of K_2 limiting

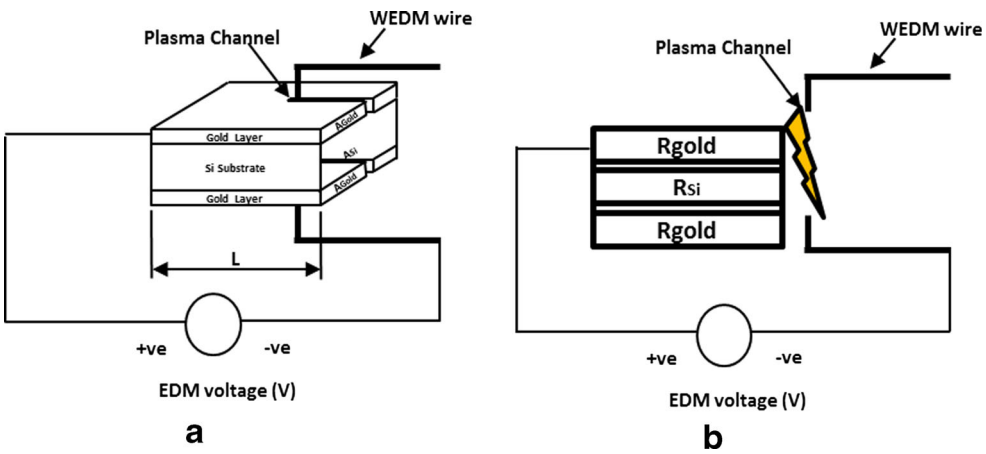


Fig. 1 **a** Simplified model of the WEDM zone. **b** Analogous electric circuit

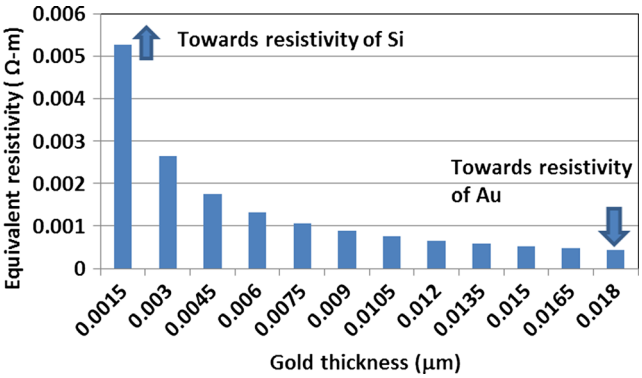


Fig. 2 Variation of resistivity of Au–Si–Au composite with thickness of Au

values for ρ_{eq} can be found from the following two equations (Eqs. 5 and 6).

$$\rho_{eq} = \lim_{K_2 \to 0} \frac{(2K_2 + 1)}{2K_2 + K_1} K_1 \rho_{Si} = \rho_{Si} \tag{5}$$

$$\rho_{eq} = \lim_{K_2 \to \infty} \frac{(2K_2 + 1)}{2K_2 + K_1} K_1 \rho_{Si} = K_1 \rho_{Si} = \rho_{gold} \tag{6}$$

It is obvious from the above discussion and Fig. 2 that if the thickness of the conductive coating is increased, the resistivity of the composite will decrease to converge towards that of the conductive coating. Reduction of resistivity or increase in conductivity of the workpiece (Si wafer) shall enhance the ease of machining of silicon by the WEDM method, which is supported by earlier work [25]. However, as the thickness of the coating is increased excessively the total material to be removed shall also increase, which might hinder the advantage of putting the conductive coating on the silicon wafer.

On the other hand, in μ-EDM, the process model (Fig. 3a) is different from that of μ-WEDM case, which is depicted in Fig. 1a. This configuration reduces the contact resistance between the Si workpiece and metallic work table ($R_{Au/metal}$) and enhances the EDM process as shown in Fig. 3b. This phenomenon is also supported by previous study [26].

3 Experimental procedure

In this research, a p-type pre polished (mirror quality) silicon wafer of 650 μm thickness was used. The wafer was coated with conductive material (Au in this research) using ion spattering machine on the both sides before the start of the actual μ-WEDMing/EDMing process. This machine is not capable for very thick coating. The coating thickness depends on time spent for coating, sputtering current, and vacuum pressure. Sputtering current and vacuum pressure were kept constant at 30 mA and 5 Pa, respectively. The rate of sputtering at 30 mA current is 0.533 nm/s. Three types of samples were prepared for the machining experiment. The first group of samples was silicon (Si) without any coating, the second and third groups were Si coated for 5 min (Si(1)) and 10 min (Si(2)) respectively. Si(1) samples have approximate coating thickness of 160 nm, and Si(2) samples have 320 nm. All three types of samples were machined for a comparative study using the μ-WEDM and μ-EDM process. The scope of this work is focused to study the enhancement of μ-EDM/ μ-WEDM operation of Si with the application of temporary metallic coating. Optimization of coating thickness is not the prime objective; hence, the authors have chosen two thickness of gold for coating. The machining parameters are summarized in Table 1.

After the machining operation, the conductive coating was removed using dilute aqua regia ($HCl/HNO_3/H_2O$=1:0.16:1). Lastly, energy dispersive X-ray spectroscopy (EDX or EDS) technique was used for chemical characterization of the

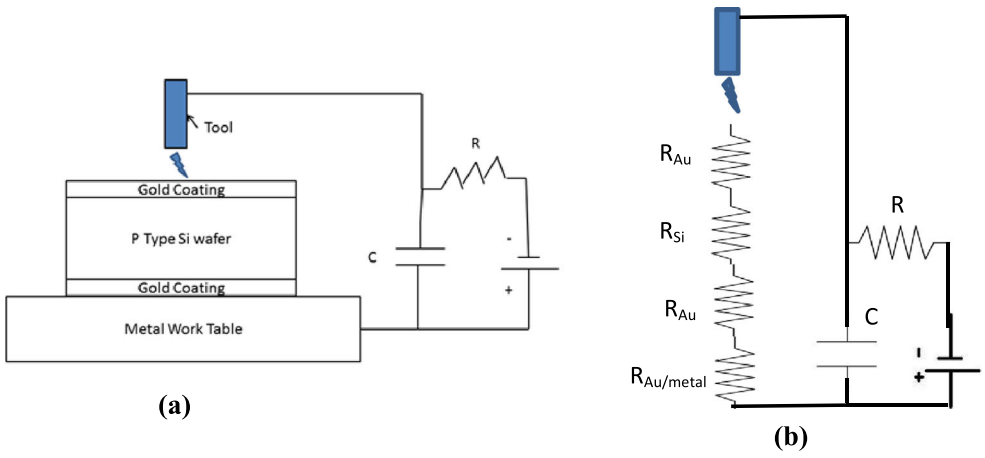


Fig. 3 **a** Sketch for μ-EDM operation for gold-coated Si. **b** Equivalent electrical model

Table 1 Summary of μ-WEDM and μ-EDM parameters

Parameters	μ-WEDM	μ-EDM
Voltage	85, 95, and 105 V	85, 95, and 105 V
Capacitor	0.1, 1, and 10 nF	0.1, 1, and 10 nF
EDM speed	5 μm/s	3 μm/s
Tool ,material	Zinc-coated brass wire	Tungsten needle
Tool/wire diameter	70 μm	500 μm
Workpiece	Polished Si wafer coated with gold (Au) thickness of 160 nm (Si(1))	Polished Si wafer coated with gold (Au) thickness of 160 nm (Si(1))
	Polished Si wafer coated with gold (Au) thickness of 320 nm(Si(2))	Polished Si wafer coated with gold (Au) thickness of 320 nm(Si(2))
	Polished Si wafer (Si)	Polished Si wafer (Si)
Programmed depth of drilling	NA	50 μm
Programmed length of cut	1 mm	NA

samples, to confirm that there is no more gold on the substrate surface. Experiments were conducted multiple times to ensure repeatability. It was found that experimental uncertainty is within 5–7 %.

4 Results and discussions

This section discusses the results of the experiments conducted for current research work. Two types of experiments (WEDM and EDM) were performed with three different samples (Si, Si(1), and Si(2)). Experiments were carried out in order to investigate importance of the coating process and its significant effects on the μ-WEDMing/ EDMing of semiconductor material like Si. The first part of this section covers μ-WEDM experiments for coated and uncoated Si, while the second part presents experiments about the μ-EDM in order to give a broad idea about the impact of coating on this type of non-conventional machining process.

4.1 Study of μ-WEDM for coated Si

4.1.1 Machining stability study

Instability in machining will lead to low material removal rate (MRR) and bad surface quality, particularly in EDM and in WEDM. In μ-WEDM/EDM, three phenomena are basically observed during machining, namely, normal discharge, abnormal arcing/ short circuit, and open circuit. The most desirable among these three is the normal discharge, which actually causes the material to be removed from the workpiece, whereas short circuit is the most detrimental among these three. When any short circuit or abnormal arcing occurs, the motion controller sends a reverse motion path command to the servo to overcome this condition. During this reverse motion, theoretically, no material is removed from the workpiece. Therefore, excess occurrence of short circuit or abnormal arcing will cause slower machining rate. The μ-WEDM operation is said to be stable if normal discharge occurs more frequently during machining. In this research, short circuit output was monitored periodically for each machining experiment to study machining stability. Figure 4 shows average occurrence of short/arcing (nos/min), for the machining of gold-coated and uncoated silicon. It was also found that the μ-WEDMing operation is completely impossible at very low discharge energy, i.e., 0.36 and 0.45 μJ, if the sample is not coated with Au due to excessive short circuit occurrence. Corresponding voltage and capacitor value for these energy levels are 85 V, 0.1 nF, and 95 V, 0.1 nF, respectively. It can be remarked from Fig. 4 that almost no short circuit occurred while μ-WEDMing gold-coated silicon samples as compared to uncoated Si. The likely cause behind this could be as follows: when uncoated silicon is machined, the system detects mostly open circuit because of its high resistivity, which causes the servo system to follow the forward path, and when

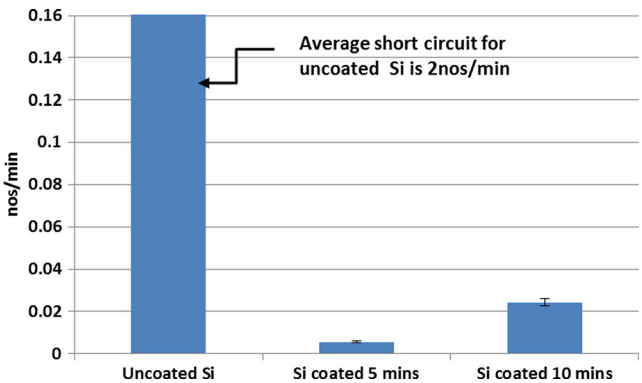


Fig. 4 Study of machining stability in terms of occurrence of short circuit (nos/min) during machining process. *Y*-scale range is kept to 0.16 to show values of "Si coated 5 min" and "Si coated 10 min"

the wire touches the silicon, it detects the short circuit. Therefore, the μ-WEDMing of uncoated silicon generates significant number of short circuits (nos/min) during operation, which retards the machining rate and also causes unevenness in the machined slots. It is also noted from Fig. 4 that Si(2) samples caused slightly higher short circuits than Si(1) samples; however, this difference is insignificant and only observed in two experiments which could be due to false detection of short circuit by the EDM controller of the machine.

4.1.2 Kerf width study

Kerf width is a vital factor to study in μ-WEDM-related research as this parameter determines the resolution of the fabricated feature. Two effects need to be considered during the study of kerf width of the machined slots by WEDM. First is the average value of kerf width, and second is the evenness or uniformity of the slot. In this study, kerf width was measured using the SEM microscopy at five different points of each slot. A parameter named as unevenness factor of the slot has been calculated, which is the standard deviation of these five values of width of the single slot. Higher value of this factor indicates more uneven slot. Figure 5 shows the variation of kerf width of the machined slot for different discharge energies for the three different samples. Figure 5a shows only one data for uncoated sample; this is because at very low discharge energy (85 V, 0.1 nF and 95 V, 0.1 nF) WEDM operation was not possible for this sample due to excessive short circuit detection during machining. The result shows for the case of coated silicon wafer the average slot width is somewhat higher compared to uncoated silicon wafer. This might be for the following cause; coating reduces resistance for the overall WEDM setup as mentioned earlier. Therefore, this helps to generate bigger spark, which results to larger kerf width. Interestingly, the study of unevenness factor for the three different samples shows (Fig. 6) uncoated Si produces significantly uneven slot as compared to coated Si (~3 times higher than Si(1) and ~1.5 times higher than Si(2)). In fact, this is expected because it is related to the results of machining stability as shown in Fig. 4. When the sample is not coated with gold or any other conducting material, the machining is unstable due to high resistivity at the machining zone as explained in Section 2. However, in the case of coated sample, resistivity at the machining zone goes down with the increase in coating thickness (Fig. 2) and machining becomes smooth with less short circuit detection. During machining of uncoated Si by the μ-WEDM, the system behaves erratically with significant detection of short circuits. This indicates that

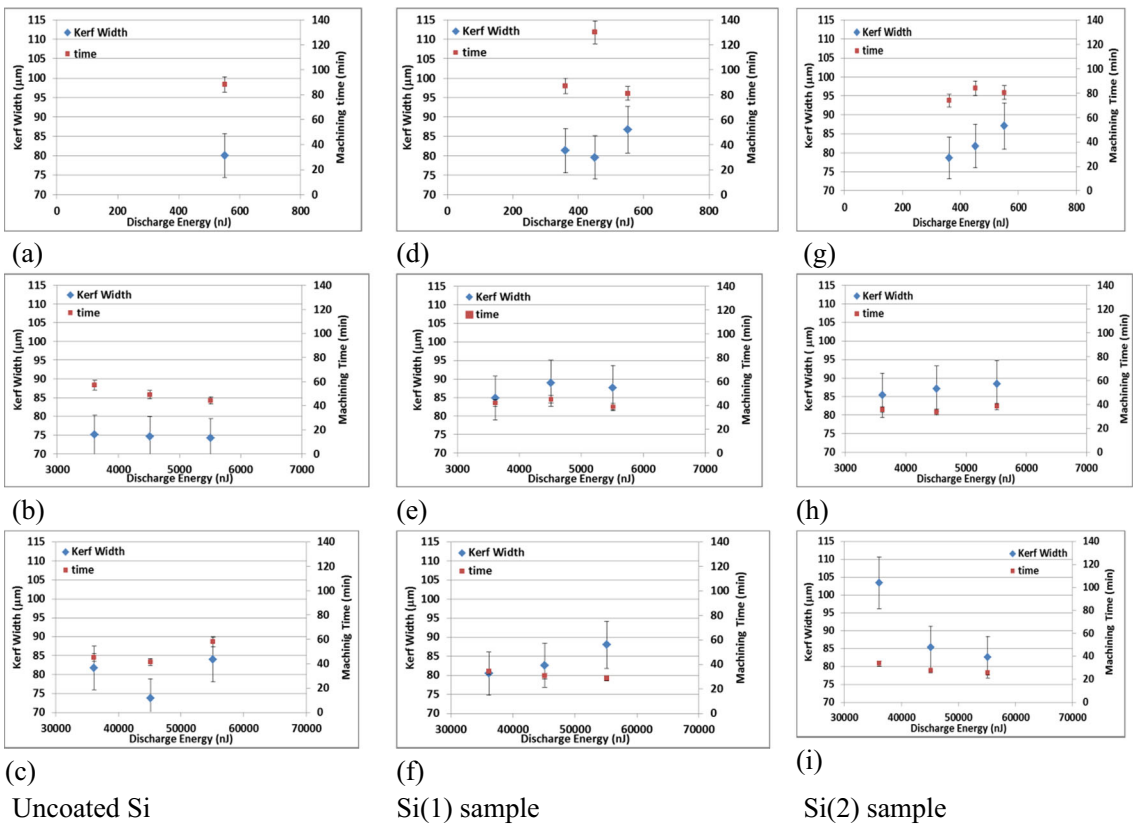


Fig. 5 Study of Kerf width with energy for three different Si samples: **a**, **d**, and **g** for low discharge energy; **b**, **e**, and **h** for medium discharge energy; **c**, **f**, and **i** for high discharge energy

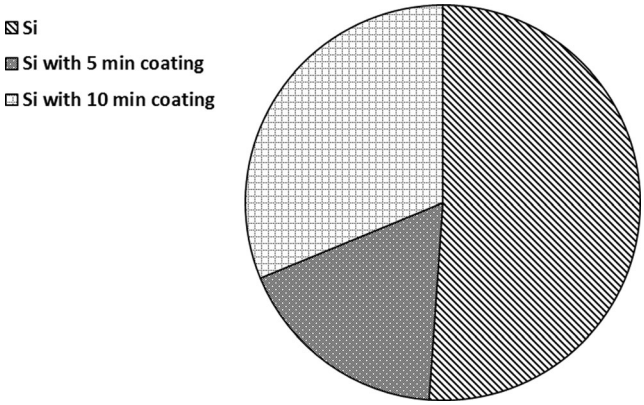


Fig. 6 Overall relative measurement of unevenness factor of the machined slots for three different samples

probability of physical contact between the wire and the Si workpiece is higher, and this may cause the wire to be pulled and misplaced. When spark generates at this condition, machined slots eventually becomes uneven. However, for the case of the Si(2) samples, the unevenness factor was observed to be higher than the Si(1) samples. During machining with Si(2) samples, the conductivity of the samples was high enough that might have caused few irregular big spark; hence, the unevenness in the machined slot.

In order to understand the variation of kerf width with discharge energy, it is necessary to examine the machining time as well. Generally, it is expected that kerf width should increase with increase in discharge energy, hence with applied voltage and capacitance [20], which is also the case for results described in Fig. 5f–h. However, it was found that, in some cases, lower discharge energy generates larger kerf as shown in Fig. 5b, c, e, and i. Probable reason behind this could be as discussed, during machining with lower energy levels in these particular cases; the machining time was longer (as shown in Fig. 5), and tool wire was in near contact with the workpiece for prolonged duration that resulted larger kerf size even in lower energy. However, in a particular case of Si(1) sample at a machining condition of 95 V and 0.1 nF, it was found that machining time was significantly larger than previous lower discharge energy; yet, the kerf width was found to be smaller. The result is described in Fig. 5d. For this particular sample, the machined slot was found to be rather uneven with high standard deviation, which indicates some sort of instability during machining; hence, this type of inconsistent result was observed.

4.1.3 Material removal rate study

The research on the μ-WEDMing operation aims to achieve the high MRR (ratio of removal volume to machining time). In order to study, this 1-mm long slot was machined with various parameters for three different Si samples. Dimensions of each groove were measured using the SEM to calculate the removed volume of the slot, hence the MRR. The slots width (kerf width) was measured in five different places, and average value was considered for calculation. It was observed that MRR is much higher for gold-coated Si as compared to uncoated Si. In the case, Si(1) minimum improvement on MRR was found to be ~18 % at 105 V and 0.1 nF machining condition and maximum improvement was ~114 % at 105 V and 10 nF machining condition. For Si(2) MRR was increased even higher. At 105 V and 0.1 nF, it was increased by ~20 %, and at 105 V and 10 nF, it was increased by ~123 % as compared to uncoated Si. Figure 7 also displays the evidence of enhanced material removal rate for Si coated by gold. It can be observed in Fig. 7 that MRR increases with discharge energy for coated Si. However, in the case of WEDMing of uncoated Si, machining was not possible at low discharge energy (minimum discharge energy required for machining was ~550 nJ for uncoated Si). Further, it was found that MRR is decreasing with increase in discharge energy for uncoated Si sample (for 10 nF, MRR is decreasing from 85 to 105 V and for 105 V MRR is decreasing from 1 to 10 nF), which is contradictory with previous results [20]. The possible reason behind this phenomenon could be this, while machining uncoated Si by WEDM the kerf width was discovered to be rather wavy with high level of inconsistency (in terms of standard deviation of five measurement points); therefore, average kerf width measured might have been overestimated and MRR was found to be high in some low discharge energy level. In the theoretical background section, it has been explained that the combined resistivity of the Au–Si–Au is significantly reduced because of the high conductivity of Au. Researchers [25] showed in their $\lambda-\theta-\rho$ theory that resistivity of the workpiece material is a very important parameter for the machinability study of the EDM/WEDM, where ρ, λ, and θ are the electrical resistivity, the thermal conductivity, and melting point of the workpiece, respectively. The theory includes the electrical resistivity of the workpiece material (ρ) because it involves the electric current transfer to create the discharge pulse. If the resistivity of the material is decreased the ease of machining by the EDM/WEDM is enhanced. The machining rate of gold-coated silicon is observed to be much higher because of the above-mentioned phenomenon. This confirms the process model, which predicts that equivalent resistivity for coated Si is higher and will enhance the machining rate. Another key factor behind higher machining rate for coated Si is related to the stability issue of the machining. As discussed earlier (Section 4.1.1), short circuit detection

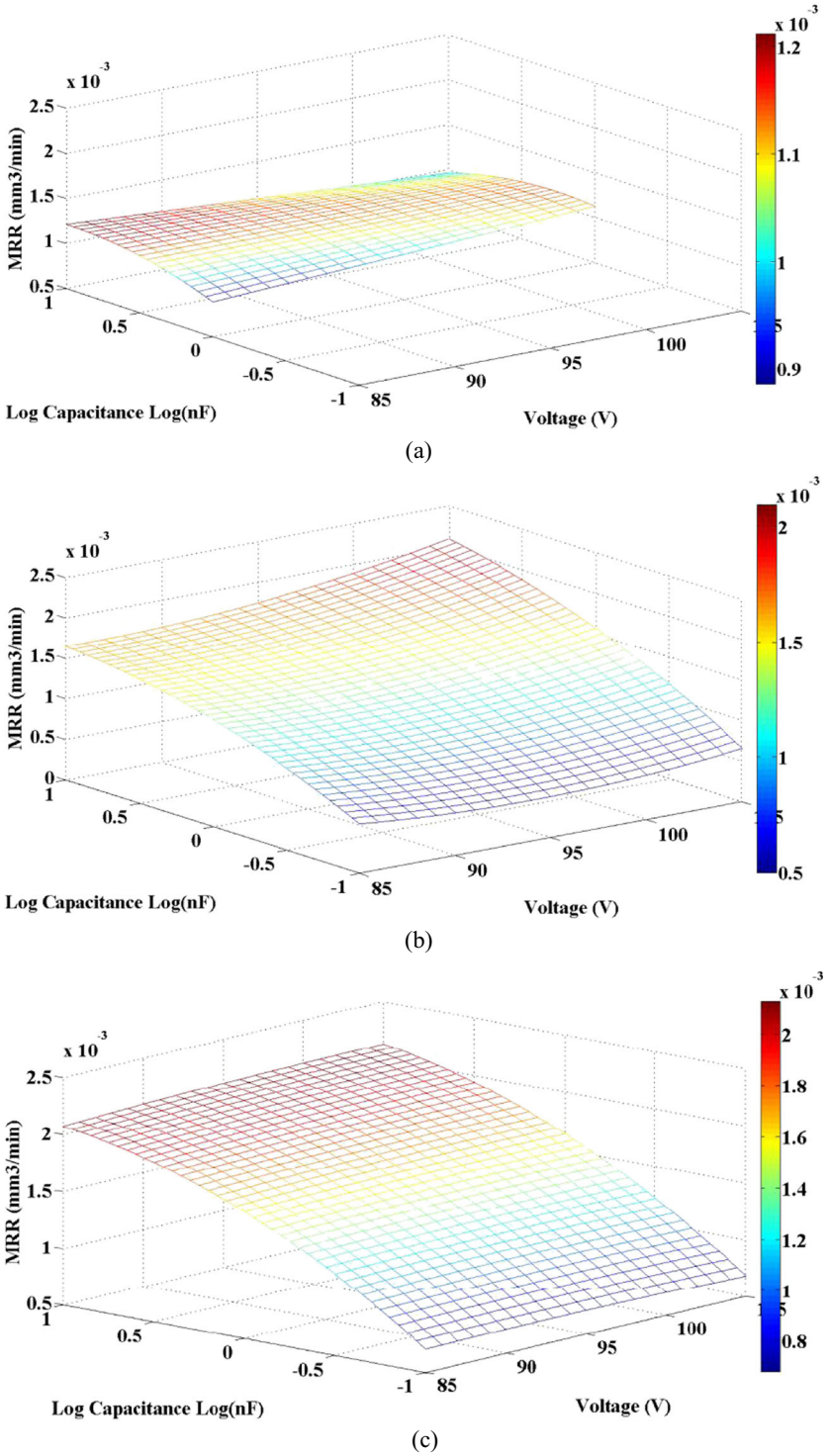


Fig. 7 Study of material removal rate (MRR) with working voltage and applied capacitance: **a** uncoated Si, **b** Si(1), and **c** Si(2)

is significantly high for the μ-WEDMing of uncoated Si wafer, which retards the machining rate of the material. It was also observed that at lowest energy level (85 V and 0.1 nF; 95 V and 0.1 nF) machining was not possible for uncoated Si wafer because of continuous detection of the short circuit.

4.1.4 Surface morphology study

Surface morphology is one of the most important parameters in manufacturing. In this study, coating process is the influencing factor, which determines the surface morphology of different machined samples (uncoated Si,

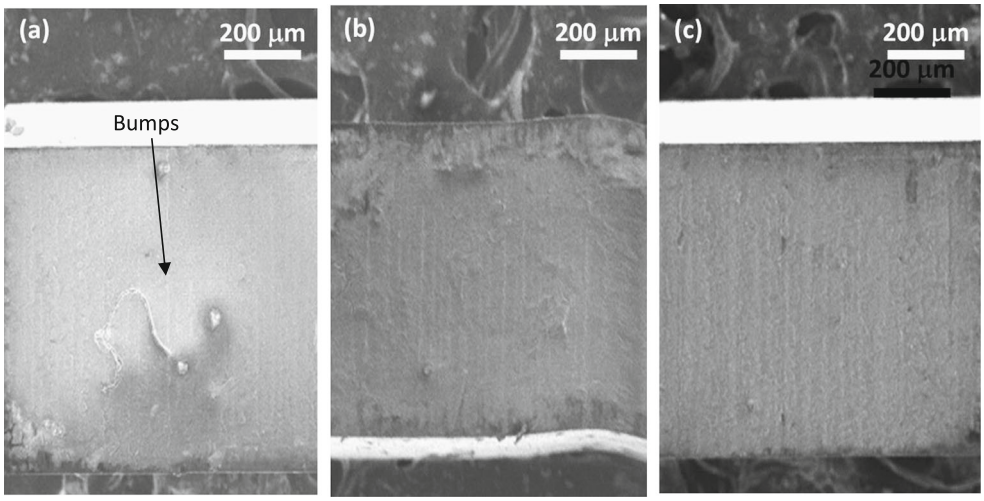


Fig. 8 SEM image of the cut surface of the machined slots by μ-WEDM process with machining condition of 95 V and 1 nF for **a** uncoated Si, **b** Si(1), and **c** Si(2)

Si(1), and Si(2)) for the same machining conditions. To study the morphology of the μ-WEDMed surface of the coated and uncoated Si wafer, the SEM imaging was carried out as shown in Fig. 8. Samples were machined under same machining conditions (105 V and 0.1 nF). It is clear that machined surface for uncoated Si wafer is quite rough with visible bumps, whereas machined surface for coated Si wafer (10 min) is remarkably smoother. However, surface quality of Si(1) falls in between. Stability of machining could be one reason for enhanced surface quality for WEDMed surface for gold-coated Si. Further, during machining, gold-coated Si spark generation was consistent, which led to smoother surface quality; on the other hand, inconsistent spark generation for uncoated Si made the machined surface rough with visible bumps.

4.2 Study of μ-EDM for coated Si

Effect of gold coating on Si wafer was also examined for μ-EDMing operation as well. Blind holes were drilled (programmed depth of 50 μm) with different machining parameters on three different types of samples, i.e., uncoated Si, Si(1), and Si(2). All the results of μ-EDM experiments are discussed in this section.

4.2.1 Study of μ-EDM stability

The number of short circuits occurrence was also counted during the μ-EDM operation. Figure 9 shows occurrence of short/ arcing (nos/min), for the machining of gold-coated silicon and uncoated silicon at different machining conditions. In all the cases except for 105 V and 0.1 nF, it has been observed that the μ-EDMing of coated Si wafer is more stable than uncoated Si wafer. However, the effect is more apparent at higher energy (85 V and 10 nF) than lower energy. Possible reason for stable machining for coated Si workpiece is the conductive coating that reduces the contact resistance between the workpiece and work table. It is worthy to mention how the machine detects the short circuit during machining to explain why higher short circuit detection for Si(1) samples than Si(2)

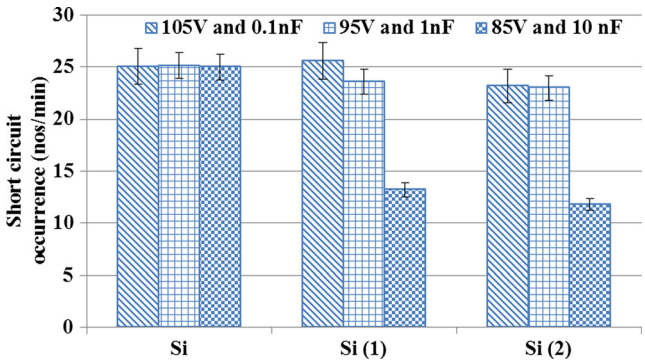


Fig. 9 Number of short circuits occurrence for three different samples at different machining parameters

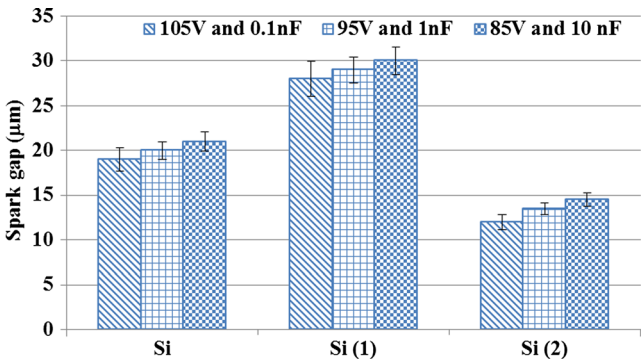


Fig. 10 Spark gap variation in μ-EDMing for three different samples at different machining conditions

Table 2 Difference in μ-EDM Machining time

Sample type	Voltage value (V)	Capacitance value (nF)	Machining time (min)
Si	85	10	88.2166
Si(1)	85	10	8.2
Si(2)	85	10	9.0333
Si	95	1	39.0333
Si(1)	95	1	15.0833
Si(2)	95	1	14.9333
Si	105	0.1	43.2833
Si(1)	105	0.1	26.2
Si(2)	105	0.1	21.7833

samples. The machine basically monitors the discharge current and compares it with a threshold value electronically to generate the short circuit input for the motion controller. The short circuit detection sensitivity is fixed and cannot be altered by the user. The possible reason for higher short circuit detection for Si(1) sample could be as follows. Si(1) and Si(2) coating both reduces contact resistance as explained earlier. However, overall bulk body resistance is higher for Si(2) sample due to higher thickness, which reduces the discharge current amount. On the contrary, discharge current is higher for Si(1) sample, which may lead to false detection of short circuit during machining process under present short circuit detection sensitivity. However, this can be confirmed if one can vary the sensitivity parameter.

4.2.2 Spark gap study

As shown in Fig. 10, in all the three machining processes, the same ratio of difference in spark gap can be seen in the three samples and always Si(1) records the highest, while Si(2) records the lowest spark gap. It is sometimes observed for the machining of uncoated Si that the tool physically touches the workpiece because of high resistivity and wobbles around the hole to create secondary sidewise spark and makes the resultant hole larger, hence the spark gap. However, for the case Si(1) and Si(2) samples, the phenomena is different. It is explained in Section 4.2.1 that, due to low bulk resistance, the Si(1)-coated sample produces larger spark with high discharge current and leads to false detection of short circuit. This large spark also produces larger diameter for the hole than Si(2) sample.

4.2.3 Study of material removal rate

Machining time for all the μ-EDM experiments are shown in Table 2. This table presents the difference in machining time in the μ-EDMing among the three samples (uncoated Si, Si(1), and Si(2)) under the same machining parameters. It can be understood that uncoated sample took significantly longer machining time than coated sample. Figure 11 shows the variation of MRR at different machining conditions for three different types of samples. It is very clear that machining rate or MRR for gold-coated silicon samples is much higher than uncoated silicon sample, especially in high discharge energy process (85 V and 10 nF). This enhancement of MRR of coated Si is due to the low contact resistance as explained in Section 4.2.1. It has been already discussed that Si(1) sample may produce higher discharge current due to low bulk resistance (this is also supported by spark gap study discussed earlier), which causes higher material removal (in single spark) with bigger spark. This leads to high MRR value for Si(1) sample. In the case of low discharge energy (105 V and 0.1 nF), machining time for Si(1) (due to higher short circuit detection as shown in Fig. 10) sample is quite high and that overall MRR is lower than that of the Si(2) sample.

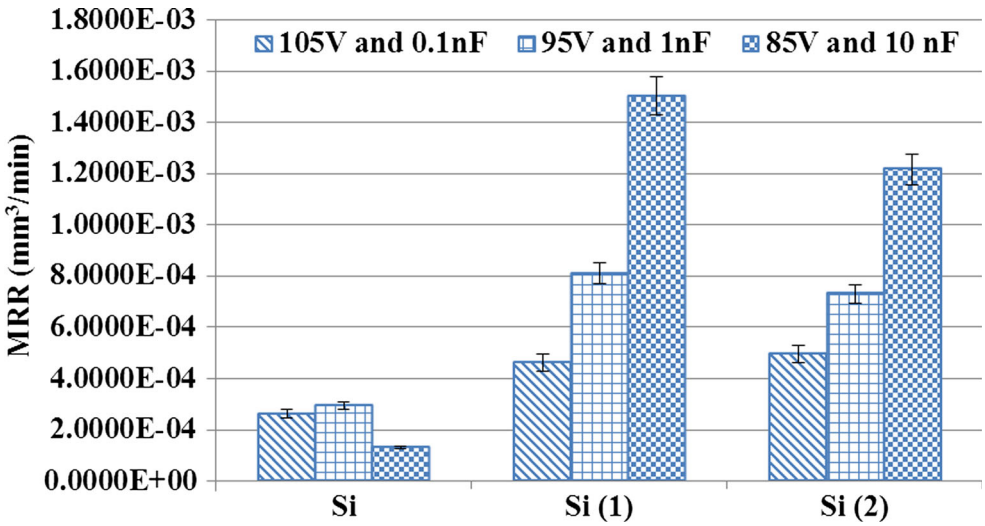


Fig. 11 Variation of MRR in μ-EDM for three different samples at different machining conditions

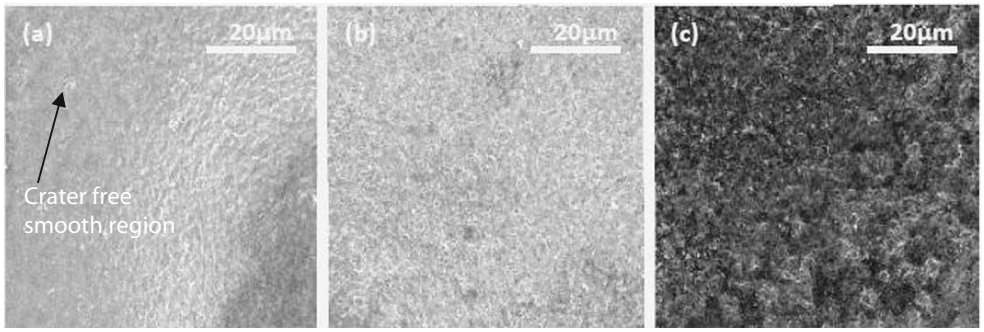


Fig. 12 Zooming SEM image of the machined hole by μ-EDM process with machining condition of 105 V and 0.1 nF for **a** uncoated Si, **b** Si(1), and **c** Si(2)

4.2.4 Surface morphology study

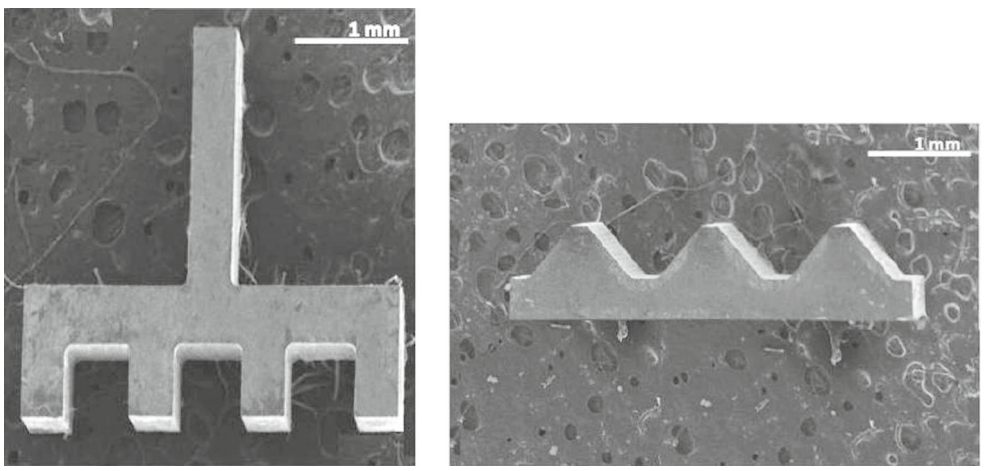
To study the morphology of the μ-EDMed surface of the coated and uncoated Si wafer, the SEM imaging was carried out as shown in Fig. 12. It is clear that machined surface for uncoated Si wafer and machined surface for Si(1) are almost similar. However for uncoated Si, there are some regions that are too flattened (shown by arrow), which indicates the presence of mechanical rubbing during EDMing operation. Si(1) sample has surface consisting of fine craters, whereas Si(2) has coarse craters as shown in Fig. 12c. As discussed earlier, due to high bulk resistance, the spark was less and non-uniform, which may have led to this type of surface for Si(2).

5 Fabrication example

In order to test the feasibility of the developed machining process in real engineering application, two different samples were fabricated. Electrostatics μ-actuator is the widely used in MEMS-based application. In industry, it is used in μ-resonators, switches, μ-mirrors, etc. In this case, rapid prototyping of miniature electrostatics actuator was carried out using this proposed WEDM process. This process is more advantageous for batch mode production as photolithography based fabrication requires involvement of different types of machines with high cost. Sample of the Si(1) was used to produce this product under 95 V and 1 nF as machining conditions. Figure 13a shows the SEM image for the product. The mini actuator has a long rod with 2 mm length and 400 μm width. The pitch width between each actuator tooth is 650 μm.

Another mini-digital reflector was also machined by the μ-WEDM (Fig. 13b) using the same sample of the Si(1) under the same machining conditions (95 V and 1 nF). This miniature digital reflector can be used as linear displacement sensor in two directions (horizontal and verticle movement). The working principle of this device is the same as digital encoder. The mini-reflector length is 3.6 mm, which has three trapezoidal reflector teeth; the average pitch width of each tooth is 500 μm. The trapezoidal shape for the cam provides two degrees of freedom in measurement.

Finally, samples were tested with electron dispersive X-ray (EDX) after selective etching of gold (Au) layer from Si substrate to confirm complete removal of the coating material after finishing the μ-EDMing/ μ-WEDMing operation. Figure 14 shows EDX analysis of original sample, gold-coated sample, and sample after removal of the gold. This figure confirms that gold can be successfully etched from Si substrate. The source of C in the EDX result is the kerocene-



(a) (b)

Fig. 13 **a** SEM image of electrostatic μ-actuator with machining condition of 95 V and 1 nF. **b** SEM image of μ-digital reflector with machining condition of 95 V and 1 nF

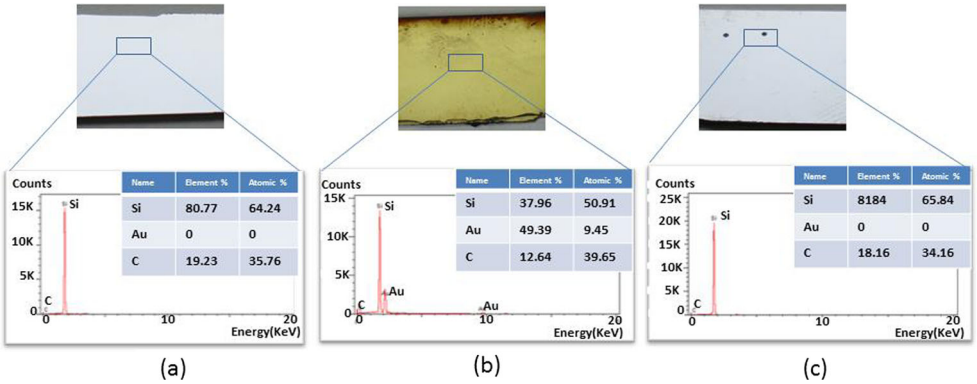


Fig. 14 Electron dispersive X-ray (EDX) analysis of samples: **a** Original Si, **b** gold-coated Si substrate, and **c** Si substrate after removal of gold

based EDM oil that was used as dielectric medium during the experiment. Selective etching process that has been used here is wet etching method, using dilute aqua regia (HCL, HNO_3, and H_2O) without damaging the Si substrate as explained earlier.

6 Conclusion

In this study, a new method is proposed for machining polished Si (p-type; resistivity, 1–50Ω cm) wafer. In this method, initially, Si workpiece is coated with a conductive material (gold for this study) and then μ-WEDM/EDM operation is carried out. Three groups of samples have been prepared for machining (uncoated Si, Si(1), and Si(2)). Finally, after the WEDM/EDM operation, the conductive layer is removed from the polished Si substrate without damaging the substrate.

Following conclusions can be made from study related to μ-WEDM experiments.

- μ-WEDMing operation is definitely impossible at very low discharge energy (~<451.25 nJ) if the sample is not coated with gold, while it is very easy to machine the coated samples for the same discharge energy.
- In machining stability issue, coating process greatly enhanced the machining stability (~100× better in the coated samples).
- Material removal rate (MRR) for coated silicon samples is much higher than uncoated silicon samples (~2× higher in Si(1) or Si(2)). This proves the hypothesis of this research that coating process will enhance the machining of Si by reducing combined resistivity of the Au–Si–Au composite.
- Kerf width study showed that the average slot width is somehow bigger in the case of coated Si samples compared to uncoated Si.
- Unevenness study showed that uncoated Si produces uneven slot, with unevenness factor 3× larger than Si(1) and about 1.5× higher than Si(2).
- Morphological study by SEM showed visible bumps for uncoated Si machined by WEDM, whereas for coated Si, the machined surface is very nice and smoother. Again, coating process enhanced the surface morphology of the WEDMed surface.

The following points can be concluded from the μ-EDM study.

- In machining stability issue, the μ-EDMing of coated Si is more stable than uncoated Si except for 105 V and 0.1 nF (low discharge energy). In this case, the Si(1) sample in the low discharge energy (recorded lower machining stability) may lead to false detection of short circuit under present short circuit detection sensitivity.
- The MRR for gold-coated silicon samples is much higher than uncoated silicon sample (about 2 to 3× in low discharge energy and about more than 7× in high discharge energy).
- In spark gap study, secondary sidewise spark was created in uncoated Si because of the high resistivity that resulted in high spark gap. While Si(1) coating recorded the highest spark gap, because of the low bulk resistance which produced larger spark, Si(2) recorded the lowest spark gap due to its high bulk resistance.
- The μ-EDMed surface of uncoated Si has region that is too flattened, which indicates presence of mechanical rubbing. Si(1) has surface of fine craters, while, due to high bulk resistance of Si(2) coating, the spark was less and non-uniform, which led to coarse craters.

References

1. Ho KH, Newman ST (2003) State of the art electrical discharge machining (EDM). Int J Mach Tools Manuf 43(13): 1287–1300. http://dx.doi.org/10.1016/S0890-6955(03)00162-7
2. Ho KH, Newman ST, Rahimifard S, Allen RD (2004) State of the art in wire electrical discharge machining (WEDM), International Journal of Machine Tools and Manufacture, Volume 44, Issues 12–

13, Pages 1247–1259, ISSN 0890–6955, http://dx.doi.org/10.1016/j.ijmachtools.2004.04.017
3. Masuzawa T (2000) State of the art of micromachining. CIRP Ann Manuf Technol 49(2):473–488
4. Yu ZY, Masuzawa T, Fujino M (1998) Micro-EDM for three-dimensional cavities—development of uniform wear method. CIRP Ann Manuf Technol 47(1):169–172
5. Rajurkar KP, Yu ZY (2000) 3D micro-EDM using CAD/CAM. CIRP Ann Manuf Technol 49(1):127–130
6. Anwar MM, Saleh T, Madden JDW, Takahata K (2014) Micropatterning polypyrrole conducting polymer by pulsed electrical discharge. Macromol Mater Eng 299(2):198–207
7. Saleh T, Dahmardeh M, Bsoul A, Nojeh A, Takahata K (2011) Field-emission-assisted approach to dry micro-electro-discharge machining of carbon-nanotube forests. J Appl Phys 110(10):7
8. Saleh T, Dahmardeh M, Bsoul A, Nojeh A, Takahata K (2012) High-precision dry micro electro-discharge machining of carbon-nanotube forests with ultralow discharge energy. 2012 I.E. 25th International Conference on Micro Electro Mechanical Systems (MEMS)
9. Saleh T, Dahmardeh M, Nojeh A, Takahata K (2013) Dry micro-electro-discharge machining of carbon-nanotube forests using sulphur-hexafluoride. Carbon 52:288–295
10. Reynaerts D, Heeren PH, Brussel HV (1997) Microstructuring of silicon by electro-discharge machining (EDM).1. Theory. Sensors and Actuators a-Physical 60(1–3):212–218
11. Luo YF, Chen CG, Tong ZF (1992) Investigation of silicon wafering by wire EDM. J Mater Sci 27(21):5805–5810
12. Peng WY, Liao YS (2003) Study of electrical discharge machining technology for slicing silicon ingots. J Mater Process Technol 140: 274–279
13. Wang W, and Liu ZD (2009) High efficiency slicing of low resistance silicon ingot by wire electrolytic-spark hybrid machining. J Mater Process Technol 209(7):3149–3155. http://dx.doi.org/10.1016/j.jmatprotec.2008.07.029
14. Okamoto Y, Uno Y, Okada A, Ohshita S, Hirano, T. and Takata S (2008) Development of multi-wire EDM slicing method for silicon ingot. Proceedings of ASPE Annual Meeting and the 12th ICPE
15. Crawford GA (2012) Process characterization of electrical discharge machining of highly doped silicon. Master of Science Thesis in Mechanical Engineering, Massachusetts Institute of Technology, USA
16. Staufert GA, Dommann V, Lauger D (1993) Behaviour of a silicon spring fabricated by wire electro-discharge machining. J Micromech Microeng 3(4):4
17. Rakwal D, Heamawatanachai S, Tathireddy P, Solzbacher F, Bamberg E (2009) Fabrication of compliant high aspect ratio silicon microelectrode arrays using micro-wire electrical discharge machining. Microsyst Technol Micro Nanosyst -Inf Storage Process Syst 15(5):789–797
18. Yu PH, Lin YX, Lee HK, Mai CC, Yan BH (2011) Improvement of wire electrical discharge machining efficiency in machining poly-crystalline silicon with auxiliary-pulse voltage supply. Int J Adv Manuf Technol 57(9–12):991–1001
19. Zhidong L, Haoran C, Huijun P, Mingbo Q and Zongjun T (2014) Automatic control of WEDM servo for silicon processing using current pulse probability detection. Int J Adv Manuf Technol. Published Online 30 Aug 2014. doi:10.1007/s00170-014-6252-2
20. Jahan MP, Lieh TW, Wong YS, Rahman M (2011) An experimental investigation into the micro-electrodischarge machining behavior of p-type silicon. Int J Adv Manuf Technol 57(5–8):617–637
21. Song X, Meeusen W, Reynaerts D, Brussel HV (2000) Experimental study of micro-EDM machining performances on silicon wafer. Proc SPIE 4174, Micromachining and Microfabrication Process Technology VI:331. doi:10.1117/12.396450
22. Takino H, Ichinohe T, Tanimoto K, Yamaguchi S, Nomura K, Kunieda M (2004) Cutting of polished single-crystal silicon by wire electrical discharge machining. Precis Eng-J Int Soc Precis Eng Nanotechnol 28(3):314–319
23. Takino H, Ichinohe T, Tanimoto K, Yamaguchi S, Nomura K, Kunieda M (2005) High-quality cutting of polished single-crystal silicon by wire electrical discharge machining. Precis Eng-J Int Soc Precis Eng Nanotechnol 29(4):423–430
24. Rasheed AN, Asan GA, Saleh T (2013) Enhancing μ-wedming (wire electro-discharge machining) of polished silicon wafer by conductive coating. J Manufact Tech Res 5(1–2):1–17
25. Mahardika MT, Tsujimoto, Mitsui K (2008) A new approach on the determination of ease of machining by EDM processes. Int J Mach Tools Manufact 48(7–8):746–760
26. Masanori K, Satoyuki O (2000) Improvement of EDM efficiency of silicon single crystal through ohmic contact. Precis Eng 24:185–190