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ORIGINAL ARTICLE

# The development of automated solder bump inspection using machine vision techniques

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**Abstract** Visual inspection is an important task in the manufacturing processes for integrated circuit boards. In this paper, we focus on the solder bump inspection problem, and an automated visual inspection method using machine vision techniques is proposed. The solder bump inspection method consists of image grabbing, image preprocessing, feature extraction, and defect detection and classification. Five defect types of solder bumps to be inspected are bridging solder, excess solder, incomplete solder, non-wetting, and missing solder. The solder area, the number of edge pixels, the deviation from center, and the deformation ratio are used as the features for solder bump defect detection and classification. The proposed method is a hybrid algorithm, and it consists of two stages: the training stage and the inspection stage. The experimental results show that the proposed method is effective in detecting defects of solder bumps.

**Keywords** Machine vision · Inspection · Solder bump · Feature extraction · Image preprocessing

## 1 Introduction

Machine vision techniques have been developed to solve many problems in manufacturing systems since the past years. In most automated manufacturing environment, the need of flexibility and reliability is important. Since machine vision proved to be useful in automated visual inspection, many automated visual inspection approaches have been surveyed [1–6].

Inspection is the process of determining whether a part deviates from one or some specifications [3]. It is known that the inspection operation is usually the largest single cost in manufacturing [1, 2]. It is well known that humans tend to make mistakes in the inspection task. The need of a 100 % inspection operation is very important in electronic industry because it can assure the quality of products and reduce the cost due to defective products. Various applications of automated visual inspection for electronic parts have been studied [7–24].

Chang et al. proposed a method for integrated circuit (IC) print mark quality inspection [7]. Chiou presented an intelligent method of selecting segmentation algorithm for real-time defection system [8]. Derganc et al. proposed a machine vision system for measuring eccentricity of bearings [9]. Edinbarough et al. proposed a neural network-based vision inspection monitoring system for electronic manufacturing [10]. Lahajnar et al. introduced a method for inspecting electric plates [11]. Liao et al. used the partial Hausdorff distance and the support vector machine classifier to inspect printed circuit board (PCB) defects [12]. Lin used the discrete transform decomposition and cumulative sum techniques to tiny defect inspection of electronic components [13]. Perng et al. reported a method to inspect two types of LED surface mounted devices [14]. Sun et al. utilized the Hooke–Jeeves pattern search with particle swarm optimization to post-slicing inspection of silicon wafers [15]. Sun et al. proposed an electric contacts inspection method using three views [16]. Tien et al proposed a microdrill inspection method using a series of image processing procedures [17]. A non-referential self compared method for bond pads inspection was introduced by Tsai and Su [18]. Wang et al. proposed a method for post bonding inspection [19]. Wu et al. introduced a reference-based method to detect and classify

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defects in PCBs [20]. Zhang et al. used a reference method to the problem of post-sawing inspection in IC encapsulation [21]. Zhou et al. presented a detection rule for inspecting extrusion defects in IC packages [22]. Perng et al. developed a wire bonding inspection method [23]. Both of 2D and 3D defects can be detected. Rau and Wu proposed a five-stage method to detect eight types of defects in the inner layer of printed circuit board [24].

One of the most important problems in automated inspection for integrated circuit boards (ICBs) is to recognize the defects of solder joints on the ICBs. Many automated visual inspection methods for solder joints have been developed [25–33]. Chiu and Perng used one layer of light, and two features classify the insufficient, acceptable, and excessive solders [25]. In their method, the location and the size of a pad are known. So it can segment the solder joint from the background precisely. Jiang et al. established a background remover-based approach for PCB solder joint inspection [26]. The solder joint locations are first identified using background remover. Nine binary image-based features and seven gray value-based features are used to detect and classify three types of defects. Kim et al. proposed a defect classification method for solder joints in SMD [27]. Both of the 2D and 3D features are used in their study. The inspection method combines the backpropagation algorithm of neural networks and the Bayes classifier. Loh and Lu analyzed the reflection of the surface-mounted device to detect defects [28]. A structured lighting was used in their study. Mar et al. present a solder joint classification system using two inspection modules [29]. The Log–Gabor filter and classifier fusion are used in the classification of five types of solder joints. Teoh et al. presented a method for inspecting defects on surface mount PCBs [30]. Based on the characteristics of images, they developed a series of image preprocessing algorithms to reduce the complexity of images. Teramoto et al. used the oblique computed tomography to capture the images of BG-mounted substrates [31]. The OCT images are then analyzed. Five features are extracted and the solder bump is inspected by means of the linear discriminate analysis and neural network techniques. Xie et al. propose an improved AdaBoost method to inspect solder joints for chip component of mounted components on PCB [32]. Their proposed method can improve the classification accuracy and independency of features. A defect diagnosis decision tree is used to classify the defect types. Yun et al. used the tiered circular illumination technique to enhance the features of defects of the solder joints [33]. They proposed the support vector machine-based method to detect the four types of solder defects on the IC boards.

The above developed methods are very useful and can solve the solder joint inspection problem in many ways. In this paper, we propose a hybrid method for the automated visual inspection of the solder bumps. The proposed method consists of two stages. In the training stage, several template ICBs are used to find the positions and characteristics of solder bumps. The defects can then be detected in the inspection stage. In both of these two stages, a charged coupled device (CCD) camera is used to obtain digital images of the ICBs. A series of image preprocessing operations is applied to the image. Each solder bump is then segmented, and some features are extracted from the solder bumps on the IC board. Further, a classification rule is developed to detect and classify solder bump defects.

The proposed method for solder bump inspection will be introduced in the next section. In Section 3, it illustrates the experimental results of the proposed automated inspection method for solder bumps. Some concluding remarks are given in the last section.

## 2 Solder bump inspection method

The proposed method for the automated inspection of solder bumps on the IC boards can be expressed as in Fig. 1. From Fig. 1, the proposed inspection method consists of two stages: training stage and inspection stage.

In training stage, several perfect IC boards are used as the templates. For each template IC board, we used the CCD camera to grab images. After performing some image preprocessing operations, the position for each solder bump in an ICB can be determined, and it is used to identify each solder bump quickly in the next stage. In addition, some features of the solder bumps can be extracted, and means and standard deviations of the features can be computed. These means and standard deviations of features extracted from the perfect IC boards can be used to check if defects exist on the IC boards in the inspection stage.

The inspection stage consists of image grabbing, image preprocessing, feature extraction, and defect detection and classification. They are explained in the following sections.

### 2.1 Image grabbing

A CCD camera is used to grab solder bump image. In order to reduce the computation effort, the color images of the inspecting IC boards are grabbed and converted to gray scales firstly. Suppose that $g(x, y)$ is the gray level for a pixel with coordinate $(x, y)$. Further, $g^{\mathrm{R}}(x, y)$, $g^{\mathrm{G}}(x, y)$, and $g^{\mathrm{B}}(x, y)$ are the corresponding values of red, green, and blue components for a RGB color model. The color to gray scale transform can be expressed as

$$g(x,y) = 0.11 \times g^{\mathrm{R}}(x,y) + 0.59 \times g^{\mathrm{G}}(x,y) + 0.3 \times g^{\mathrm{B}}(x,y). \quad (1)$$

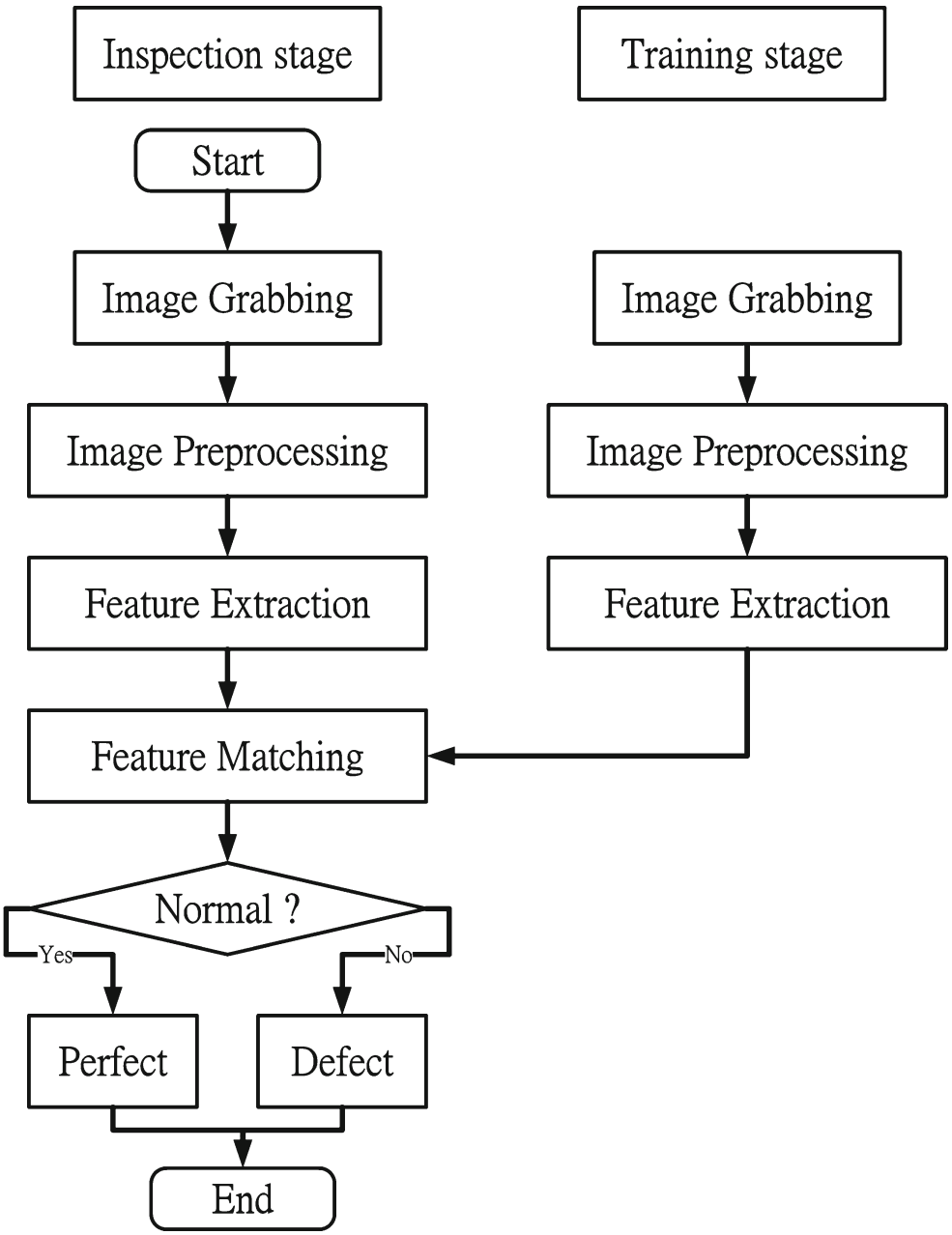



**Fig. 1** Flowchart for the automated visual solder bump inspection on the IC board

## 2.2 Image preprocessing

In order to enhance the features of the solder bumps, the images should undergo a series of image preprocessing operations, including noise reduction, thresholding, morphological operation, labeling, edge detection, and calibration.

### *2.2.1 Noise reduction*

A noisy image may reduce the accuracy of the subsequent image processing. The purpose of noise reduction is to restore the gray levels of pixels to the original values as much as possible. The median filter has the ability for preserving important features of electronic parts [34]. Therefore, we use the median filter to remove noise in the solder bump image. The gray level of the concerned pixel is replaced by the median of the gray levels of its neighbors.

### *2.2.2 Image thresholding*

In order to analyze the solder bumps, we need to separate the solder bump from the background. Figure 2a shows an example of color ICB image. The image of gray level is shown in Fig. 2b. Figure 2c is the histogram of gray levels of Fig. 2b. Figure 3 shows the binary images of Fig. 2b for different thresholds. It is seen that the solder bump inspection will be affected by the thresholding operation.

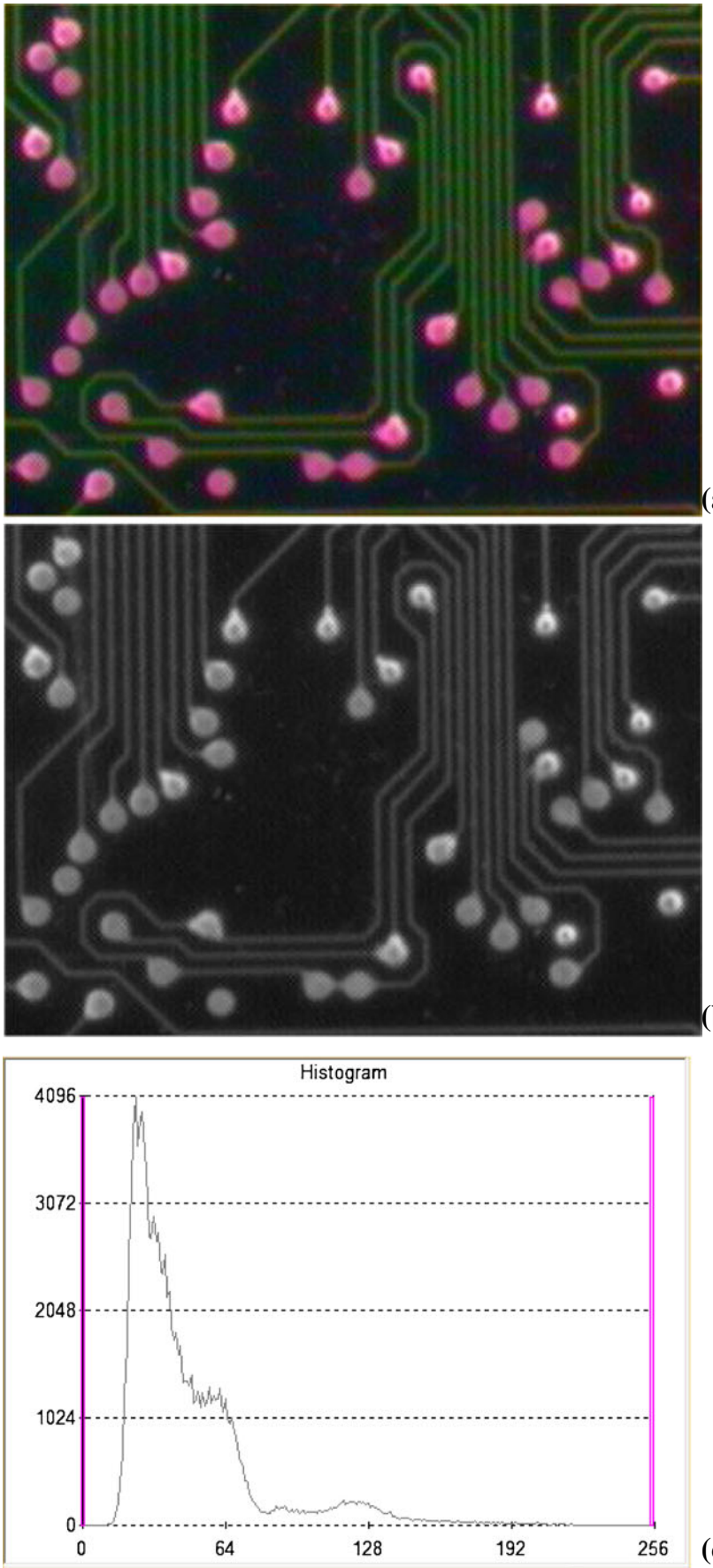



**Fig. 2** An example of solder bumps: **a** original image, **b** gray level, and **c** its corresponding histogram

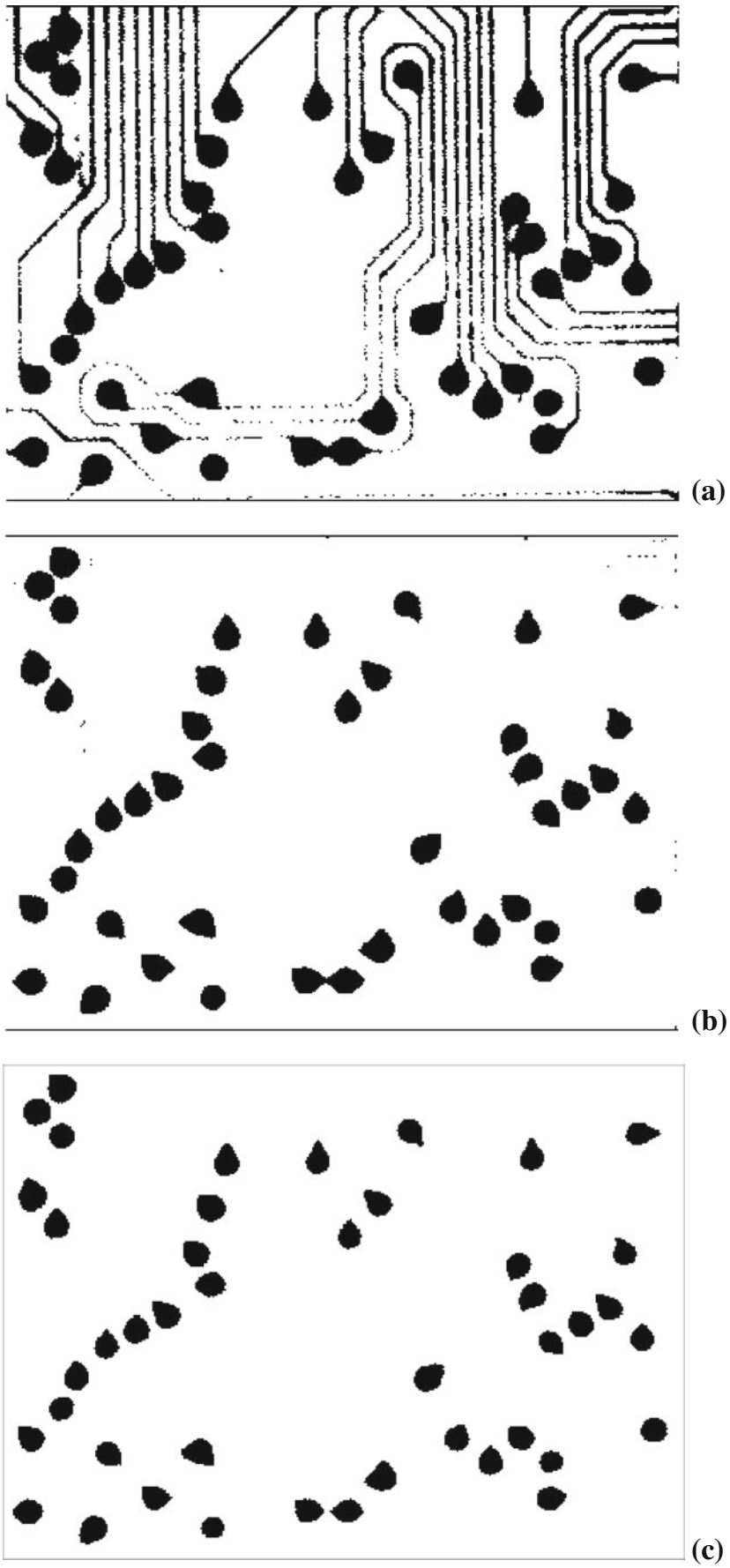



**Fig. 3** The results of binary images by different thresholds: **a** 60, **b** 80, and **c** 100

Many image thresholding approaches have been proposed for selecting the threshold to convert the gray level image to binary image. For speed consideration, we can use the images of perfect ICBs to find a threshold in the training stage. It will be used in the inspection stage to convert the gray level image into binary image.

### 2.2.3 Image opening and closing

The image of solder bump may be corrupted by noise during the thresholding process. To reduce the noise effect, the opening and closing operations can be used. They consist of two elementary operations (erosion and dilation), and they are the common used morphological operations [35]. Figure 4 shows a binary image to be processed with a 3×3 structure element and the result of applying the mathematical morphological operations. Figure 5 is an example of conducting both opening and closing operations to the image in Fig. 3c.

### 2.2.4 Image labeling

The labeling process is used to identify each isolated solder bump. Each solder bump which position of it has been determined in the training stage will be numbered. The information of positions can then be used to identify each solder bump. The image labeling will be quick because only a constrained region will be checked in the inspecting stage. Figure 6 shows an example of image labeling result of the solder bumps in Fig. 5. There are 44 solder bumps numbered, and the position of each solder bump can be identified.

### 2.2.5 Edge detection

In order to analyze the features of solder bumps, we need to find the edges of them. By performing edge detection, we can find the edge of solder bumps. Many edge detectors have been proposed. For a gray level image, the edges can be detected by a Sobel operator. Figure 7a shows the result of edge detection from the gray level image in Fig. 2b by the Sobel edge detector. It is seen that there are many noise occurred in the image. Especially, the edges of wires are also detected. Since we are only interested in the edges of solder bumps, instead of using the gray level image, the binary image is used to detect edges of solder bumps.

Since an image labeling process will be applied to the binary image, the edge detection can be done by a template method using predefined edge patterns in the same time [36]. Further, the coordinates of edges can be recorded during the template matching edge detection. The template method is effective in detecting edges and can be used with the labeling process. Each solder bump has been identified in the image labeling process, and the location of solder bump can be determined. The edge detection can only be applied to the region of each solder bump. It will also reduce the processing time. Figure 7b shows the result of edge detection of Fig. 5.

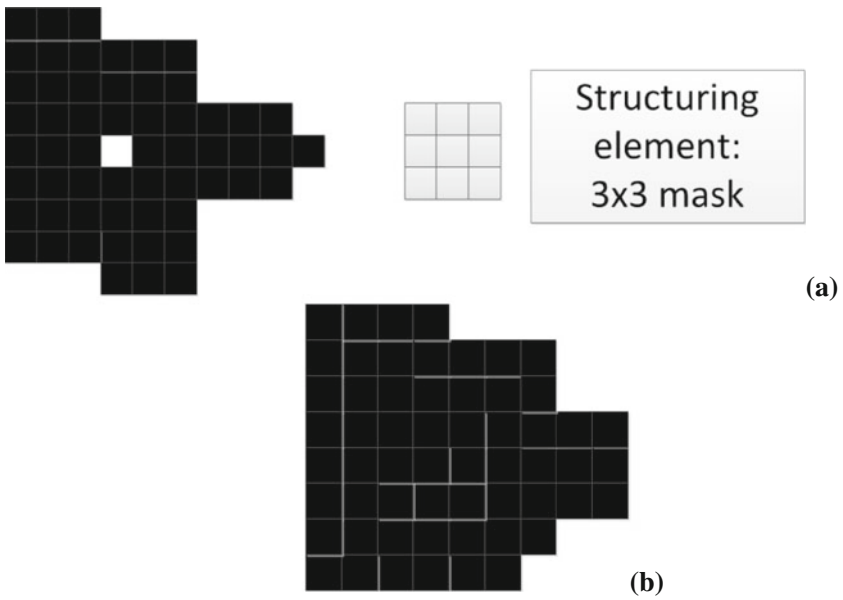



**Fig. 4** An example of **a** binary image and its 3×3 structuring element, **b** the result after applied opening and closing operations

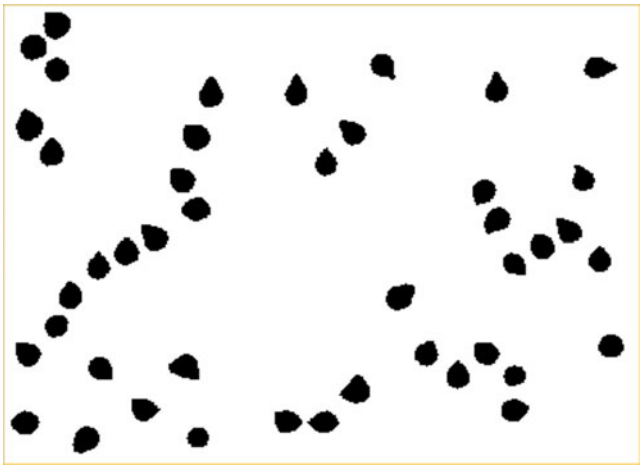


**Fig. 5** Results of morphological operations: opening and closing operations

### 2.2.6 Image calibration

The proposed method is a hybrid method. In order to find the missing bond defects, a calibration process should be performed. After calibration has been performed, the coordinate relationship between the template and inspecting IC boards can be determined. The positions of solder bumps can also been found, and the inspection can then be done bump by bump. The method of calibration is to search two calibration marks on the IC boards. Once the two marks have been located, the image of the inspecting IC board can be shifted and rotated to the standard orientation. Figure 8 shows the two marks in the referential and the inspecting image.

The two aligning marks in referential ICB can be determined in the training stage. The corresponding two aligning marks in the inspecting ICB can be determined

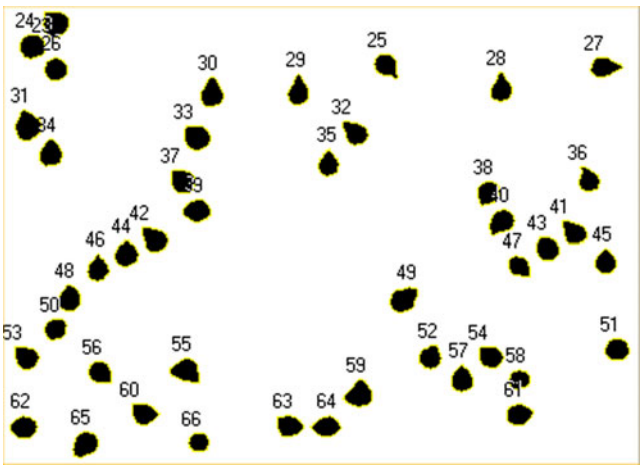
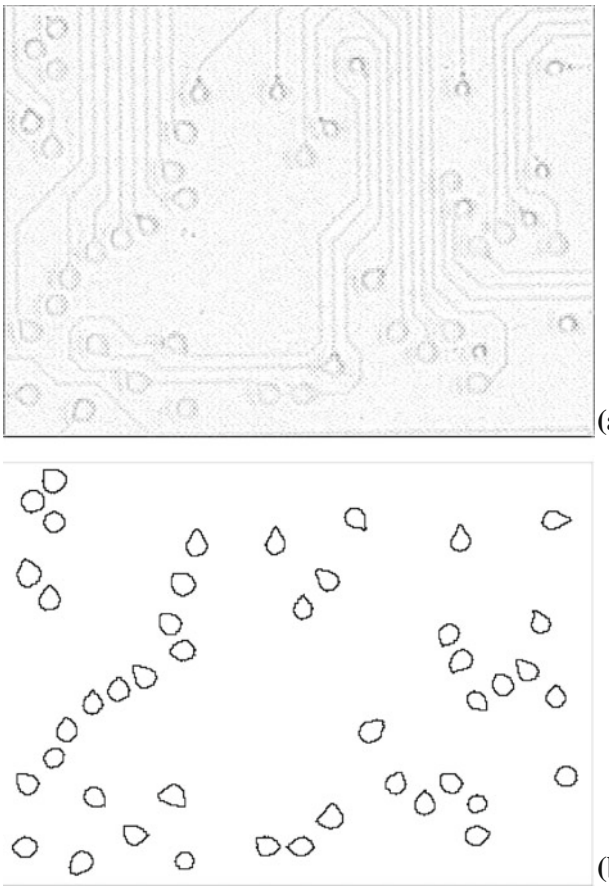



**Fig. 6** Image labeling: 44 solder bumps numbered (from no. 23 to no. 66)



**(a)**

**(b)**

**Fig. 7** Results of edge detection from: **a** gray level image and **b** binary image

using the coefficients of correlation. Figure 9 shows the computation of these values by overlapping the calibration mark of template to the inspecting image. Suppose that $t(i, j)$ and $g(i, j)$ are the gray levels of template and inspecting images. The coefficient of correlation in coordinate $(x, y)$ between two images is defined as the following equation:

$$r(x,y) = \frac{\sum_{i=1}^{m}\sum_{j=1}^{n}(g(i,j)-\overline{g}(x,y))(t(i,j)-\overline{t}(x,y))}{\sqrt{\sum_{i=1}^{m}\sum_{j=1}^{n}(g(i,j)-\overline{g}(i,j))^2\sum_{i=1}^{m}\sum_{j}^{n}(t(i,j)-\overline{t}(i,j))^2}}, \tag{2}$$

where the size of mark is $m \times n$,

$$\overline{t}(x,y) = \frac{\sum_{i=1}^{m}\sum_{j=1}^{n}t(i,j)}{mn},$$

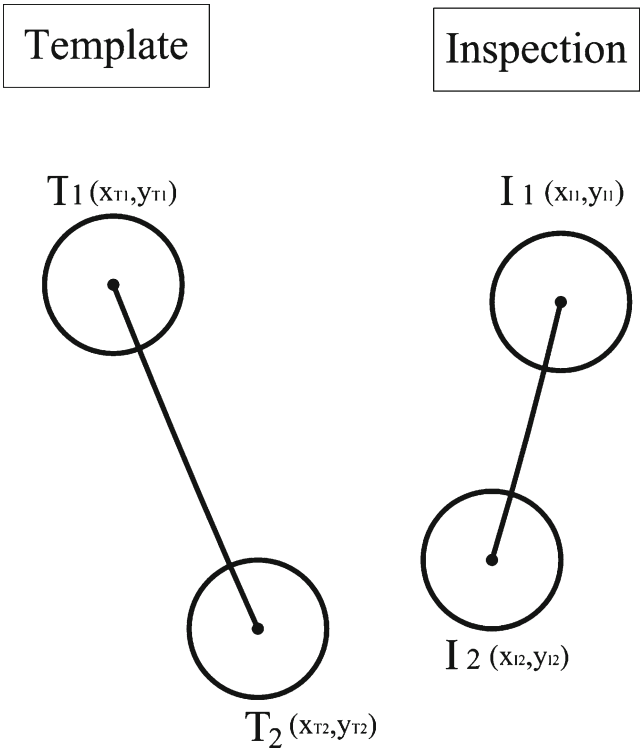



**Fig. 8** Two aligning marks in referential image and inspecting image, respectively

and

$$\overline{g}(x,y) = \frac{\sum_{i=1}^{m}\sum_{j=1}^{n} g(i,j)}{mn}.$$

The search of corresponding mark will be done in a restricted region in the inspecting stage. The corresponding mark will be in the location which has the maximum value of coefficient of correlation.

To find the angle of rotation, we can overlap points $T_2$ and $I_2$ as shown in Fig. 10. Suppose that $a$, $b$, and $c$ are the lengths of three segments $\overline{I_1I_2}$, $\overline{T_1T_2}$, and $\overline{T_1I_1}$, respectively. The angle θ can then be found by the following equation.

$$\cos\theta = \frac{a^2 + b^2 - c^2}{2ab}, \tag{3}$$

where

$$a = \sqrt{(x_{I_1} - x_{I_2})^2 + (y_{I_1} - y_{I_2})^2},$$
$$b = \sqrt{(x_{T_1} - x_{T_2})^2 + (y_{T_1} - y_{T_2})^2},$$
$$c = \sqrt{(x_{I_1} + x_{I_2} - x_{T_1} - x_{T_2})^2 + (y_{I_1} + y_{I_2} - y_{T_1} - y_{T_2})^2}.$$

Once the angle of rotation has been determined, we can calibrate them as in Fig. 10. The following equations are used to calibrate the coordinates of the inspecting image to the template image:

$$\begin{aligned} x' &= (x - x_0)\cos\theta + (y - y_0)\sin\theta, \\ y' &= -(x - x_0)\sin\theta + (y - y_0)\cos\theta, \end{aligned} \tag{4}$$

where $(x_0, y_0)$ is the coordinate difference of aligning marks $T_2$ and $I_2$,

$$\begin{aligned} x_0 &= x_{T_2} - x_{I_2}, \\ y_0 &= y_{T_2} - y_{I_2}, \end{aligned} \tag{5}$$

and $(x', y')$ is the transformed coordinate of $(x, y)$.

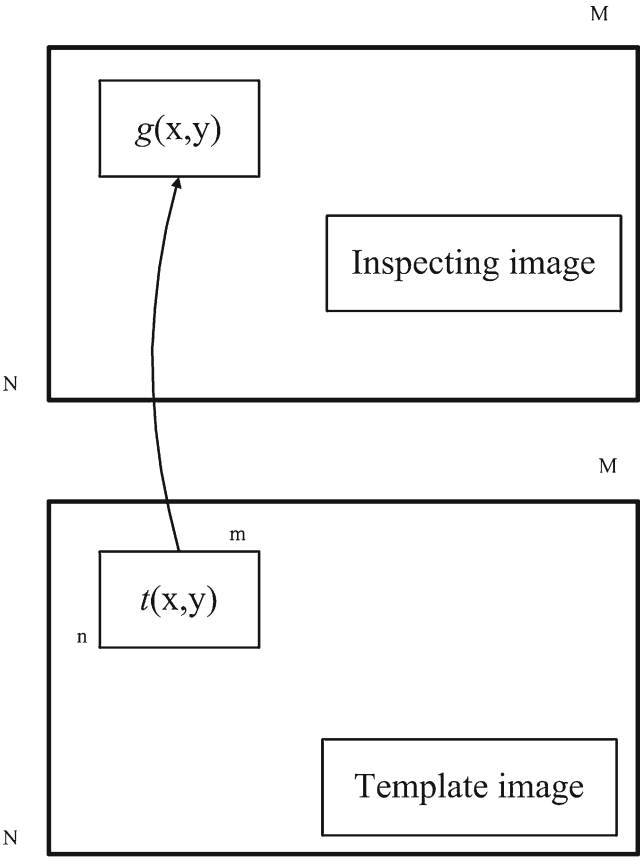



**Fig. 9** Coefficient of correlation between mark in template and inspecting image

### 2.3 Feature extraction

After performing image preprocessing, four features should be extracted from the image of IC boards to identify the defects of solder bumps. They are area of solder bump, the number of edge pixel, the deviation from center, and the deformation ratio:

1. Area of solder bump ($A_S$): The area of solder bump can be easily obtained by a method of object counting from the binary image. It can be done in the image labeling step. The number of pixels in an object is said to be the

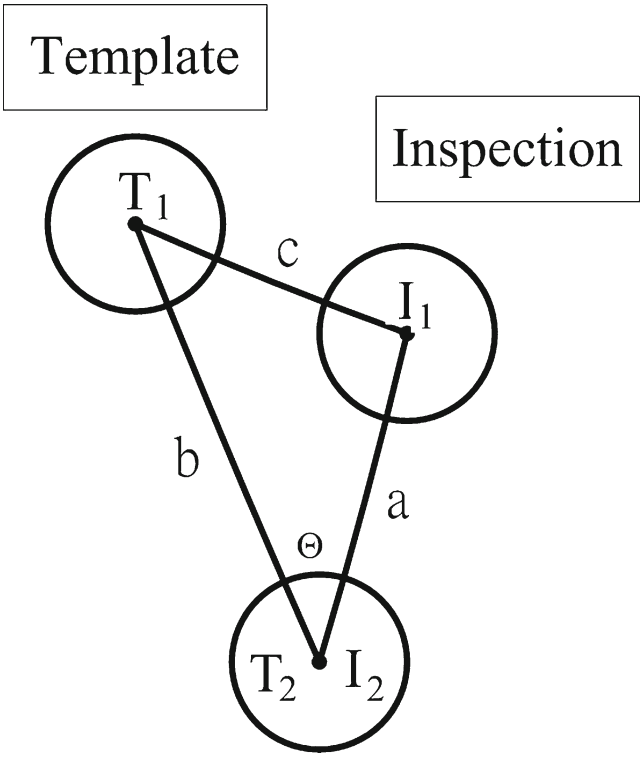



**Fig. 10** Overlapping marks in template and inspecting images to find the angle of rotation

area of solder bump. It is used to evaluate the quality of solder bumps. The area should be in an interval for a normal solder bump.

2. Number of edge pixels ($N_E$): The number of edge pixels on the solder bump can be extracted from the edge image. It is also used for evaluating the sizes of solder bumps. It can be done in the edge detection step using the template matching method.
3. Deviation from center ($D_C$): The deviation from center is used to identify the bridging defect. Since we have found the coordinates of the edge pixels of solder bumps in the edge detection process, the use of edge pixels to estimate the center of solder bumps is easy and fast. Suppose that $(x_i, y_i)$ is the $i$-th edge pixel of the solder bump, $N_E$ is the number of edge pixels, and $C(x_c, y_c)$ is the estimated center of the solder bump.

$$x_c = \frac{\sum_{i=1}^{N_E} x_i}{N_E}, \quad y_c = \frac{\sum_{i=1}^{N_E} y_i}{N_E}. \tag{6}$$

We can use the above equation to find the estimated center of each inspecting solder bump. Suppose that $(x_c^T, y_c^T)$ and $(x_c^I, y_c^I)$ are the centers of template and inspecting solder bumps. Then the deviation of center can be evaluated by the distance of the two centers.

$$D_C = \sqrt{\left(x_c^I - x_c^T\right)^2 + \left(y_c^I - y_c^T\right)^2}. \tag{7}$$

4. Deformation ratio ($R_D$): The deformation ratio is defined as the following formula (see Fig. 11).

$$R_D = \frac{d}{D}, \tag{8}$$

where $d$ and $D$ are the shortest and longest distances between the edge pixels and the estimated center, respectively.

Figure 12 shows an example of computing the above features. Figure 12a is a solder bump. It is seen that there are 58 pixels for the object after performed closing and opening operations; therefore, the area of solder bump will be 58 for the solder bump. Figure 12b shows the edge image of the solder bump in Fig. 12a. Since there are 26 edge pixels, so the number of edge pixels is 26 as shown in Fig. 12b. Suppose that the estimated centers of template and inspecting solder bump are (3.2, 3.9) and (3.3, 3.6), respectively (Fig. 12c). The deviation of center will be distance between these two centers and it is 0.32. In Fig. 12d, it is seen that the coordinates of the nearest and the farthest pixels from the center are (4, 1) and (8, 5), respectively. Therefore, we can find the shortest and longest distances. That is the $d$=2.7 and $D$=4.9, and the deformation ratio will be 0.55.

## 2.4 Defect detection and classification

The proposed solder bump inspection method is a hybrid approach. It includes two stages: the training stage and the inspection stage.

### *2.4.1 Training stage*

In the training stage, we use some templates to establish the information about aligning marks and solder bumps. Each

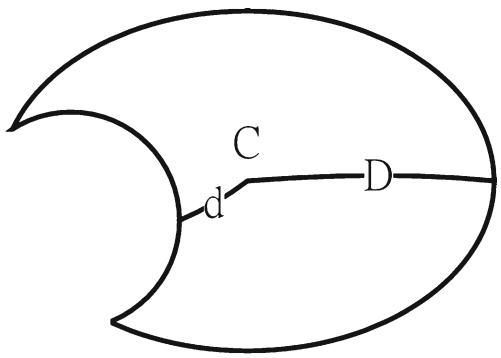



**Fig. 11** The deformation ratio: $D$ and $d$ are the longest and shortest distances between the edge pixels and the center

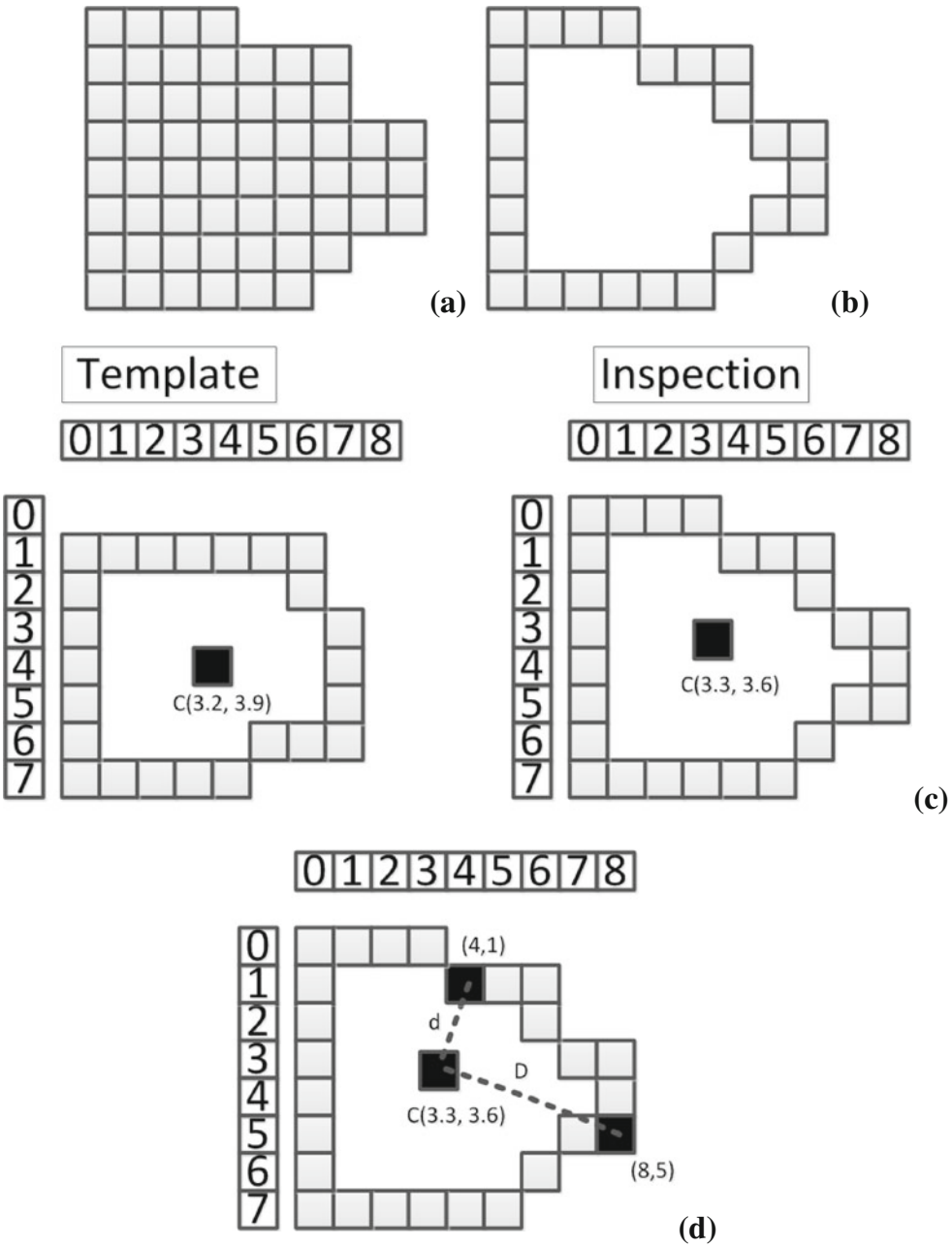



**Fig. 12** The features: **a** area, **b** number of edge pixels, **c** deviation of centers, and **d** deformation ratio

of the features is used to identify defects on the solder bumps. In order to check whether the inspecting IC boards are perfect or not, we should find the values of the features from templates before inspection stage.

The templates are chosen from several perfect IC boards. The means and the standard deviations of the four features can then be found. And the allowed intervals of features are determined using the statistical concept. Suppose that $\overline{f}$ and $s$ are the mean and standard deviation of the feature, and there are $N_t$ templates used to establish the decision criterion. The $1-\alpha$ confidence interval of the corresponding feature can be found with the following equation [37]:

$$\overline{f} \pm t_{\alpha/2} \frac{s}{\sqrt{N_t}}, \tag{9}$$

where

$$\overline{f} = \frac{\sum_{i=1}^{N_t} f_i}{N_t},$$

$$s = \left( \frac{\sum_{i=1}^{N_t} \left(f_i - \overline{f}\right)^2}{N_t - 1} \right)^{1/2}.$$

For a large number of templates, $t_{\alpha/2}$ is approaching to $z_{\alpha/2}$, and the above equation can be approximated by a standard Gaussian distribution as

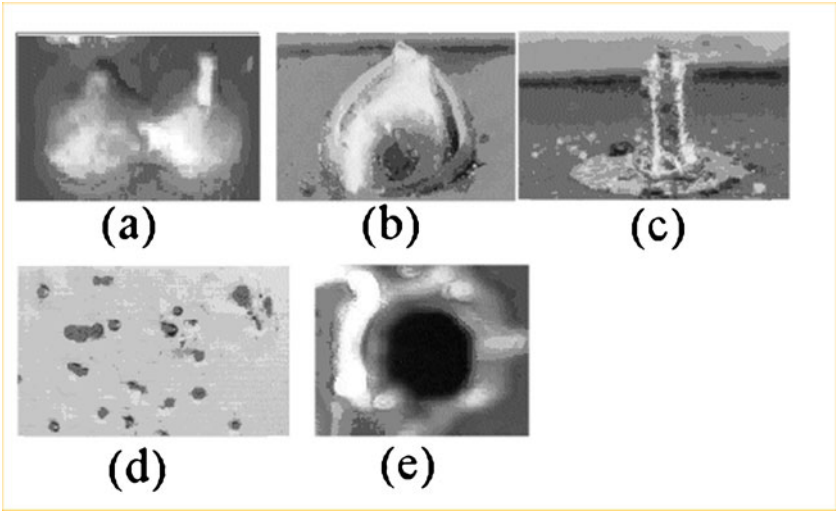



**Fig. 13** Five types of solder bump defects: **a** bridging, **b** excess solder, **c** incomplete solder, **d** non-wetting, and **e** missing solder

$$\overline{f} \pm z_{\alpha/2}\frac{s}{\sqrt{N_t}}. \tag{10}$$

Given a confidence level $1-\alpha$, we can obtain its $1-\alpha$ confidence intervals for each of features, and it will be used in the inspection stage to detect and classify the defects.

### *2.4.2 Inspection stage*

Five major types of defects commonly seen in the solder bumps are bridging, excess solder, incomplete solder, non-wetting, and missing bump as seen in Fig. 13. In the inspection stage, we should be able to determine if there exists a defect on a solder bump. In addition, it must classify the defect into one of the above five types of defects.

The characteristics of five types of the common solder bump defects are summarized as in Table 1. They are based on the extracted four features from the solder bumps. When a large value or a small value of feature has been detected, it may indicate a defect on solder bumps.

Given a confidence level $1-\alpha$, we can find the lower and upper allowances of the four features by Eq. (10). We can use the four sets of allowances to identify the defects. Suppose that the lower and upper allowances of four features are: area of solder bump ($A_{S\_L}$, $A_{S\_U}$), number of edge pixels ($N_{E\_L}$, $N_{E\_U}$), deviation from centers ($D_{C\_L}$, $D_{C\_U}$), and deformation ratio ($R_{D\_L}$, $R_{D\_U}$).

The position of each solder bump has been determined and so is the region of interest. Therefore, the processing and detection of solder bumps can then only apply to the region of interest in the inspection stage. After the solder bumps of inspecting IC board have been identified and the features can then be determined. Further, the features are used for detecting and classifying the defects while comparing them to the features of template.

First, the missing solder can be detected by checking whether there exists a bump in the region of interest. Next, the number of edge pixels, the area of solder bump, and the deviation from centers are compared with the preset values to find the bridging solder. Thirdly, the defects of excess solder and incomplete solder can be detected by the use of $A_S$, $N_E$, and $R_D$. Finally, the area of solder bump and number of edge number are used to classify the non-wetting defects.

From the characteristics of defect types listed in Table 1, the defect detection and classification rule is illustrated in Fig. 14. A solder bump passes all of the above defect detection processes will be denoted as a perfect bump. If all of the solder bumps in an IC board are perfect, the inspecting IC board will said to be perfect. Otherwise, it is said that there exists defects and the positions and the types of defects will be recorded.

**Table 1** The characteristics of the five types of solder bump defects

| Defect type | Characteristics |
|---|---|
| Missing solder | Cannot find center of solder bump |
| | Cannot find area of solder bump |
| | Cannot find number of edges |
| | Cannot find deformation ratio |
| Bridging | Excessive area of solder bump |
| | Excessive number of edge pixel |
| | Shifted center of solder bump |
| Excess solder | Excessive area of solder bump |
| | Excessive number of edge pixel |
| | Large deformation ratio |
| Incomplete solder | Insufficient area of solder bump |
| | Insufficient number of edge pixels |
| | Large deformation ratio |
| Non-wetting | Insufficient area of solder bump |
| | Insufficient number of edge pixels |

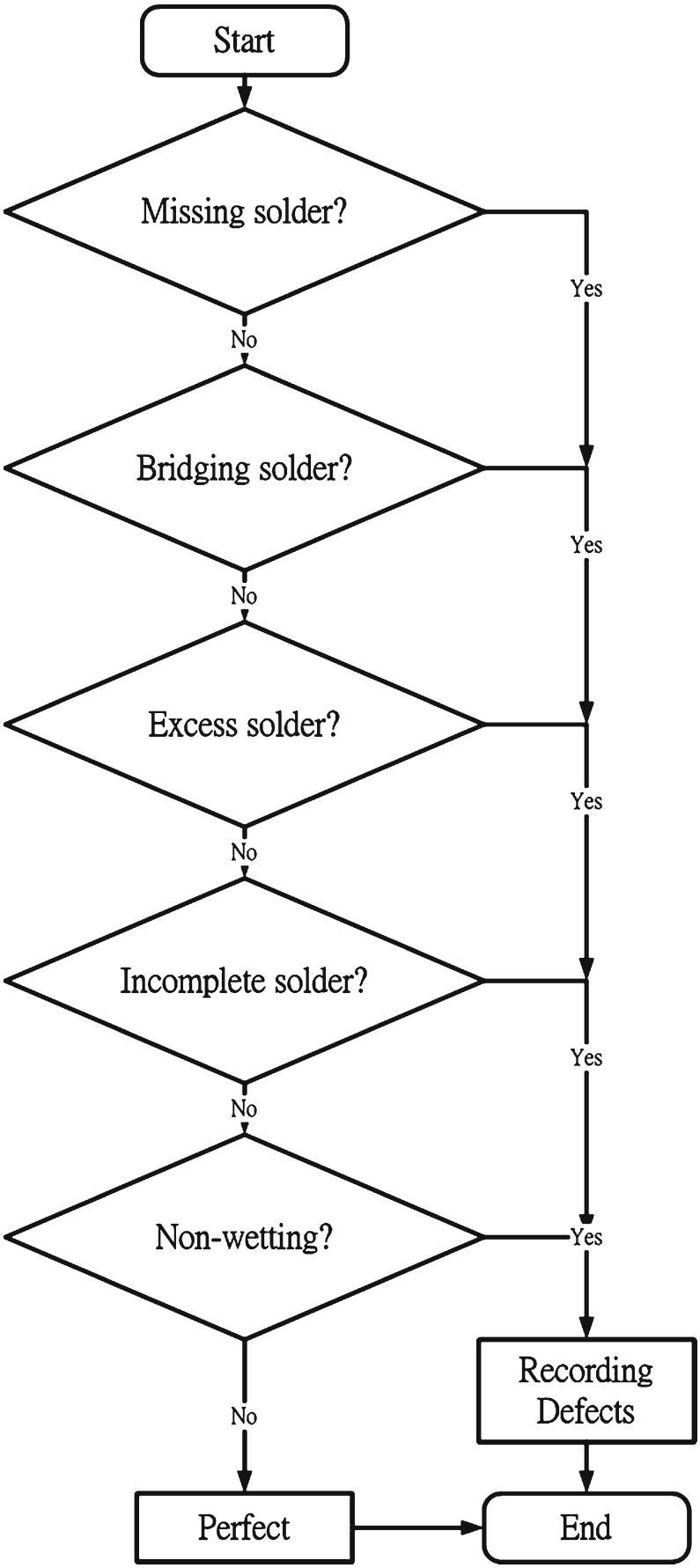



**Fig. 14** Rules for detecting and classifying defects of solder bumps

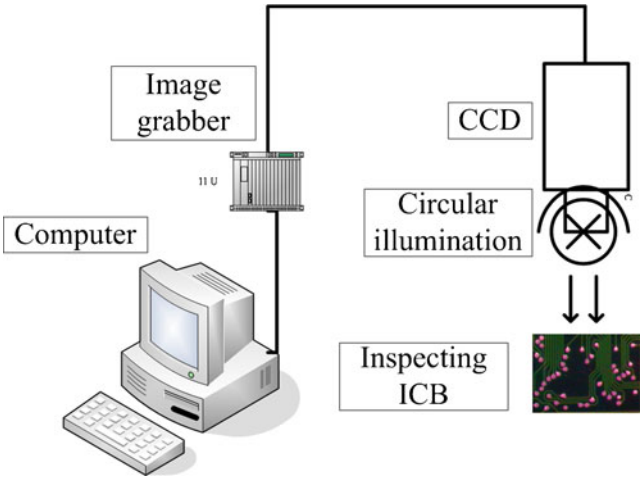



**Fig. 15** System diagram for automated solder bump inspection

## 3 Experimental results

In order to evaluate the proposed method for detecting defects of solder bumps, an experiment has been conducted. Figure 15 shows the system diagram of the automated solder bump inspection system. The system consists of personal computer, image grabber (Matrox Meteor), CCD camera (Mintron OS-50D), and circular illumination. The programming language is Borland C++ with Matrox MIL library. The distance between the CCD camera and the testing ICB is fixed to be 16.5 cm.

All of the grabbed color images are converted into gray images in this experiment. A 3×3 median filter is applied to the gray images to reduce the noise. In the training stage, we used 64 perfect IC boards as the templates to establish the features of the solder bumps. There are 106 solder bumps to be inspected in each of the IC boards. As described before, threshold value may affect the quality of solder bumps in binary images. Since we need only the solder bumps to be analyzed, various values have been tested to find the best threshold in the training stage. The threshold value is set to 110 to convert the gray level images into binary images.

**Table 2** An example of the means, standard deviations, lower bounds, and upper bounds of the four features for a solder bump using 64 templates with significance level $1-\alpha=99$ %

| | Mean | Standard deviation | Lower bound | Upper bound |
|---|---|---|---|---|
| Area of solder bump (unit: pixel$^2$) | 65.27 | 5.71 | 63.43 | 67.10 |
| Number of edge pixels (unit: pixel) | 33.95 | 7.60 | 31.51 | 36.40 |
| Deviation from centers (unit: pixel) | 1.80 | 0.96 | 0.00 | 2.11 |
| Deformation ratio | 0.78 | 0.20 | 0.72 | 1.00 |

**Table 3** Experimental results of solder bump inspection

| Defect type | Number of samples | Number of incorrect judge | Correct rate (%) |
|---|---|---|---|
| Normal | 6,600 | 173 | 97.39 |
| Missing solder | 800 | 0 | 100.00 |
| Bridging | 800 | 0 | 100.00 |
| Excess solder | 800 | 9 | 98.88 |
| Incomplete solder | 800 | 11 | 98.63 |
| Non-wetting | 800 | 23 | 97.13 |

Further, to remove the uneven binarization problem, a 3× 3 structuring mask is used in the image opening and closing morphological operation. After applying the above image processing operations to the images, the solder bumps are then detected by conducting an image labeling operation.

For each template, we should find the area of solder bump, number of edge pixels, estimated center of solder bump, and deformation ratio for each solder bump. The deviation from center is found by two consecutive templates. The means and the standard deviations of the four features were then computed. They are used to determine the defects of solder bumps in the inspection stage.

The significance level is set to 99 % in the experiment. The upper bound and lower bound of the four features will then be determined for each of the 106 solder bumps. Since there are 106 solder bumps in an IC board, we should have 106 sets of these bounds. Since the computations of these features are based on coordinates of image, the units according to deviations from center and numbers of edge pixels are pixel, and area of solder bumps will be square pixel. The number of templates is 64 in computing these allowances. Table 2 shows an example of the means, standard deviations, lower bounds, and upper bound bounds of the four features. It is seen that the lower bound of deviation from centers is 0, since it will always be greater than 0. Further, the deformation ratio is always less than or equal to 1.0; therefore, its upper bound is 1.0. The upper bounds and lower bounds were used in detecting and classifying the defects of solder bumps.

**Table 4** The correct flaw classification rates of the proposed method and some previous methods

| Method | Number of samples | Correct flaw classification rate (%) |
|---|---|---|
| Our method | 10,600 | 97.96 |
| Chiu and Perng [25] | 806 | 95.00 |
| Jiang et al. [26] | 87 | 97.30 |
| Kim et al. [27] | 203 | 99.50 |
| Loh and Lu [28] | 80 | 92.31 |
| Mar et al. [29] | 1,000 | 95.00 |

In the inspection stage, 100 IC boards were used to evaluate the proposed method. There are 10,600 (=106×100) solder bumps to be inspected in this experiment. They consist of 6,600 normal and 4,000 defective solder bumps. Each type of defects has 800 solder bumps. The purpose of inspection is to detect and classify defects existing in the IC board.

The same image processing procedures are applied to the inspected IC boards. After performed a calibration operation, the information of locations of solder bumps are used to extract the solder bumps quickly. The mean of solder bump centers of the templates is considered as the estimated center of solder bump. The four features of each solder bump in the inspected IC board can then be found. By using the defect detection and classification rule as in Fig. 14, we can determine the solder bumps to be normal or defective. The frequencies and types of defects can be recorded at the same time.

Table 3 shows the solder bump defect detection and classification results. It is seen that the defect types of bridging and missing solder can be detected correctly. For the defects of excess solder and incomplete solder, there are nine and 11 incorrect judges, respectively. They are classified as perfect solder bumps. There are 23 defects of non-wetting that are not correctly classified. They can be detected as defects, but they are classified as the missing solder problem. The incorrect flaw classification rate is about 2.87 %. Since there are 20 defects that are not detected for the 4,000 defects, so the faults missed rate is about 0.50 %. Further, about 173 normal solder bumps are considered as defective solder bumps. The false alarm rate is about 2.61 %. They are classified as excess solders or incomplete solders. This is due to their areas of solders or the numbers of edge pixels are larger than the upper bound or are less than the lower bound. The false alarm rate can be reduced if a narrow width of allowances is used. But the faults missed rate may increase in the same time. Overall, there are 216 incorrect judges, and the correct flaw classification rate is about 97.96 %.

Table 4 presents the correct flaw classification rates of the proposed method and some previous methods. It is seen that all of the previous methods as well as the proposed method have the high correct flaw classification rates. However, the proposed method has the largest number of samples. Further, the proposed method has low false alarm (2.61 %), faults missed (0.50 %), and incorrect flaw classification rates (2.87 %) and has a high correct flaw classification rate (97.96 %). It can illustrate the good performance of the proposed method.

## 4 Conclusions

In this paper, we propose a hybrid method for the automated visual inspection of solder bumps on the IC boards. Two stages for inspecting the solder bump defects are the training stage and the inspection stage. In the training stage, several template images are used to define the positions and features of solder bumps. In the inspection stage, four features of solder bumps are used in the defect detection and classification. They are area of solder bump, the number of edge pixels, the deviation from center, and the deformation ratio. A defect detection and classification rule is applied to determine whether there exist solder bump defects on the IC boards. Five types of defects are bridging, excess solder, incomplete fillet, non-wetting, and the missing bump. From the experimental result, it is seen that the correct flaw classification rate is about 97.96 %. This high correct rate indicates that the proposed method is able to effectively detect and classify the defects.

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