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CCII- and OTA-Based Tunable Memcapacitor Emulator Circuits Without Using Passive Elements

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Abstract

In this paper, two floating memcapacitor emulator circuits, one based on a second-generation current conveyor (CCII) and the other on an operational transconductance amplifier (OTA), are proposed. The first floating memcapacitor contains a single CCII, one multiplier, and four transistors, while the second one comprises a single OTA, one multiplier, and only two transistors. External transistors are operated as electronically controllable grounded capacitors and resistors. Therefore, the inverse memcapacitances of the circuits are adjusted electronically by applying appropriate bias voltages. Both emulator circuits can be operated to have incremental or decremental characteristics. The analyses of frequency response, electronic adjustability, temperature behavior, and non-volatile behavior of the circuits, as well as Monte Carlo analysis, are performed. Furthermore, an adaptive learning circuit is utilized to demonstrate the applicability of the proposed memcapacitor. Additionally, the CCII-based emulator circuit is constructed on a printed circuit board using discrete circuit elements and tested experimentally. The non-volatility feature of the circuit was tested for both incremental and decremental memcapacitors. The simulation and experimental results agree with the expected results.

Keywords Memcapacitor · CCII · OTA · Floating · Incremental · Decremental · Electronic tunability

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1 Introduction

The relationship between charge (q) and flux (φ) of a memristor, a fourth fundamental circuit element, was defined by Chua [16]. However, the memristor did not attract researchers' attention until 2008, when the HP research team announced the fabrication of a natural TiO_2 memristor [47]. The realization of memristors marked the starting point for memristor-based studies. These studies can be categorized into three types: I. memristor emulator circuit design [3, 4, 6, 7, 14, 24, 29, 31, 33, 40, 41, 62], II. memristor-based circuit design [1, 5, 59, 63, 64, 67], and III. fabrication of the memristors [6, 18, 28, 42, 47]. However, apart from these studies, researchers are also interested in higher-order memelements such as meminductors [22, 27, 34, 44, 46, 58] and memcapacitors [8–10, 12, 13, 19–21, 23, 25, 26, 30, 35–38, 43, 45, 48, 50, 51, 53, 54, 56, 57, 61, 65, 66, 68]. Both the memcapacitor and meminductor elements exhibit nonlinear pinched hysteresis characteristics in their relationships between charge and voltage and flux and current, respectively.

Memcapacitor emulator design is a new research area because it is difficult to obtain memcapacitors on the market as a discrete circuit element. Research into the advantages of memcapacitor-based circuits is vital for circuit designers. Effectiveness, high accuracy, low energy consumption, electronic controllability, simple structure, and compatibility with VLSI designs are important parameters for designing memcapacitor emulator circuits. Active-circuit elements can fulfill these requirements and are suitable for designing memcapacitor emulators. Therefore, different types of active-circuit-element-based memcapacitor emulators have been reported in the literature [8–10, 12, 13, 19–21, 23, 25, 26, 30, 35–38, 43, 45, 48, 50, 51, 53, 54, 56, 57, 61, 65, 66, 68]. Konal et al. [25] designed a voltage differencing current conveyor (VDCC)-based memcapacitor emulator circuit with electronically controllable properties. The circuit operates in low-frequency ranges and is realized using discrete circuit elements. However, the application of the emulator is limited because the circuit has a grounded structure. Vista and Ranjan [50] designed a memcapacitor emulator based on a differential voltage current conveyor transconductance amplifier (DVCCTA). The circuit has a simple structure but is grounded. Yesil and Babacan [61] presented a second-generation current conveyor (CCII)- and operational transconductance amplifier (OTA)-based memcapacitor emulator circuit. The circuit is electronically controllable, implemented using discrete circuit elements, and demonstrates a strong memory effect and a charge–voltage relationship with pinched hysteresis. However, because the proposed structures are grounded, their applications are limited. The aforementioned CCII-based memcapacitor emulator circuit was implemented using two AD844s and one AD633. Hosbas et al. [21] designed a voltage differencing transconductance amplifier (VDTA)-based memcapacitor using a VDTA-based memristor emulator. The memcapacitor circuit is electronically controllable and exhibits a strongly pinched hysteresis loop. However, it has a grounded structure. Fouda and Radwan [19] proposed a grounded memristor-less memcapacitor emulator circuit that used four OPAMPs, a multiplier, and a single current-controlled current source. They provided the PSpice results for the circuit but noted that it has not yet been experimentally tested. Romero et al. [37] designed a memcapacitor emulator circuit based on the Miller effect. The designed circuit was tested in both a simulation program and

a field-programmable analog array (FPAA) and comprised an OPAMP, buffer, capacitor, and memristor owing to its mutator structure. A memcapacitor emulator circuit using one VDTA element and two grounded capacitors was designed by Petrović [35]. The circuit was experimentally tested in a simulated environment using off-the-shelf components. Owing to the VDTA element, the circuit is electronically adjustable but grounded. Vista and Ranjan [51] proposed a circuit that can emulate the behavior of a floating memcapacitor. The circuit is electronically adjustable both incrementally and decrementally. Although the circuit was implemented using an adaptive learning circuit, experimental results were not provided. Singh and Rai presented a VDCC-based floating structure memcapacitor emulator circuit [45]. The circuit contains only one VDCC, one capacitor, and one memristor owing to its mutator structure. However, only the simulation results of the circuit are available. Sah et al. [38] designed a floating memcapacitor emulator using off-shelf devices. Two OPAMPs and a multiplier circuit were used. The experimental results were obtained by building a circuit on a breadboard; however, the circuit did not have an electronically adjustable structure. Wang et al. proposed a memcapacitor emulator circuit using a mutator structure [54]. The circuit was designed using five OPAMPs, an LDR, LED, a diode, 12 resistors, and two capacitors. A large number of active and passive elements were used in the circuit, and the circuit was not electronically adjustable. Sharma et al. [43] proposed an emulator circuit that can function as both a memristor and memcapacitor using two CCIIs and a multiplier circuit. The study presents the experimental results, and the circuit can be operated as both grounded and floating circuits. Although this circuit can operate both incrementally and decrementally, it does not exhibit electronically adjustable properties. Bhardwaj et al. [9] presented a universal memelements emulator with one each of a CCII, OTA, a resistor, and two capacitances. Although the simple and universal structure of the circuit is a crucial advantage, experimental studies on this circuit have not yet been conducted. Bhardwaj and Srivastava [10] designed a grounded multiplier-less charge-controlled memelements emulator consisting of one VDCC, one OTA, two capacitors, and a resistor. Although the circuit is electronically adjustable, the fixed and variable components cannot be adjusted independently.

A floating emulator circuit [66] was designed to obtain a memristor, memcapacitor, and meminductor. The circuit for the memcapacitor consists of four AD844s, one OPAMP, one varactor diode, six resistors, and two capacitors. Zheng et al. [68] presented a universal interface that could be used as a memristor, memcapacitor, or meminductor. In the universal structure, four AD844s, a varactor diode, two capacitors, and two resistors are employed to form a memcapacitor emulator circuit. As a universal structure was presented in these studies [66, 68], a large number of elements were used in the circuits. Wang et al. designed a floating memcapacitor emulator circuit [53] using a real memristor. The circuit contained three AD844s, three passive elements, and a memristor produced by Knowm. Simulations and experiments were conducted using the designed circuit. Yu et al. designed a floating memcapacitor emulator circuit with a mutator structure [63]. The circuit consisted of four AD844s, two OPAMPs, a multiplier circuit, and 10 passive elements. Although the simulation and experimental results of the circuit have been presented, the number of elements used in the circuit is high, and the circuit has no electronic tunability. In the floating memcapacitor emulator designed by Biolek et al. [12], one AD8421, two LM311s,

one MAX4523, one Op27, four capacitors, five resistors, and one potentiometer were used. Both simulation and experimental studies have been conducted on circuits that require numerous components. Gur et al. [20] designed a simple MO-OTA-based memcapacitor emulator circuit. Although the circuit is fully floating and electronically controllable, the number of elements is large because it contains two MO-OTAs, four transistors, a capacitor, and a resistor. Additionally, only the simulation results were included in this study, and no experimental studies were conducted. In a study by Tatović and Petrović [48], a floating memcapacitor emulator circuit was proposed using one VDCC, two MOSFETs, and two capacitors. The proposed circuit was electronically tunable; however, it was only tested in a simulation environment. However, no experimental studies have been conducted on these circuits.

In summary, the circuits designed in many studies [8–10, 19, 21, 25, 26, 35–37, 50, 54, 61] are grounded; therefore, their application areas are relatively limited compared to those for floating structures. However, some studies on floating memcapacitor emulators [12, 13, 20, 23, 38, 45, 48, 51, 53, 56, 57, 65, 66, 68] have not provided experimental results [13, 20, 23, 45, 48, 51], whereas in other studies, the circuits lack electronic adjustability features [12, 38, 53, 65, 66, 68]. Memcapacitor emulators, both grounded and floating, have also been designed [30, 43]; however, their active and passive element counts are high.

In this study, two floating memcapacitor emulator circuits, one CCII-based and the other OTA-based, are proposed. The CCII-based memcapacitor circuit comprises only one CCII, a single analog multiplier, and four MOSFETs. The OTA-based memcapacitor circuit contains a single OTA, single analog multiplier, and two MOSFETs. Using MOSFETs and the transconductance gain of the OTA, the memcapacitance of the proposed circuits can be electronically adjusted both incrementally and decrementally. Both the proposed circuits were simulated using the LTspice program. Furthermore, an adaptive learning circuit was implemented to demonstrate the applicability of the proposed memcapacitor. A CCII-based emulator circuit was developed on a PCB using an AD844 multiplier, resistor, and two capacitors and tested. The results obtained from the experimental and simulation studies are compatible with each other and with the mathematical equations.

2 Proposed CCII-Based Memcapacitor Emulator Circuit

Memcapacitors are defined using the relationship between the charge integral (σ) and flux (φ). This relationship is expressed in Eq. (1).

$$C_{\mathrm{M}}(\varphi) = \frac{\mathrm{d}\sigma}{\mathrm{d}\varphi} \tag{1}$$

The voltage-controlled and charge-controlled memcapacitor elements are defined in Eqs. (2) and (3) [49]. The emulator circuits proposed in this study are controlled by charge.

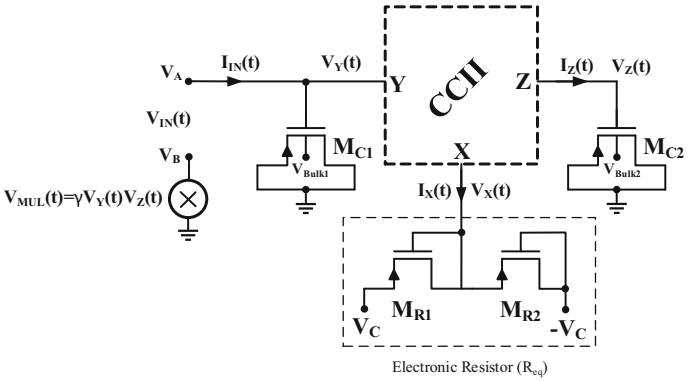


Fig. 1 CCII-based floating memcapacitor

$$q(t) = C_{\mathrm{M}}\left[\int_{t_0}^{t} V_{\mathrm{C}}(\tau)\mathrm{d}\tau\right]V_{\mathrm{C}}(t) \tag{2}$$

$$V_{\mathrm{C}}(t) = C_{\mathrm{M}}^{-1}\left[\int_{t_0}^{t} q(\tau)\mathrm{d}\tau\right]q(t) \tag{3}$$

The CCII-based memcapacitor emulator circuit contains one CCII, one multiplier, and four MOSFETs, as shown in Fig. 1. The transistors have the capability to function as capacitors [2, 15, 17]. In this circuit, the M_{C1} and M_{C2} MOSFETs are used as grounded and electronically adjustable capacitors. The M_{R1} and M_{R2} transistors are used as grounded and electronically adjustable resistors that formed the equivalent resistance R_{eq} [55], defined in Eq. (4).

$$R_{\mathrm{eq}} = \frac{1}{2\mu_{\mathrm{p}}C_{\mathrm{OX}}(V_{\mathrm{C}} - V_{\mathrm{TH}})\left(W/L\right)_{\mathrm{M_{R1},M_{R2}}}} \tag{4}$$

The current–voltage relationships between the terminals of the CCII element are shown in Eq. (5). In the equation, α and β represent the current and voltage gains of a CCII element, respectively. In an ideal CCII element, the values of α and β are equal to one and are independent of frequency.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \beta & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \tag{5}$$

As shown in Fig. 1, an input voltage is applied to terminals A and B of the proposed circuit. The input current that flows through terminal$A$ is related to the charge on capacitor C_1, as expressed in Eq. (6). This is because the current flows completely

through capacitor C_1, and no current flows from terminal Y. The voltage at terminal X is β times the voltage at terminal Y, as shown in Eq. (5). The current flowing through terminal X is expressed as $I_X(t) = V_x(t) / R_{\text{eq}}$. Since the current flowing through terminal X is α times the current flowing from terminal Z, Eqs. (7) and (8) are obtained.

$$V_{\text{A}}(t) = V_{\text{Y}}(t) = \frac{1}{C_1}\int I_{\text{IN}}(t)\text{d}t = \frac{q(t)}{C_1} \tag{6}$$

$$I_{\text{Z}}(t) = \alpha I_{\text{X}}(t) = \frac{\alpha V_{\text{X}}(t)}{R_{\text{eq}}} = \frac{\alpha\beta V_{\text{Y}}(t)}{R_{\text{eq}}} = \frac{\alpha\beta q(t)}{C_1 R_{\text{eq}}} \tag{7}$$

$$V_{\text{Z}}(t) = \frac{1}{C_2}\int I_{\text{Z}}(t)\text{d}t = \frac{\alpha\beta}{C_1 C_2 R_{\text{eq}}}\int q(t)\text{d}t \tag{8}$$

If the equation for the voltage at the output terminal of the multiplier is positive, the expression for $V_{\text{MUL}}(t)$ is as shown in Eq. (9). A floating structure is obtained when the output terminal of the multiplier is connected to terminal B of the input voltage. The relationship between the input voltages at terminals A and B is given by Eqs. (9) and (10): The expression γ refers to the constant coefficient of the multiplier element.

$$V_{\text{B}}(t) = V_{\text{MUL}}(t) = \gamma V_{\text{Y}}(t) V_{\text{Z}}(t) = \frac{\gamma\alpha\beta q(t)}{C_1^2 C_2 R_{\text{eq}}}\int q(t)\text{d}t \tag{9}$$

$$V_{\text{IN}}(t) = V_{\text{A}}(t) - V_{\text{B}}(t) = \frac{q(t)}{C_1} - \frac{\gamma\alpha\beta q(t)}{C_1^2 C_2 R_{\text{eq}}}\int q(t)\text{d}t \tag{10}$$

When the expression in Eq. (10) is rearranged, the inverse memcapacitance in the incremental structure is derived, as shown in Eq. (11). However, when the output of the multiplier is negative, Eq. (12) yields an inverse memcapacitance in the decremental structure.

$$C_{\text{M}}^{-1}(t) = D_{\text{M}}(t) = \frac{V_{\text{IN}}(t)}{q(t)} = \underbrace{\frac{1}{C_1}}_{\text{Fix part}} - \underbrace{\frac{\gamma\alpha\beta}{C_1^2 C_2 R_{\text{eq}}}\int q(t)\text{d}t}_{\text{Variable part}} \tag{11}$$

$$C_{\text{M}}^{-1}(t) = D_{\text{M}}(t) = \frac{V_{\text{IN}}(t)}{q(t)} = \underbrace{\frac{1}{C_1}}_{\text{Fix part}} + \underbrace{\frac{\gamma\alpha\beta}{C_1^2 C_2 R_{\text{eq}}}\int q(t)\text{d}t}_{\text{Variable part}} \tag{12}$$

The main reason for using MOSFETs instead of resistors and capacitors in the circuit design is that their resistance and capacitance cannot be altered electronically. By contrast, MOSFET-based designs offer the opportunity to adjust these values electronically. As indicated by Eqs. (10) and (11), the fixed and variable parts of the inverse memcapacitor equations can be modified separately. Since the values of the passive elements can be changed electronically, the fixed part with C_1 and the variable part with R_{eq} and C_2 can be adjusted independently. Capacitances C_1 and C_2 can be changed by adjusting the bulk voltages of transistors M_{C1} and M_{C2}, which function as MOS

capacitors [2, 15, 17]. Similarly, voltage V_C can be adjusted to alter the equivalent electronic resistance R_{eq} of transistors M_{R1} and M_{R2} [55].

An additional benefit of designing a circuit using MOSFETs rather than directly using passive elements is the ability to build the circuit directly within the integrated circuit, as the proposed circuit has no external components such as resistors and capacitors.

3 Proposed OTA-Based Memcapacitor Emulator Circuit

The proposed OTA-based floating memcapacitor emulator circuit is shown in Fig. 2. The circuit consists of one OTA, one multiplier, and two MOSFETs. As mentioned in the previous section, MOSFETs M_{C1} and M_{C2} function as the grounded MOS capacitors C_1 and C_2, respectively.

The terminal relationships of OTA can be represented as $I_z(t) = g_m(V_P(t) - V_N(t))$ and $I_P(t) = I_N(t) = 0$. The g_m value of the OTA element is denoted as $g_m = K(V_{REF} - V_{SS} - V_{TH})$, and the expression for K in this equation is represented as $K = B\mu_n C_{ox}\sqrt{{}^1/_2\left({}^W/_L\right)_{M_1}\left({}^W/_L\right)_{M_9}}$ [60]. The parameters μ_n, C_{ox}, and V_{TH} represent carrier mobility, gate oxide capacitance per unit area, and threshold voltage, respectively. B is defined as the gain of the current mirror between transistors $M_{5,3}$ and $M_{6,4}$, and according to this OTA structure, the value of B is 2. As shown in Fig. 2, an input voltage is applied between terminals A and B in the emulator circuit. As no current flows from terminal N, the input current flows through capacitor C_1, yielding the charge expression in Eq. (13). The current flowing from terminal Z can be described as $I_z(t) = -g_m V_N(t)$ because terminal P is connected to ground. Current $I_z(t)$ flowing through capacitor C_2 is given by Eq. (14).

$$V_A(t) = V_N(t) = \frac{1}{C_1}\int I_{IN}(t)\mathrm{d}t = \frac{q(t)}{C_1} \tag{13}$$

$$V_Z(t) = \frac{1}{C_2}\int I_Z(t)\mathrm{d}t = -\frac{1}{C_2}\int g_m V_N(t) = -\frac{g_m}{C_1 C_2}\int q(t)\mathrm{d}t \tag{14}$$

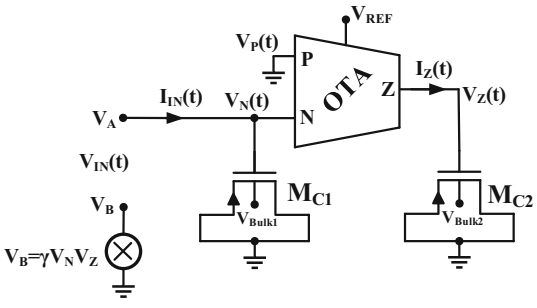


Fig. 2 Proposed OTA-based floating memcapacitor

When the multiplier circuit is used as a positive multiplier, voltage $V_B(t)$ is obtained, as shown in Eq. (15). Equation (16) is obtained when an input voltage is applied between terminals A and B. In the equations, γ represents the constant coefficient of the multiplier element.

$$V_B(t) = \gamma V_N(t) V_Z(t) = -\frac{\gamma g_m q(t)}{C_1^2 C_2} \int q(t)\mathrm{d}t \tag{15}$$

$$V_{IN}(t) = V_A(t) - V_B(t) = \frac{q(t)}{C_1} + \frac{\gamma g_m q(t)}{C_1^2 C_2} \int q(t)\mathrm{d}t \tag{16}$$

When Eq. (16) is rearranged, the inverse memcapacitance expression of the decremental structure is obtained as shown in Eq. (17). If the input voltage is applied to the P terminal instead of the N terminal of the OTA element or the output of the multiplier is set to be negative, the inverse memcapacitance is obtained incrementally, as in Eq. (18).

$$C_M^{-1}(t) = D_M(t) = \frac{V_{IN}(t)}{q(t)} = \underbrace{\frac{1}{C_1}}_{\text{Fix part}} + \underbrace{\frac{\gamma g_m}{C_1^2 C_2} \int q(t)\mathrm{d}t}_{\text{Variable part}} \tag{17}$$

$$C_M^{-1}(t) = D_M(t) = \frac{V_{IN}(t)}{q(t)} = \underbrace{\frac{1}{C_1}}_{\text{Fix part}} - \underbrace{\frac{\gamma g_m}{C_1^2 C_2} \int q(t)\mathrm{d}t}_{\text{Variable part}} \tag{18}$$

In the proposed emulator circuit, capacitors C_1 and C_2 are formed by MOSFETs M_{C1} and M_{C2}. This design allows the capacitance values to be adjusted by changing the bulk voltage of the MOSFETs. The value of g_m can be adjusted by changing the bias voltage V_{REF} of the OTA element in the circuit. These properties provide the circuit with an electronically adjustable structure.

4 Simulation Results

Two proposed floating memcapacitor circuits are simulated using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm process model parameters in the LTspice program. In simulation studies, the circuit's responses at various frequencies, electronic tunability, behavior at different temperatures, and memory effects were examined, and Monte Carlo analysis was also performed.

4.1 Simulation Results for the CCII-Based Floating Memcapacitor Emulator Circuit

The internal structure of the CCII element used in the CCII-based memcapacitor emulator circuit is illustrated in Fig. 3. The CCII element is designed using the LTspice program and TSMC 0.18-μm process model parameters. The dimensions of the MOSFET elements in the CCII are listed in Table 1. The supply voltages of the CCII element

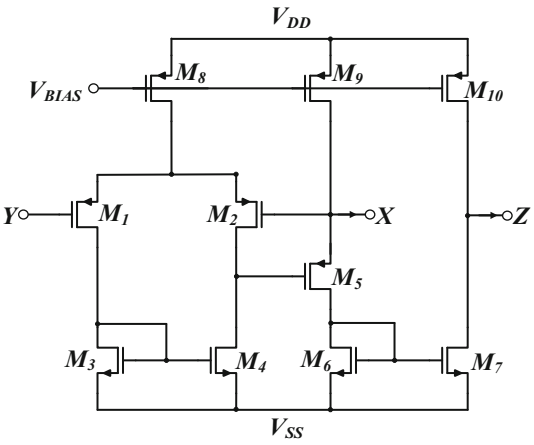


Fig. 3 Internal structure of the CCII element

Table 1 Dimensions of MOSFET elements in the CCII element

MOSFETs	W (μm)	L (μm)
M_1, M_2, M_5	30	0.18
M_3, M_4, M_6, M_7	10	0.54
M_8, M_9, M_{10}	30	0.54

are set to $V_{DD} = -V_{SS} = 0.9$ V, and its bias voltage is fixed at 350 mV. In the CCII element, the bulk terminals of the p-type MOSFETs are connected to the source, whereas the bulk terminals of the n-type MOSFETs are connected to a minimum voltage of − 0.9 V. The dimensions of the MOS capacitor elements in the circuit are chosen using $W/L = 100\mu m/4\mu m$, and those of the transistors in the electronic resistor structure are selected as $W/L = 60\mu m/2\mu m$.

In all the simulation studies conducted on the CCII-based circuit, unless specified otherwise, the input signal is selected as a sinusoidal wave at 5 MHz and 60 mV. Since the voltage of the electronic resistor V_C is set to 460 mV, the equivalent resistance in the circuit is maintained at 6 kΩ. The bulk voltages of the capacitors in the circuit are fixed at 0 V, and their capacitance values vary between 1 and 1.3 pF.

The CCII-based emulator circuit can operate incrementally and decrementally, as described in Eqs. (11) and (12), respectively. These operational modes are determined by setting the multiplier element to either a positive or a negative output. When the multiplier is set to positive, the emulator circuit operates in the incremental mode, as shown in Fig. 4a. Conversely, when the multiplier element is set to negative, the emulator circuit operates in decremental mode, as shown in Fig. 4b. In all simulation studies conducted on CCII-based circuits, with the exception of the non-volatility behavior test, the multiplier element is chosen as positive, and the simulation outcomes are achieved using the incremental structure.

The hysteresis loops depicted in Fig. 5 are obtained by varying the input voltage frequency between 4, 5, and 30 MHz. As the operating frequency increases, the hysteresis

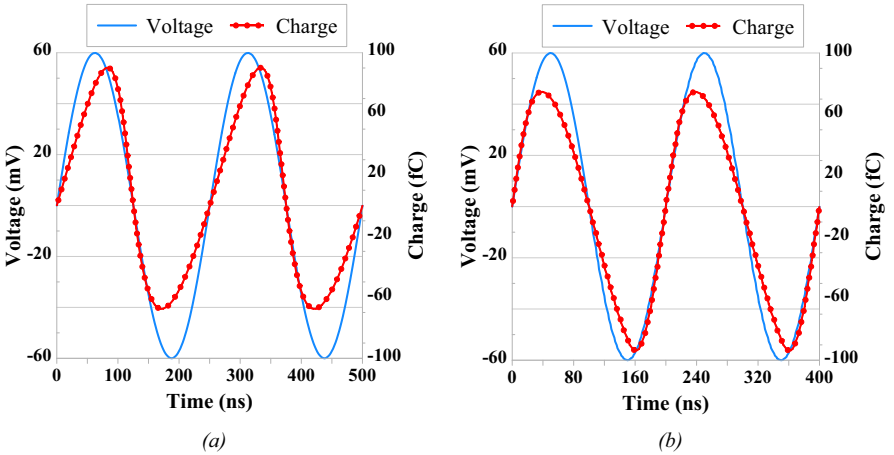


Fig. 4 Charge–voltage graph of the CCII-based circuit showing **a** the incremental structure and **b** the decremental structure

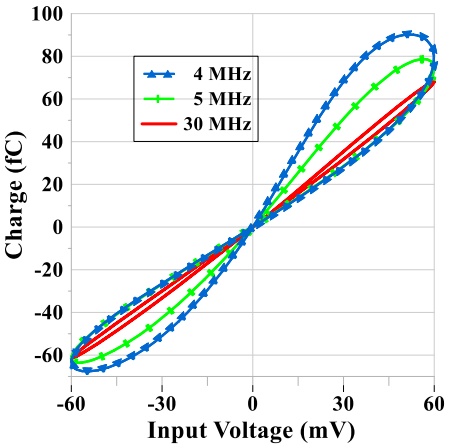


Fig. 5 Hysteresis loops obtained at frequencies of 4 MHz, 5 MHz, and 30 MHz when the input voltage is 60 mV

loops become more linear. To demonstrate the electronic tunability of the proposed emulator circuit, the values of R_{eq} and C_2 are varied electronically. The voltage V_C of the electronic resistor is set to three different values: 440 mV (corresponding to $R_{eq} = 8.1$ kΩ), 460 mV ($R_{eq} = 6$ kΩ), and 480 mV ($R_{eq} = 4.6$ kΩ). The resistance decreased with an increase in V_C. This decrease in resistance increased the variable part of the memcapacitance, as described by Eq. (11). The changes in the variable part are illustrated by the hysteresis curves shown in Fig. 6.

The capacitance of MOS capacitors is affected by both the bulk voltage (V_{Bulk}) and the gate-source voltage (V_{GS}). The relationship between capacitance and V_{GS} varies based on the bulk voltage, as shown in Fig. 7a. When the CCII-based emulator circuit is operated at a frequency of 5 MHz and the bulk voltage of the MOS capacitor is set

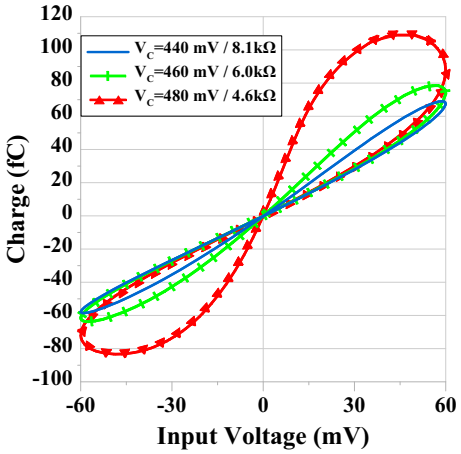


Fig. 6 Hysteresis loops obtained when voltage V_C of the electronic resistor is 440 mV, 460 mV, and 480 mV

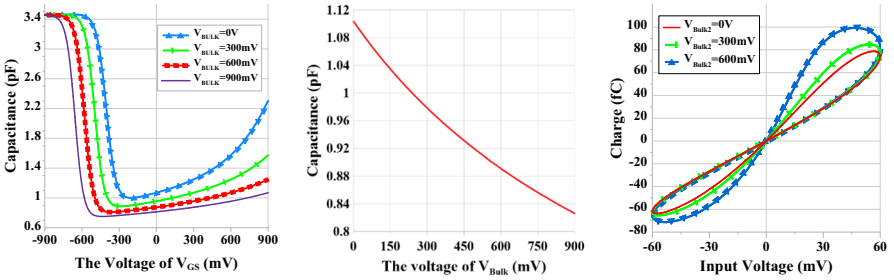


Fig. 7 **a** Capacitance values according to voltages V_{Bulk} and V_{GS}. **b** The effect of the change in V_{Bulk} voltage on the capacitance. **c** Hysteresis loops according to change in bulk voltage of the MOS capacitance C_2

to 0 V, V_{GS} on the MOS capacitors varies from − 223 to 360 mV. Correspondingly, as illustrated in Fig. 7a, the capacitance varies between 1 and 1.3 pF. The capacitance graph obtained by maintaining a constant V_{GS} voltage at an average value of 70 mV and varying the bulk voltage between 0 and 900 mV is shown in Fig. 7b. As the bulk voltage of the MOS capacitor increases, there is a corresponding decrease in the capacitance of capacitor C_2. This decrease leads to an increase in the variable part of the memcapacitor in accordance with Eq. (11). The effect of these changes on the emulator circuit is demonstrated by the hysteresis loops shown in Fig. 7c.

The temperature stability of the circuit is examined by applying an input voltage of 60 mV at a frequency of 5 MHz. Results at temperatures of − 25 °C, 27 °C, and 80 °C are presented in Fig. 8. An examination of the results shown in Fig. 8 indicates that although the amplitude of the hysteresis loop varies with temperature, the overall characteristic structure of the circuit remains relatively stable. In the Monte Carlo analysis, 100 iterations were conducted on the width (W) and length (L) values (with 5% tolerance) of the MOSFETs, which acted as capacitors and electronic resistors

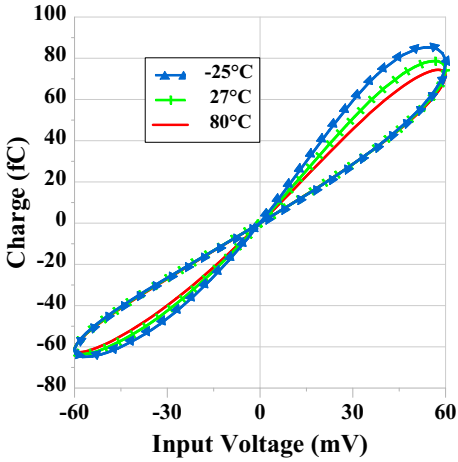


Fig. 8 Hysteresis loops for temperatures of − 25 °C, 27 °C, and 80 °C

in the circuit. The resulting hysteresis loops depicted in Fig. 9 demonstrate that even with a 5% tolerance for the specified parameters, the circuit continues to exhibit its fundamental characteristics.

To assess the non-volatile behavior of the proposed circuit, positive pulses with an amplitude of 60 mV and width of 10 ns are applied at intervals of 10 ns. Figure 10a and b shows the voltage and charge graphs of the increasing and decreasing structures, respectively. Although the amplitude of the applied voltage remains constant, a change in charge can be observed. Based on the equation $C = q/V$, a change in charge with a constant voltage suggests a directly proportional change in the capacitance. The charge measurement in the circuit is determined by the voltage across capacitor C_1, as indicated in Eq. (6). When the voltage applied to the circuit is reduced to zero, the voltage across the C_1 capacitor also appears to be zero, resulting in the charge being immeasurable and displaying zero. However, upon reapplying the voltage, the

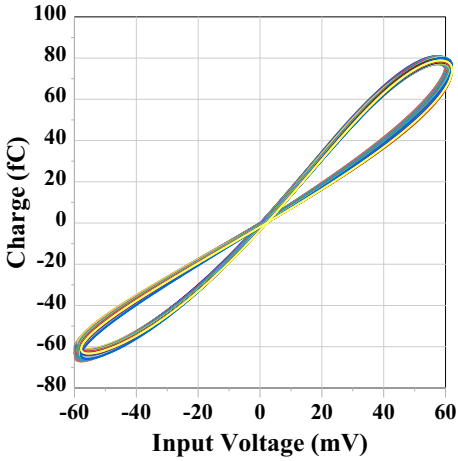


Fig. 9 Result of 100 iterations of Monte Carlo analysis with 5% tolerance

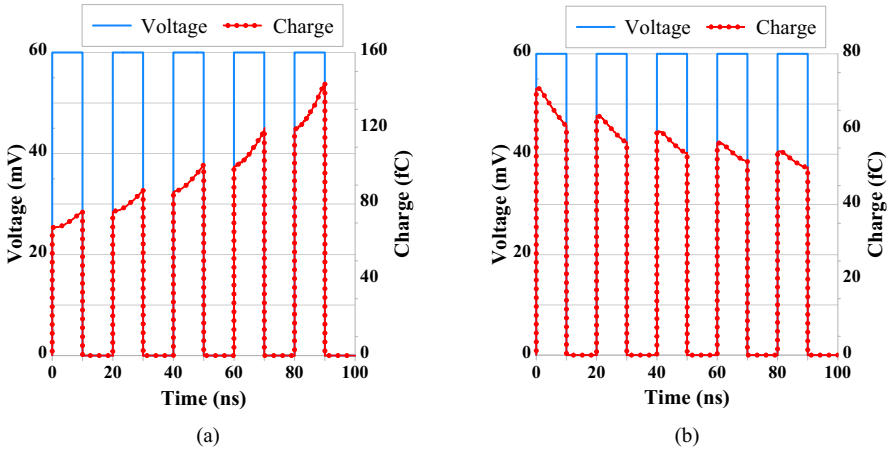


Fig. 10 Non-volatile behavior of the **a** incremental structure and **b** decremental structure of the CCII-based emulator circuit

charge continues from where it left off, in accordance with the increasing–decreasing structure. This behavior demonstrated the non-volatile nature of the circuit.

4.2 Simulation Results for OTA-Based Floating Memcapacitor Emulator Circuit

The internal structures of the OTA elements are shown in Fig. 11. The OTA element is designed using MOSFETs, according to the TSMC 0.18-μm process parameters, with the MOSFET dimensions listed in Table 2. The lengths of the transistors are chosen to be large enough to increase the parasitic resistance at the Z terminal of the OTA ($r_{o6}//r_{o8}$). Notably, the output resistance of MOSFET is proportional to the length of MOSFET; accordingly, as the lengths of the transistors increase, the voltage on the

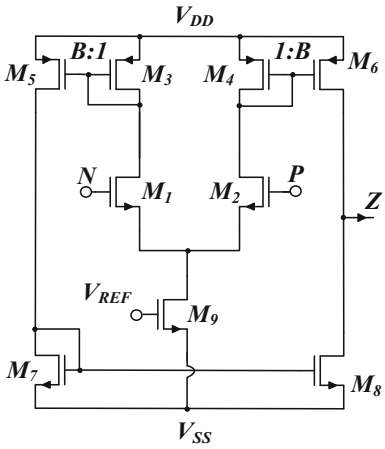


Fig. 11 Internal structure of the OTA element

Table 2 Dimensions of MOSFETs used in the OTA element

MOSFETs	W (μm)	L (μm)
M_1, M_2, M_3, M_4, M_9	3.6	1.8
M_5, M_6	7.2	1.8
M_7, M_8	2.4	1.8

capacitance is minimally affected by the parasitic resistance at the Z terminal. In the simulation, the output resistance is measured as 767 kΩ.

The supply voltages of the OTA element are set to $V_{DD} = -V_{SS} = 0.9$ V. In the OTA structure, the bulk terminals of the p-type MOSFETs are connected to the source, while the bulk terminals of the n-type MOSFETs are connected to a minimum voltage of − 0.9 V. The dimensions of the transistors that comprise the MOS capacitors in the circuit are chosen as $W/L = 100\mu m/4\mu m$.

In all analyses of the OTA-based circuit, unless otherwise specified, the input signal is set to a 60-mV, 4-MHz sinusoidal signal. The V_{REF} voltage is maintained at − 200 mV, and the g_m value of the circuit is fixed at 39.73 μA/V. In addition, the voltage at the bulk terminals of the MOS capacitors within the circuit is 0 V.

By setting the multiplier element in the circuit shown in Fig. 2 to positive and negative values, the circuit can be transformed into a decremental or incremental structure. In these studies, because the multiplier element is chosen to be positive, a decreasing structure is used for the simulations.

The voltage–charge graph of the OTA-based decremental circuit is depicted in Fig. 12a, while the graph for the incremental circuit is shown in Fig. 12b. To examine the response of the circuit at various frequencies, the input signal frequency is set to 2, 4, and 30 MHz, respectively. The hysteresis loops that result from these frequency adjustments are shown in Fig. 13. As the frequency increases, the hysteresis loops

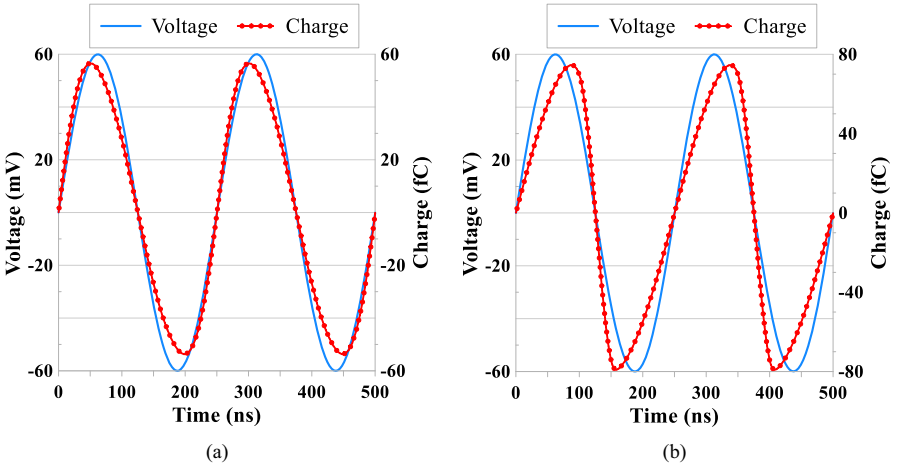


Fig. 12 Charge–voltage graph of the OTA-based circuit **a** decremental structure and **b** incremental structure

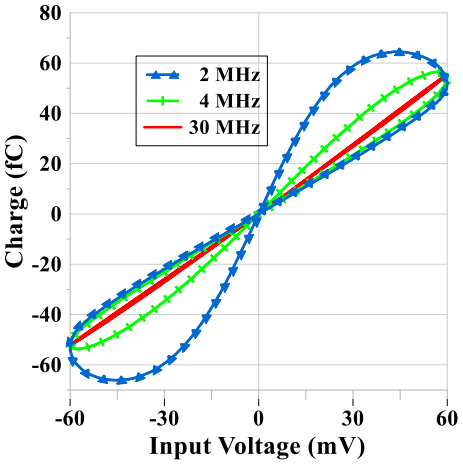


Fig. 13 Hysteresis loops obtained at frequencies of 2 MHz, 4 MHz, and 30 MHz

exhibit a more linear behavior.

The proposed emulator circuit can be electronically adjusted by changing the g_m value of the OTA element and the capacitance value of the MOS capacitorC_2. To change the g_m value of the OTA element, the voltage V_{REF} can be adjusted to − 400 mV ($g_m = 5$ µA/V), − 200 mV ($g_m = 39.73$ µA/V), or 0 V ($g_m = 85.83$ µA/V). As shown in Eqs. (16) and (17), there is a direct correlation in which the g_m value of the OTA element increases with V_{REF}. This relationship is visually represented in Fig. 14, which shows that an increase in g_m corresponds to an increase in the variable part of the memcapacitance.

The relationship between the bulk voltage and capacitance of the MOS capacitor C_2 is shown in Fig. 7a. The MOS capacitors utilized in both the CCII- and OTA-based emulator circuits are identical in size. The hysteresis loops corresponding to the bulk voltages of 0, 450, and 900 mV are shown in Fig. 15. As the bulk voltage

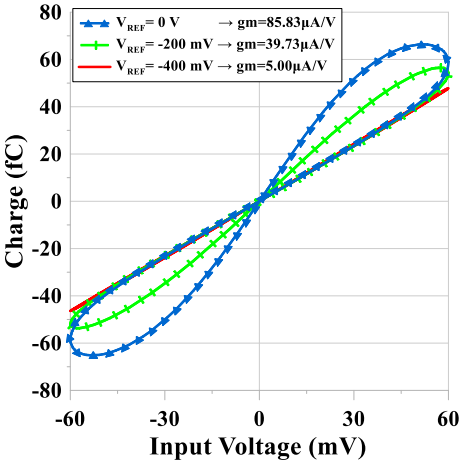


Fig. 14 Hysteresis loops according to change in voltage V_{REF} of the OTA element

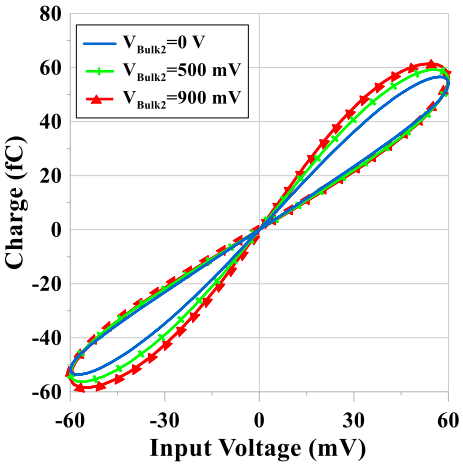


Fig. 15 Hysteresis loops according to change in bulk voltage of MOS capacitance C_2

increases, a decrease in the capacitance of C_2 is observed, increasing the fixed part of the memcapacitance. In operational conditions where the circuit is set to a frequency of 4 MHz and the bulk voltage of the MOS capacitor is maintained at 0 V, the voltage V_{GS} on the MOS capacitors fluctuates between − 444 and 121 mV. This results in a capacitance range of 1.13–2.76 pF. To investigate the temperature stability of the circuit, temperatures of − 25 °C, 27 °C, and 80 °C are selected in the LTspice program, and the results are shown in Fig. 16.

For the Monte Carlo analysis, the tolerance values for the width (W) and length (L) of the MOS capacitors used in the circuit are set to 5%. The analysis results for 100 hysteresis loops, presented in Fig. 17, indicate that there is minimal change in the behavior of the circuit at the 5% tolerance level.

To evaluate the non-volatile behavior of the circuit, positive pulses with an amplitude of 60 mV and a width of 20 ns were applied at intervals of 20 ns. When the signal is

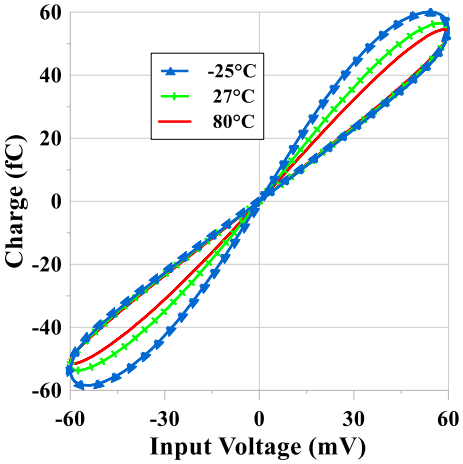


Fig. 16 Hysteresis loops for the selected temperatures of − 25 °C, 27 °C, and 80 °C

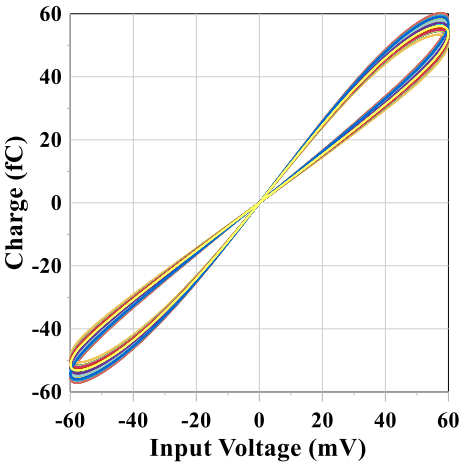


Fig. 17 Result of 100 iterations of Monte Carlo analysis with 5% tolerance

applied to the decremental structure of the memcapacitor circuit, a progressive decrease occurs in the charge for each pulse, as illustrated in Fig. 18a. Conversely, when the signal is applied to the incremental structure, the charge increases incrementally with each pulse, as shown in Fig. 18b. The circuit retains its last charge value and resumes operation from the point of interruption between two consecutive positive pulses.

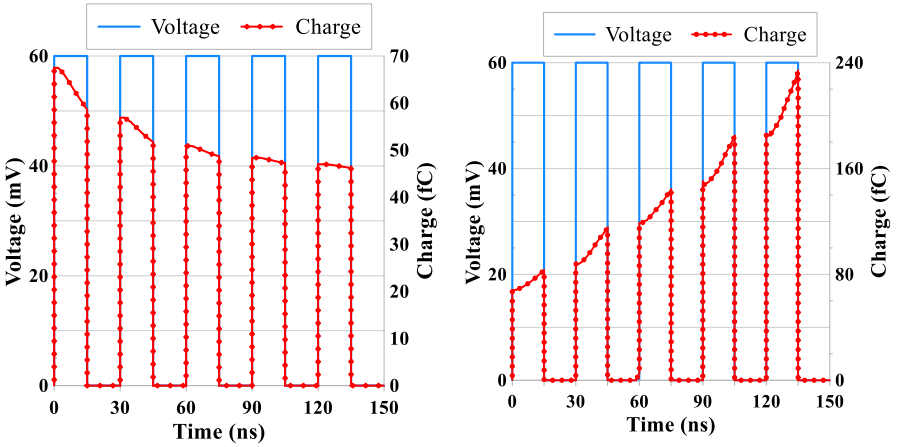


Fig. 18 Non-volatile behavior of the **a** decremental structure and **b** incremental structure of the OTA-based emulator circuit

5 Emulating Amoeba Behavior with Adaptive Learning Using Memcapacitor Emulator Circuits

Saigusa et al. [39] demonstrated that amoeba-like cells possess the ability to learn and modify their behavior in anticipation of upcoming stimuli. Serial RLC circuits with memory elements were used in previous studies [10, 11, 32, 51, 52] to electrically simulate this behavior. To demonstrate the effectiveness of the memcapacitor emulator circuits proposed in this study, a series RLC circuit is established, and the adaptive learning behavior of the amoeba is modeled by connecting the proposed memcapacitor emulator instead of the capacitor. In Fig. 19, the adaptive learning behavior of an amoeba is modeled to demonstrate the effectiveness of both the CCII-based and OTA-based memcapacitor emulator circuits.

Both circuits are tested using the same procedure. The resistance value in the circuit is 1 kΩ, and the inductance value is 1 μH. Input signals with − 100 mV amplitude and duration of 40 ns are applied to the circuits.

For the CCII-based circuit, Fig. 20a shows that for a delay of 320 ns between the first and the second input signals, the corresponding output signals are − 141 mV and − 146 mV, respectively. In another scenario shown in Fig. 20b, when three signals are applied at intervals of 20 ns, the output signal initially increases up to − 187 mV for

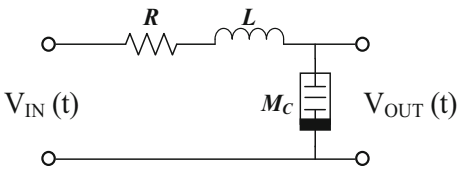


Fig. 19 Adaptive learning circuit using memcapacitor with $R = 1$ kΩ and $L = 1$ μH

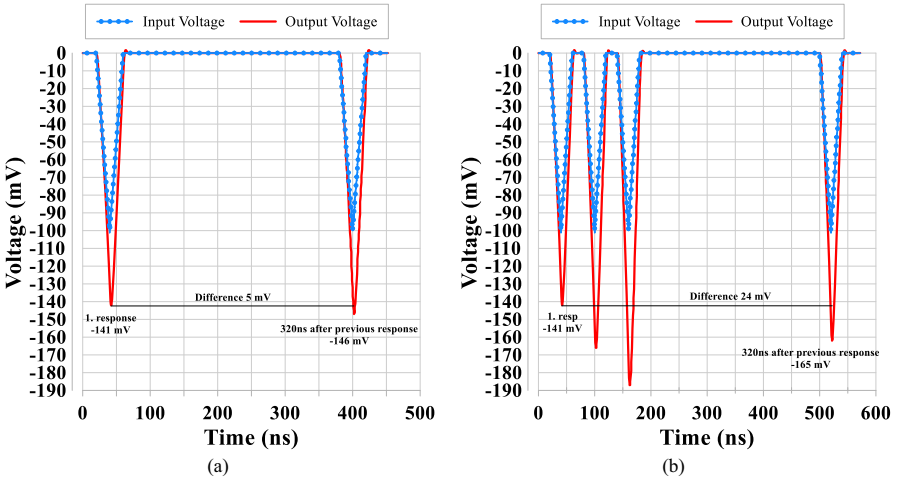


Fig. 20 Response of the CCII-based circuit 320 ns after **a** one signal is applied and **b** three signals are applied

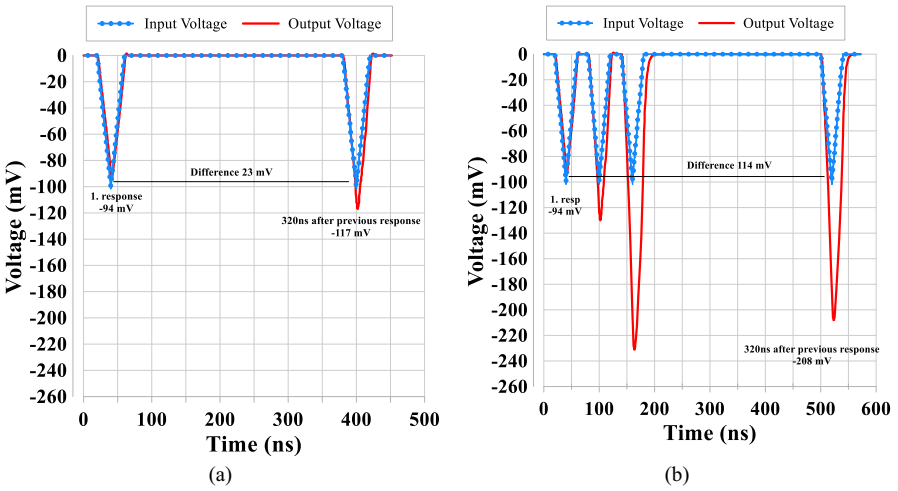


Fig. 21 Response of the OTA-based circuit 320 ns after **a** one signal is applied and **b** three signals are applied

the first three signals. Thereafter, when an input signal is applied again after a delay of 320 ns, the output voltage is measured as − 165 mV.

In the OTA-based circuit, two signals are initially applied with an interval of 320 ns between them, as illustrated in Fig. 21a, similar to the approach used in the CCII-based circuit. When the first signal is applied, it can be observed that the output signal of the circuit is − 94 mV and the second output signal is − 117 mV. In the second simulation, as illustrated in Fig. 21b, three signals are initially applied to gauge the system response, followed by an additional signal after a delay of 320 ns. When three signals are applied in the simulation, it is observed that the output of the third signal reaches − 230 mV. Subsequently, after a 320 ns delay and damping of the entire system, another signal was applied. Upon measuring at this stage, the output signal is found to be − 208 mV.

In simulation studies performed by waiting for 320 ns after a single signal, it is observed that the circuit cannot fully learn the stimulus and tends to forget it. In contrast, in the second experiment, in which three signals are first applied and the signal is reapplied after waiting for 320 ns, it is revealed that the circuit learns the stimulus following the first three stimuli. Consequently, a more pronounced reaction can be observed than in the first experiment when the same signal is reapplied after the same delay.

6 Experimental Results

In the proposed circuit, MOSFETs are employed instead of passive elements, and simulation studies are conducted to analyze the performance of the circuit without using passive elements. To conduct experimental tests on this circuit, it must be produced as an integrated circuit. Owing to the unavailability of integrated circuit production

equipment, experimental studies have been conducted using discrete elements on PCB. Although MOS capacitor structures are suitable for integrated circuits, the desired values cannot be obtained on a PCB. Therefore, ceramic capacitors are employed instead of MOS capacitors in these experiments. However, using discrete components on the PCB instead of integrated circuits not only limits the frequency of the circuit to the limits of elements, such as AD633 and AD844, but also requires operating the circuit at lower frequencies to mitigate parasitic effects. This frequency reduction necessitates the use of capacitors larger than those used in the simulations, resulting in the selection of larger capacitor sizes for experimental studies.

The proposed circuit is composed of one AD844, one AD633, a 10 kΩ resistor, and two 470 pF capacitors. As shown in Eqs. (11) and (12), the inverse capacitance is defined in terms of the input voltage and charge. While the input voltage is measured directly as floating, the charge is obtained by multiplying the voltage at the Y terminal by the capacitance C_1, as shown in Eq. (6). Figure 22a displays the macromodel used in this experimental study. Figure 22b and c presents the structure of this macromodel on the PCB and the results obtained during circuit operation, respectively.

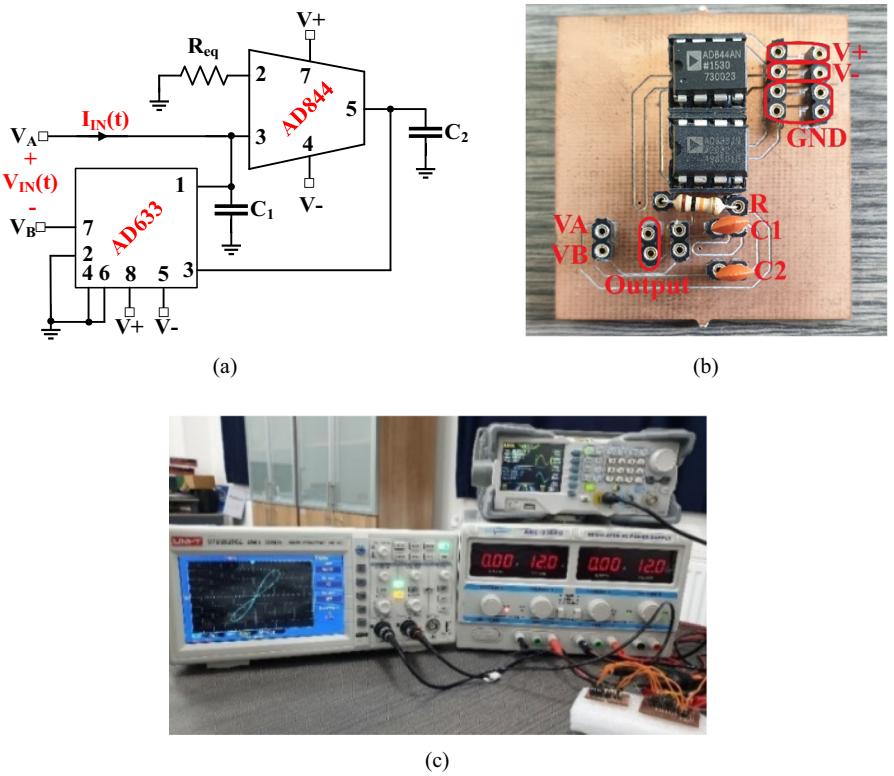
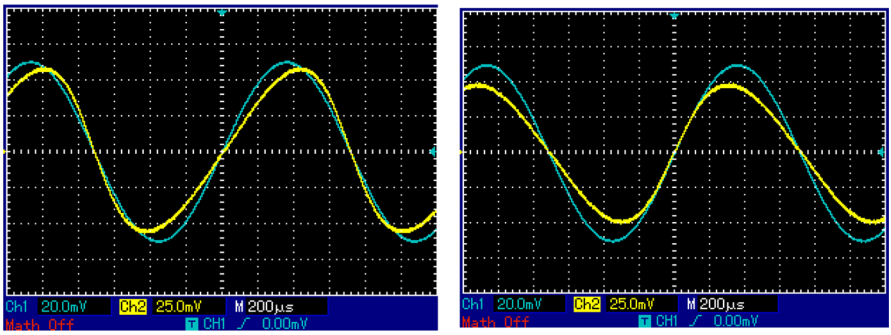


Fig. 22 Proposed circuit's **a** macromodel, **b** PCB front-side layout, and **c** hysteresis loop obtained using an oscilloscope



(a) (b)

Fig. 23 Voltage–charge graph of the **a** incremental structure and **b** decremental structure

The circuit operates with a supply voltage of $\pm$ 12 V, and a sinusoidal input signal with an amplitude of 100 mV and a frequency of 700 Hz is applied. Based on (11) and (12), the circuit can be configured to exhibit increasing and decreasing behaviors, respectively. When the multiplier element in the circuit is set to a positive value, it results in an incremental structure, as shown in Fig. 23a. Conversely, setting the multiplier element to a negative value leads to a decremental structure, as illustrated in Fig. 23b. The blue and yellow lines on the oscilloscope display correspond to the applied voltage and charge, respectively. To evaluate the frequency response of the circuit, the operating frequencies are set to 500 Hz, 700 Hz, 1 kHz, and 4 kHz, and the resulting hysteresis loops are shown in Fig. 24. An analysis of the results reveals that, as expected, the hysteresis loops of the circuit tend to become more linear as the frequency increases. Despite the variations in frequency, the hysteresis curve largely retains its symmetrical structure. In addition, the slight shift in the origin of the curve observed at lower frequencies diminishes as the frequency increases, resulting in the midpoint of the hysteresis loop approaching the origin.

To analyze the impact of the passive components within the circuit, the values of the resistor R_{eq} and the capacitor C_2 are adjusted. R_{eq} is set to three different values: 6.8 kΩ, 10 kΩ, and 15 kΩ. The oscilloscope images shown in Fig. 25 display the results of these modifications. The capacitance of C_2 capacitor was set to 330, 470, and 680 pF, respectively. Oscilloscope images that capture the results of these variations are presented in Fig. 26. As demonstrated in Eq. (11), an increase in the values of R_{eq} and C_2 decreases the fixed part of the memcapacitor.

The experimental results indicate that an increase in the values of R_{eq} and C_2 decreases the fixed part of the circuit, resulting in a more linear hysteresis.

To examine the non-volatile behavior, a 2 kHz square signal with an amplitude of 100 mV is applied to the emulator circuit. In the oscilloscope screenshot depicted in Fig. 27, the measured input voltage is displayed in blue. As the memcapacitor expression cannot be directly shown, the charge is derived by measuring the voltage across capacitor C_1, in accordance with Eq. 6. Since the capacitance of C_1 is constant, dividing the voltage by the capacitance of C_1 according to the $q = CV$ formula allows the charge shown in yellow on the oscilloscope screenshot to be displayed.

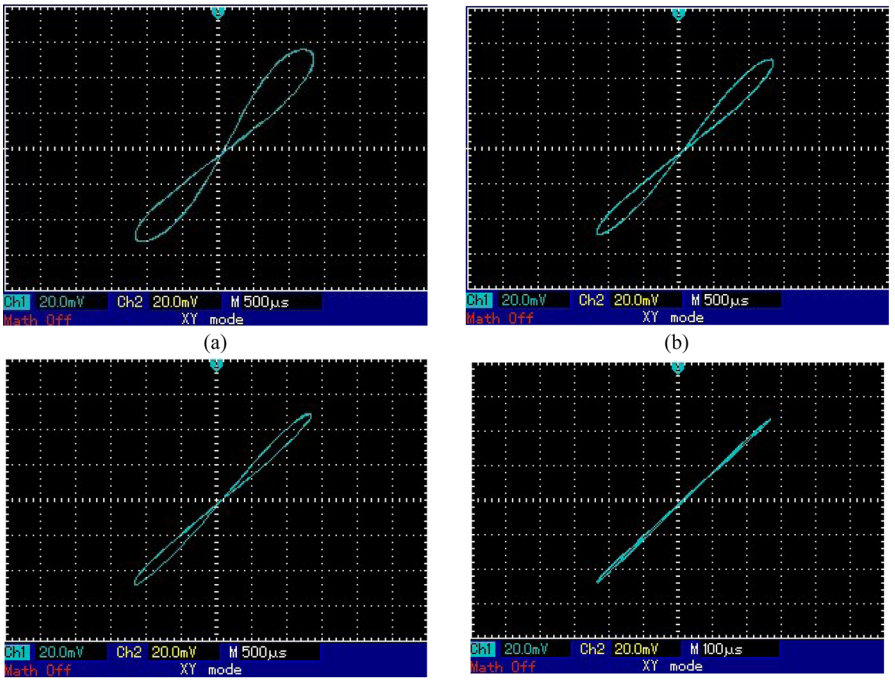


Fig. 24 Hysteresis loops observed using an oscilloscope at frequencies of **a** 500 Hz, **b** 700 Hz, **c** 1 kHz, and **d** 4 kHz

Figure 27a and b shows the non-volatile behavior of the circuit in the incremental and decremental structures, respectively. The results reveal that as the direction of the input voltage changes, the charge expression resumes from its previous position and displays symmetry about the x-axis.

7 Conclusion

In this study, two electronically controllable floating memcapacitor emulator circuits based on CCII and OTA are presented. The first proposed circuit contains a single CCII, analog multiplier, and four MOSFETs, while the second comprises a single OTA, analog multiplier, and two MOSFETs. In the first proposed circuit, two MOSFETs (M_{R1} and M_{R2}) work as electronically tunable grounded resistors, whereas two MOSFETs (M_{C1} and M_{C2}) act as electronically tunable grounded capacitors. For the second proposed circuit, two MOSFETs (M_{C1} and M_{C2}) act similarly as electronically tunable grounded capacitors, while the transconductance gain of the OTA can be tuned by the bias voltage (V_{REF}). Therefore, the inverse memcapacitance of both proposed circuits can be controlled electronically. Simulation results are presented considering different performance parameters to examine the performance of both circuits. Furthermore, temperature and Monte Carlo analyses were performed in simulation

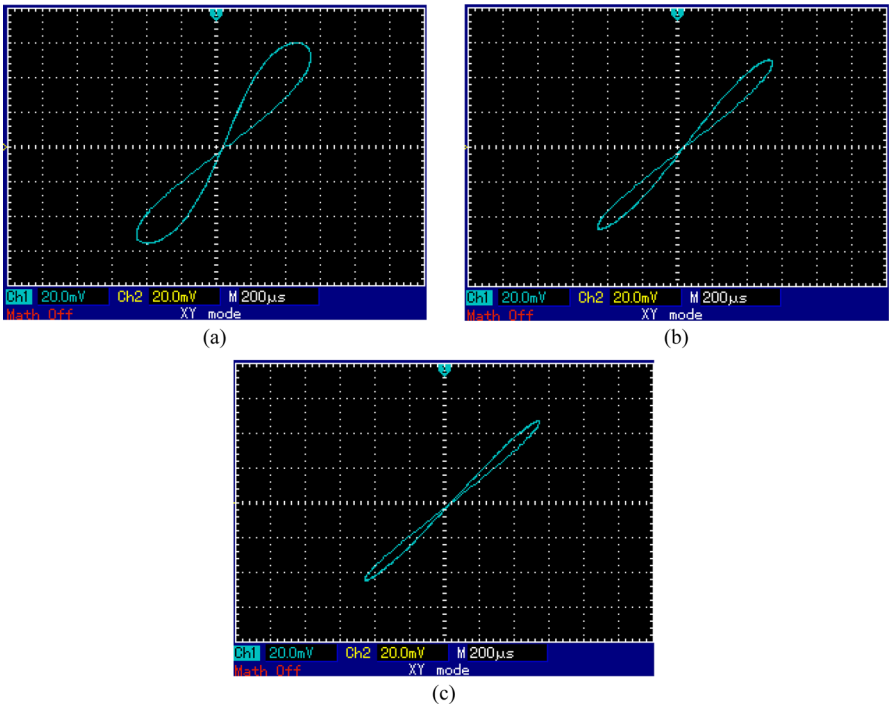


Fig. 25 Oscilloscope results when the resistance value of R_{eq} is set to **a** 6.8 kΩ, **b** 10 kΩ, and **c** 15 kΩ

studies of both circuits. The non-volatile behavior of the circuits was analyzed in both the incremental and decremental structures, and the memory effect of the circuit was demonstrated. Considering their memory properties, memelements have significant potential for applications in neuromorphic circuits and biological system mimics. As an example of the application of the proposed memcapacitor circuits, an RLC circuit was established to mimic an amoeba-like cell, utilizing a memcapacitor instead of a conventional capacitor to exploit its adaptive capabilities. In addition to the simulation studies, experimental studies were conducted by implementing a CCII-based circuit on a PCB. As the circuit was constructed on a PCB rather than on an integrated circuit, it is designed using passive circuit elements instead of MOSFETs. Frequency analyses of this circuit were performed, and the effects of changing the passive circuit elements on the circuit were demonstrated. In conclusion, the simulation, experimental, and application results agree well with those of previous studies.

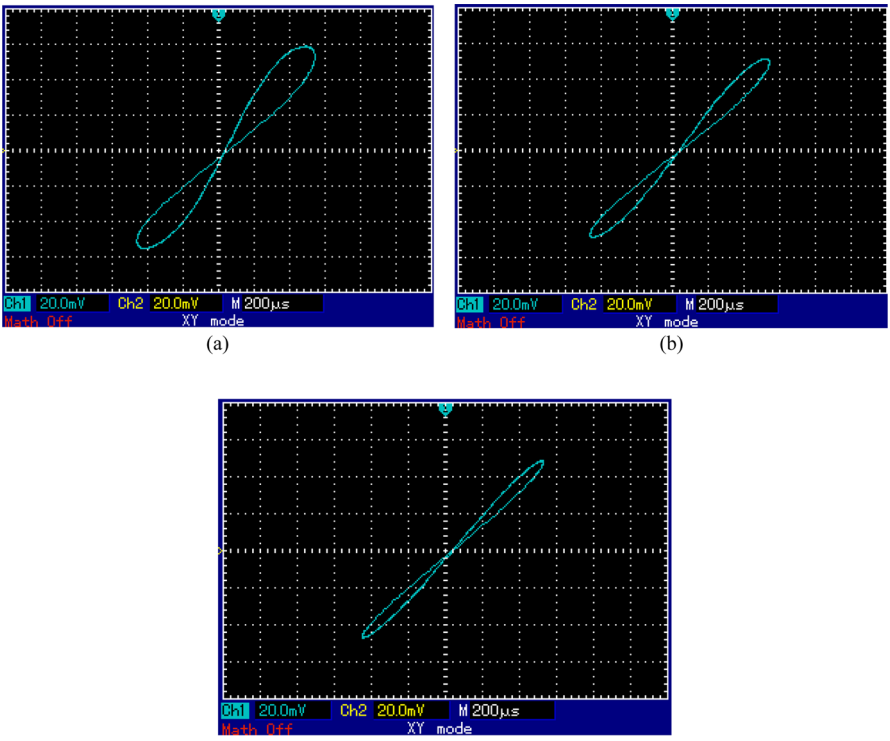


Fig. 26 Oscilloscope results when the capacitance of C_2 is set to **a** 330 pF, **b** 470 pF, and **c** 680 pF

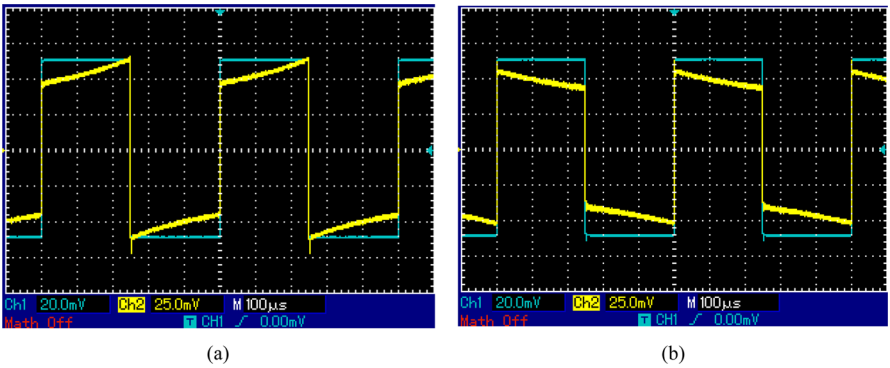


Fig. 27 Non-volatile behavior of the circuit at 2 kHz for **a** incremental structure and **b** decremental structure

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Data availability Data sharing is not applicable to this article, as no datasets were generated or analyzed during the current study.

Declarations

Conflict of interest The corresponding author declares no conflicts of interest regarding the publication of this paper.

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