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A Wide Dynamic Range CMOS Differential Rectifier for Radio Frequency Energy Harvesting Systems

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Abstract
In this paper, a radio frequency energy harvesting system with a wide dynamic range rectifier is presented. This rectifier has two feedback and feedforward structures. These paths keep the rectifier's power conversion efficiency (PCE) high at different input powers and thus create a high dynamic range (DR). This rectifier also has better sensitivity. Advances in the rectifier contribute to more satisfactory results for the final system. The circuit is simulated with 180 nm TSMC CMOS technology at a frequency of 900 MHz. Also, a π-type input impedance matching network circuit is used. This circuit is matched at $P_{\text{in}} = -19.5$ dBm and $f = 900$ MHz. In addition, an off-chip balun is utilized to convert the received single-ended signal to the differential one. The achieved PCE and DR are 86.03% and 9.76 dB, respectively, with a sensitivity of -19.32 at 1 V output voltage. Furthermore, the overall circuit results indicate a PCE of 76.13%, a DR of 6.3 dB, and a sensitivity of -18.75 dBm.

Keywords Radio frequency energy harvesting · Differential CMOS rectifier · Impedance matching network · Power conversion efficiency · Dynamic range · Sensitivity

1 Introduction

Today, one of the challenges facing electronics engineers is the power supply of devices that are impractical to connect directly to wiring or batteries. Although the same methods (especially battery usage) are still used to supply power, researchers are

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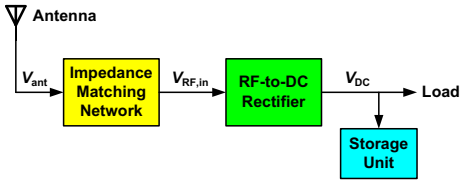


Fig. 1 Block diagram of an RF energy harvesting system

looking for new ways to make it easier. Batteries have a limited lifetime, which raises the problem of replacing them after a certain time. For example, in the medical field [4], replacing the batteries of implants in the body can be very dangerous and expensive at the same time. In the case of the radio-frequency identification (RFID) [13], Internet of Things (IoT) or wireless sensor networks [10, 23, 26], the replacement of the battery is extremely tedious due to the large number of sensors, which may be located in dangerous areas. An alternative solution to this predicament is the utilization of environmental energies that are typically overlooked. Energy harvesting is a method that uses energy from the environment, such as radio-frequency signals [16, 17], solar [5], piezoelectric [28], heat [3], etc. to convert it into energy that can be used by sensors and electrical devices. The energy obtained from this method has very low power, but it is enough to operate low-power devices. Energy harvesting systems are usually classified according to their energy source. The most commonly used systems are vibration energy, thermal energy, light energy, and electromagnetic energy. In this paper, we intend to investigate the conversion of radio-frequency signals' energy into DC energy that can be used by sensors.

The task of the radio-frequency energy harvesting (RFEH) system is to receive the input energy and convert it to DC energy for an electric load or store it in a storage unit. A general block diagram of an RFEH system is illustrated in Fig. 1. The system includes an antenna, an impedance matching network, an RF rectifier, and a storage capacitor. These systems have three important parameters. Sensitivity is the lowest input power needed to produce the minimum usable DC voltage for a load. The power conversion efficiency (PCE) is the ratio of the output power delivered to the load to the power at the circuit's input. Dynamic range (DR) is also a range of input power whose PCE is greater than a specific ratio of its maximum. In this paper, we consider the range above 80% of the maximum PCE as the DR [15].

Today, Dickson and differential rectifiers are widely used. The Dickson rectifier [9] operates with ordinary diodes or Schottky diodes. As depicted in Fig. 2a, the Dickson model can be implemented in standard CMOS technology using diode-connected transistors. But we will face a high voltage drop (at least one threshold voltage) resulting in reduced PCE especially at low input powers. Because of the diode-connected structure, this scheme exhibits low return current at both high and low input powers, offering an advantage in terms of low current leakage. To solve the problem of this type of rectifiers, auxiliary circuits are usually used to supply part of the threshold voltage of the transistors and the so-called threshold voltage compensation is done in [25]. The structure of this system is such that it compensates for the threshold voltage using four-stage combinations. These compounds consist of transistors that are in the sub-threshold region. Using this structure, Dickson's low-sensitivity problem is partially

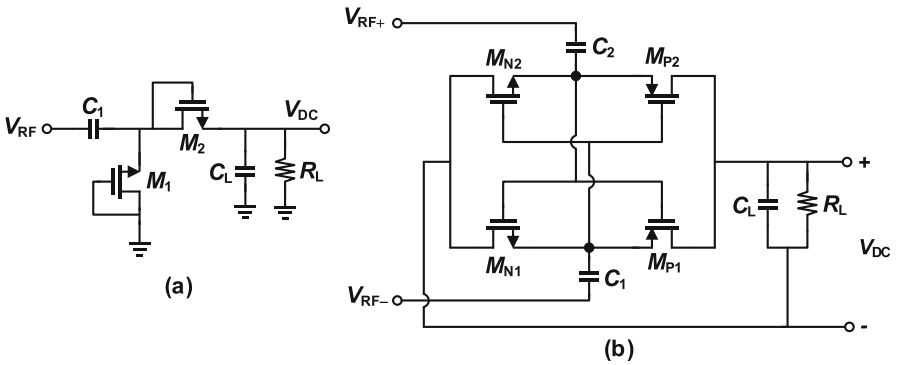


Fig. 2 **a** Dickson rectifier [9] and **b** conventional differential one [13]

solved, and the circuit has a high-power conversion efficiency over a wide range of input powers. Compensation is also done in such a way that the level of compensating voltages is limited and varies according to the input power. In this work, a kind of intelligent compensation has been done.

A differential rectifier is shown in Fig. 2b [13]. In the steady-state and when this circuit operates in its positive cycle, the gate of transistor M_{N1} is tied to the positive voltage, and its source is tied to the negative voltage, so in this state, this transistor is on. Simultaneously, the source of transistor M_{P2} is linked to the positive voltage, and its gate to a negative voltage, making it also on. In this case, we will have a loop that transmits the input power to the circuit, rectifies the signal, and charges the output capacitor. Likewise, transistors M_{N2} and M_{P1} will be on when the circuit is in its negative cycle, forming another charge loop. This rectifier can work at low power with high PCE. Transistors in this structure operate in the linear region, so these transistors will have a lower voltage drop resulting in less power being lost in the rectifier itself. The disadvantage of this rectifier type is the high reverse current of these transistors at higher input powers.

Auxiliary feedback circuits are used to solve this problem. In Fig. 3, a structure is

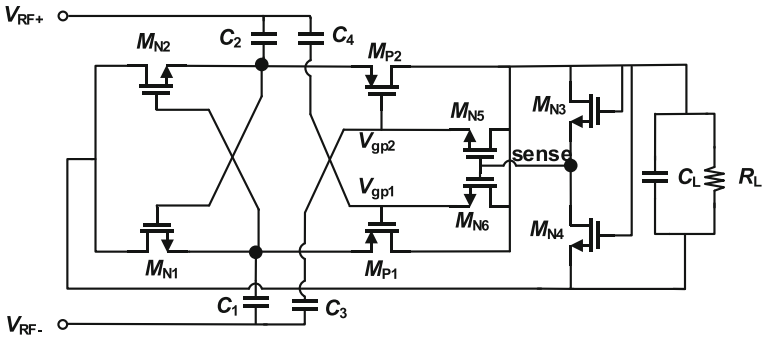


Fig. 3 Differential rectifier using transistor feedback network presented in [21]

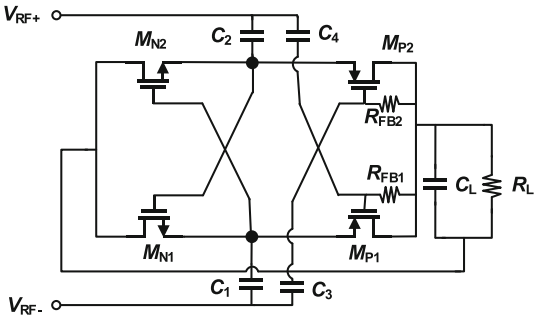


Fig. 4 Proposed differential rectifier using resistors as a feedback system in [22]

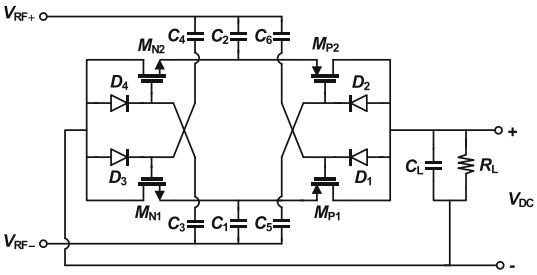


Fig. 5 Differential rectifier using diode-connected transistors, presented in [2]

introduced by utilizing transistors to generate a feedback network from the output to the gate of P-type transistors. This feedback network turns off the P-type transistors at high input power levels to prevent the discharge of the output energy. Unfortunately, this structure reduces the output resistance. Also, this configuration does not offer a path to improve efficiency at low capacities [21]. In [22], instead of using the large feedback circuit, only resistors R_{FB1} and R_{FB2} are used. As illustrated in Fig. 4, these two resistors have a very large value. Although this method increases the dynamic range in the rectifier, it limits the input current and reduces the efficiency at high input powers.

The circuit illustrated in Fig. 5 presents a less defective structure compared to others [2]. As can be seen, in this configuration, the auxiliary circuit endeavors not to disturb the input current. This reference suggests the usage of diode-connected transistors. Specifically, transistors D_1 and D_2 remain off at low input powers. However, at higher input powers, when the output voltage exceeds the input voltages, these diodes activate to turn off the main P-type transistors. Consequently, the return current from these transistors is significantly reduced. Unfortunately, the return current of N-type transistors is not considered in this structure. On the left side of the circuit, diode-connected transistors are employed. These transistors are introduced to boost the input current, but due to their high threshold voltage, they typically remain off and do not contribute positively to the circuit.

In [19], a novel high dynamic range rectifier has been suggested, which reduces reverse current, increases forward current, and ultimately, improves the rectifier's PCE, sensitivity, and DR. This paper provides detailed circuit operation and analysis, along

with extensive post-layout simulation results. Additionally, the design of the input impedance matching network and the entire energy harvesting system is reported.

The remainder of the paper is organized as follows: Sect. 2 presents the structure of the proposed RF energy harvesting system with a detailed description and analysis of the proposed CMOS rectifier. Post-layout simulation results are provided in Sect. 3. The conclusion is presented in Sect. 4.

2 Proposed RF Energy Harvesting System

In this section, the proposed RF energy harvesting system is described, with the rectifier at its core being initially expounded upon. The second part covers the rest of the circuit, including the matching network, balun, and antenna.

2.1 Proposed Differential Rectifier

As shown in Fig. 6a, the proposed rectifier consists of a conventional differential rectifier and 8 diode-connected PMOS transistors. These diode-connected transistors, which we call diodes in this article, give the feed-forward and feedback routes for this circuit. The D_1-D_4 diodes provide a feedback path and reduce the return current at high input power levels. Also, the D_5-D_8 diodes provide a feed-forward path, enhancing the power reception of the rectifier at low or medium input power levels.

In the conventional differential rectifier, when the input power is high, the absolute values of V_{DC+} and V_{DC-} exceed V_{RF+} and V_{RF-}. In this scenario, the drain and source of M_{P1}, M_{P2}, M_{N1}, and M_{N2} transistors are swapped, transforming the sources into drains and vice versa. When this happens, the rectifier begins to discharge the output capacitor, and drain its energy to reach equilibrium. This significantly reduces PCE at high input powers, consequently diminishing the DR. To counteract this situation, as illustrated in Fig. 6a, D_1–D_4 diodes are employed. In this case, because the absolute value of V_{DC+} and V_{DC-} are larger than V_{RF+} and V_{RF-}, the anode voltage of these diodes is greater than their cathode and high threshold voltage. So, D_1 and D_4 (in negative cycle), and D_2 and D_3 (in positive cycle) become ON and turn off M_{P1}, M_{N2}, M_{P2}, and M_{N1} transistors, respectively. Whit these switches (M_{P1}, M_{P2}, M_{N1}, and M_{N2} transistors) turned off, there is no pathway to discharge the output capacitor. Consequently, PCE remains unaffected, and the DR stays wide. It's essential to note that the mentioned circuit utilizes transistors M_{N1}, M_{N2}, M_{P1}, and M_{P2} as switches, functioning in either an "on" or "off" state. These transistors undergo changes in their states as time progresses, ultimately reaching a stable state. As a result, the circuit and its transistors lack a fixed bias point. The steady-state process of the rectifying system at high input power levels for M_{P2} transistor is shown in Fig. 6c.

To reduce the PCE loss, the current passing into the diodes should be low. When a PMOS diode-connected transistor operates in the saturation region, its drain-source current is given by:

$$I_{diode} = \frac{1}{2}\mu_p C_{ox}(W/L)(V_{SG} - |V_{TH}|)^2 \tag{1}$$

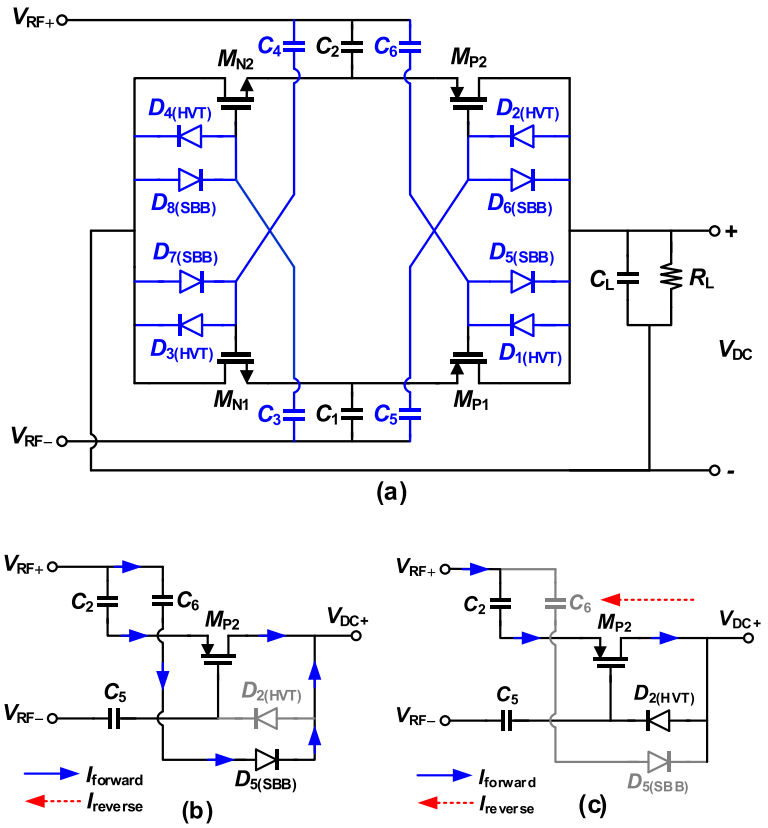


Fig. 6 **a** Suggested differential RF to DC converter and steady-state process of the rectifying systems at **b** low and **c** high input power levels

and in the sub-threshold region, it is described as:

$$I_{diode} = I_{ds0} e^{\frac{V_{SG}-|V_{TH}|}{nV_T}} \left(1 - e^{\frac{-V_{SD}}{V_T}}\right) \tag{2}$$

where n is dependent on the process, W/L is the transistor's aspect ratio, V_{TH} is the threshold voltage, V_{T} is the thermal voltage, and I_{ds0} is dependent on the aspect ratio and the process. As explained in [2], and according to the relations (1) and (2), the current passing through these diodes is directly proportional to their aspect ratio and inversely proportional to their threshold voltage. As a result, we have opted for a smaller aspect ratio, achieved by utilizing a longer channel length for these diodes. Also, we use high threshold voltage (HVT) PMOS transistors to realize D_1–D_4 diodes.

Similarly, D_5–D_8 diodes provide feed-forward paths in the circuit. These diodes are added to the rectifier to increase forward input current. When the circuit operates at low or medium input power levels, the output voltage is still lower than $V_{\mathrm{RF+}}$ and

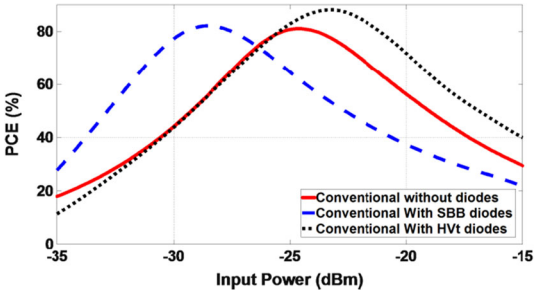
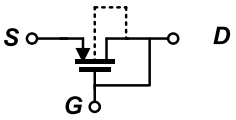


Fig. 7 Comparison of power conversion efficiency (PCE) in different circuit configurations: standard circuit (no diodes), circuit with SBB diodes only, and circuit with HVT diodes only



$V_S > V_D$ & diode on => $V_{SB} > 0$ => $|V_{TH}| \downarrow$ & $I_{fwd} \uparrow$
$V_S < V_D$ & diode off => $V_{SB} = 0$ => $I_{rev} \downarrow$

Fig. 8 Self body biased (SBB) diode-connected PMOS transistor and its operation at different situations

V_{RF-}. As a result, these diodes can turn on, creating an additional path for charging the output capacitor. All these explanations are presented in Fig. 6b and c.

A better understanding of the functions of self body biasing (SBB) and HVT diodes in a circuit can be achieved by comparing the PCE in various situations. This encompasses a standard circuit without diodes, a circuit containing solely SBB diodes, and a circuit employing only HVT diodes. It is clear that SBB diodes enhance PCE at lower input powers, while HVT diodes enable higher peak PCE and increased efficiency levels at higher input powers. This description is illustrated in Fig. 7.

According to relations (1) and (2), it is obvious that if the threshold voltage of D_5–D_8 diodes becomes lower, these diodes turn on sooner and can have a better effect on the circuit. It is also crucial that the reverse current in these diodes be smaller. By utilizing the SBB technique, beneficial in low-power systems, we can achieve both advantages. As shown in Fig. 8, in this technique, the transistor's bulk is connected to its drain instead of connecting to the source. In this case, when the diode is ON ($V_S > V_G$), according to relation (3), the absolute value of threshold voltage is less than $|V_{TH0}|$. Whereas when the bulk is connected to its source, its $|V_{TH}|$ becomes larger than or equal to $|V_{TH0}|$.

$$V_{TH} = V_{TH0} - \gamma\left(\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}\right) \tag{3}$$

In this context, V_{TH0} represents the threshold voltage without body effect, γ denotes the body effect coefficient, V_{BS} is the voltage difference between the bulk and source terminals, and the formula for the Fermi level (ϕ_F) is given by $\phi_F = (kT/q)\ln(N_{sub}/n_i)$, where k represents Boltzmann's constant, q symbolizes the elementary charge of an electron, N_{sub} stands for the doping density of the substrate, and n_i denotes the electron density in undoped silicon [24]. The typical value of $2\phi_F$ is about 0.7 V [24].

Also, when the diode is OFF ($V_S < V_G$), the positions of the source and drain terminals change with each other. In this situation, the new source-bulk voltage equals zero, while these diodes still exhibit a reverse current. We know that the higher the threshold voltage, the lower the leakage current. Under these conditions, according to (3), the absolute value of the new threshold voltage is larger than $|V_{TH0}|$, reducing the return current. In simple terms, this technique improves the performance of the proposed circuit when D_5–D_8 diodes are either ON or OFF by providing large feed-forward and small reverse currents in ON and OFF states, respectively. Additionally, proper transistor sizing helps achieve balanced operation, minimize distortion, and improve efficiency in converting RF to DC signals. Proper transistor sizing is paramount in achieving balanced operation, minimizing distortion, and improving the efficiency of RF to DC signal conversion. Our approach to selecting transistor sizes revolves around ensuring symmetry between NMOS and PMOS transistors, a critical factor in maintaining balanced signal paths. Notably, we aim for consistent behavior from both transistor types. Due to the inherent difference in charge carrier mobility, with PMOS transistors exhibiting lower mobility compared to NMOS transistors, a deliberate decision was made to size the PMOS transistors five times larger than their NMOS counterparts. This intentional disproportionality is designed to counterbalance the impact of the mobility difference and attain the desired equilibrium in circuit behavior.

Alternating currents and charges of M_{P2}'s drain are shown in Figs. 9 and 10 for the conventional and proposed rectifiers. These currents and charges are in steady state mode and represent the required amounts for generating a 1.5 V DC output. As expected, both circuits need an equal net charge to produce the same output voltage for the same loads. However, the range of forward and reverse charges in the conventional

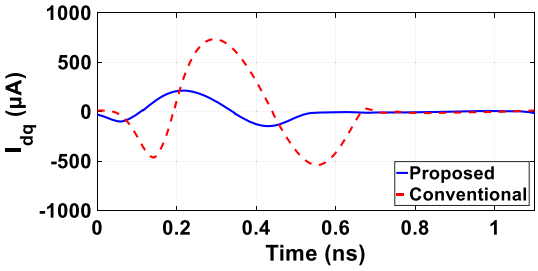


Fig. 9 Steady-state drain-source current of M_{P2} in the standard differential and suggested rectifiers to create 1.5 V output voltage

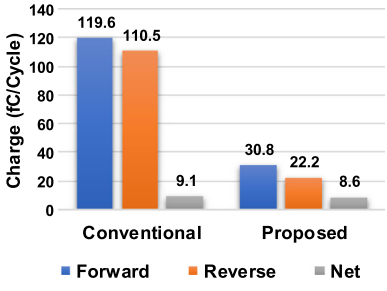


Fig. 10 Alternating charges per cycle in the standard differential and suggested rectifiers to create 1.5 V output voltage

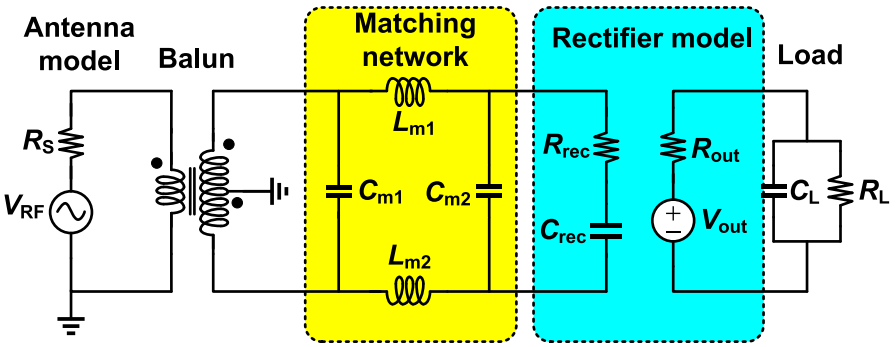


Fig. 11 The model of RF energy harvesting system

rectifier is several times larger than that of the proposed rectifier. This shows that the proposed circuit can provide the same voltage and charge at lower input power levels.

2.2 Matching Network

As shown in Fig. 11, we modeled the antenna with an RF voltage source and a 50 Ω resistor. Additionally, an off-chip balun is used to convert the single-ended input signal to a differential one. The circuit needs an input impedance matching network to transfer the maximum power from the antenna and balun to the rectifier. Moreover, because the input signal has a low voltage at the start-up of the circuit, this matching circuit serves as a passive voltage amplifier according to relation (4).

$$V_{Rec} = \frac{V_{RF}}{2}\sqrt{1+Q^2} \tag{4}$$

where V_{Rec} is the voltage at the input of the rectifier, V_{RF} is the voltage of the source, and Q is the quality factor of the circuit. In this case, due to the increase of the rectifier's input voltage, the dead zone decreases, the sensitivity increases, and the circuit starts working sooner.

In this paper, a π-type input impedance matching circuit is used. Because the circuit operates in large-signal mode and lacks direct bias, it is very difficult to design an impedance matching circuit. The input impedance of the rectifier varies with frequency, the amount of input power, and the amount of input voltage. We use the iteration technique in this situation. In the first step, the matching operation is performed for the amount of rectifier impedance observed in the non-matching mode. The mentioned matching circuit is designed and added to the rectifier circuit. Then, after doing this, the rectifier is optimized again with new values. After this step, the input impedance of the rectifier is revaluated, and a new matching circuit is designed for this new impedance. This will take several iterations and then converge to a constant value. The condition for the convergence of this value is the selection of the appropriate initial value. The loop in Fig. 12 will be rotating and repeating until the observed impedance from the rectifier head converges to a certain amount. It should be noted that naturally, after

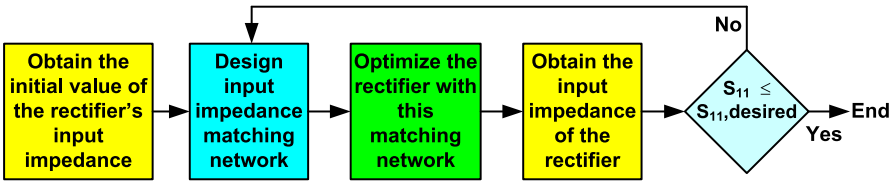


Fig. 12 Conceptual diagram of input impedance matching circuit design for nonlinear and large-signal systems

performing the necessary iterations, the impedance seen from the matching circuit should correspond to the impedance observed from the antenna and the balun. At the end, this circuit is matched at $P_{in} = -19.5$ dBm and $f = 900$ MHz.

3 Post-layout Simulation Results

The structure introduced in this paper is crafted utilizing the 180 nm RF-CMOS process through cadence design systems. This choice of design and fabrication platform allows us to demonstrate the circuit's performance. Also, the ADTL2-18 + is employed as an off-chip balun due to its suitable parameters for this application. These parameters are low S_{11}, creating low phase differences between the two sides of the differential signal. Layouts of the proposed and conventional rectifier and on-chip matching capacitor (C_{m2}) are shown in Fig. 13. C_{m2} is sized at 365 fF, a value suited for on-chip dimensions. Nonetheless, larger inductors and capacitor are needed for L_{m1}, L_{m2}, and C_{m1}, making it more pragmatic to place them outside the chip. As illustrated in Figs. 11 and 13, C_{m2} occupies the initial position on the left side of the IC. Hence, it is viable to establish a direct connection between C_{m2} and the rest of the components within the matching network situated externally to the chip. Metal–insulator–metal (MIM) capacitors are used for capacitors, NMOS2V transistors are used for N-type transistors, PMOS2V transistors are used for P-type transistors and feedforward diodes, and PMOS3V transistors are used for high-threshold diodes. It is noteworthy to mention

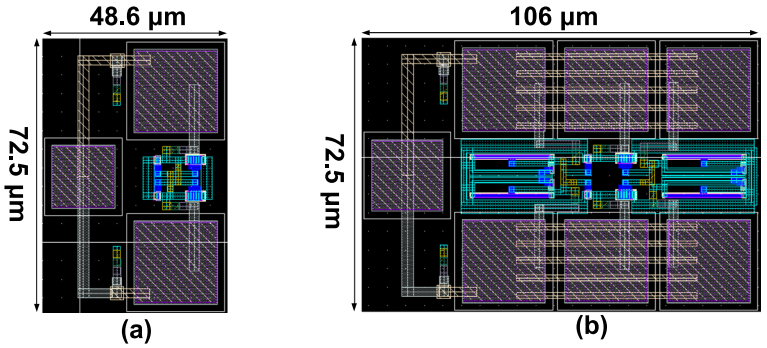


Fig. 13 Layout of **a** conventional and **b** proposed rectifiers and on-chip matching capacitor (C_{m2})

Table 1 Device values of the proposed rectifier and input impedance matching network

Parameter	Size	Parameter	Size
$M_{N1,2}$	1.76 µm/180 nm	R_L	100 kΩ
$M_{P1,2}$	5 × 1.76 µm/180 nm	C_{m1}	10.31 pF
D_{1-4}	220 nm/500 nm	C_{m2}	365 fF
D_{5-8}	220 nm/20 µm	L_{m1}	41 nH
C_L	0.5 pF	L_{m2}	41 nH

that the transistors are not shielded in this layout. Additionally, it is important to highlight that in the case of the rectifier-only design, the calculation of the net RF input power supplied to the rectifier can be ascertained using the subsequent equation.

$$P_{RF} = P_{Sig}\left[1 - |S_{11}|^2\right] \tag{5}$$

where P_{RF} signifies the net *RF* input power for the rectifier, P_{Sig} represents the *RF* power source from the signal generator, and S_{11} corresponds to the rectifier's input reflection coefficient [7]. Also, as a summary, Table 1 encapsulates the value of designed device components.

It is important to note that in evaluating differential rectifiers, only the results of the matching and rectifier circuit sections are taken into account, and the impact of the antenna and balun is excluded from consideration. This approach ensures fair comparisons, eliminating the influence of the balun and antenna (particularly the balun) on the results. In this paper, we present the results in both scenarios.

Figure 14a illustrates the S_{11} results versus the input frequency at − 19.5 dBm input power, and Fig. 14b demonstrates this result in terms of input power at 900 MHz input frequency. As shown in Fig. 14, this circuit exhibits an $S_{11} = -38$ dB at the desired frequency and input power. As explained in Sect. 2.2, the input impedance of the rectifier is influenced by factors such as frequency and input power. Considering that the rectifier exhibited its highest power conversion efficiency (PCE) around − 20 dBm input power, we developed a dedicated matching system aimed at achieving optimal alignment at this power level and a frequency of 900 MHz. Leveraging the proposed wide dynamic range CMOS differential rectifier and having a grasp of the expected input power, it becomes possible to fine-tune the matching circuit accordingly. This

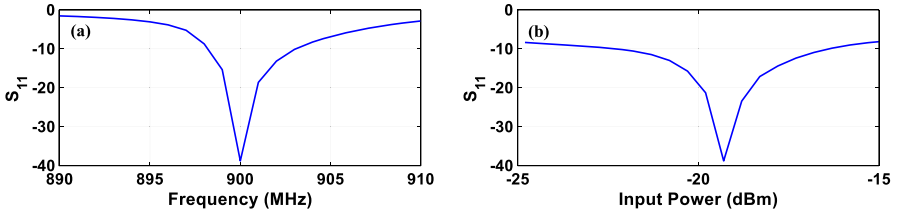


Fig. 14 S_{11} results with respect to **a** frequency at $P_{in} = -19.5$ dBm and **b** input power at $f = 900$ MHz

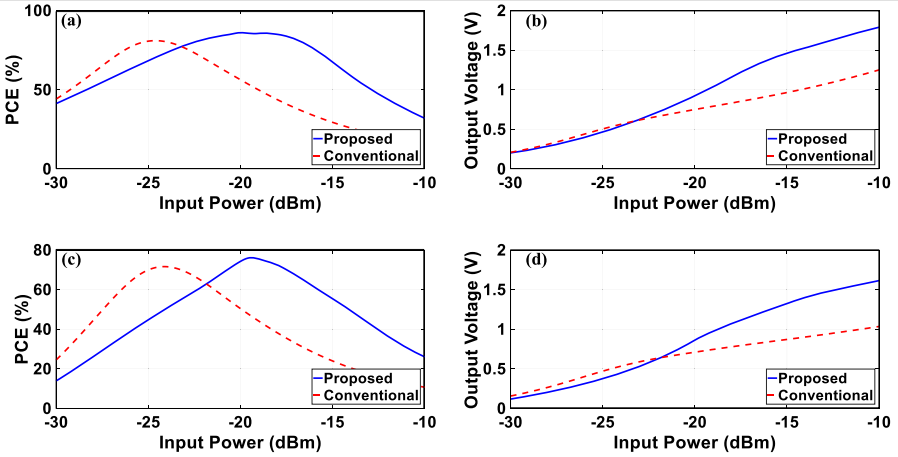


Fig. 15 The rectifier's **a** PCE and **b** the output voltage and the total system's **c** PCE and **d** the output voltage

adjustment enables the realization of the highest attainable output power. It is important to note that this study focuses on an IoT application, where the input power typically is around − 20 dBm.

Figure 15 shows the PCE and output voltage for the rectifier and total system in conventional and proposed structures. As depicted in Fig. 15a and b, the input power is changing from $P_{\text{in}} = -30$ dBm to $P_{\text{in}} = -10$ dBm. This leads to a corresponding output voltage range, varying from $V_{\text{DC}} = 0.2$ V to $V_{\text{DC}} = 1.79$ V. The PCE for the proposed rectifier is 86.03%, which offers an improvement of 5.03% compared to the conventional rectifier. According to Fig. 15a, the dynamic range of the proposed structure is 9.76 dB, which is 3.5 dB more than the conventional circuit. According to Fig. 15b, the rectifier sensitivity used in this paper equals − 19.3 dB, which shows an improvement of 5.01 dB compared to the conventional circuit. These improvements directly translate to increased energy extraction from the available input, enabling more efficient energy conversion and utilization. With higher PCE, a greater portion of the harvested energy can be effectively converted into usable power, enhancing the overall performance of energy harvesting devices. Additionally, the improved DR allows for better signal reception and adaptability to varying input conditions, ensuring reliable operation even in challenging scenarios. Therefore, these advancements contribute to the viability and effectiveness of energy harvesting technologies, particularly in applications where low input power is the norm.

To examine the robustness of the designed circuits, the sensitivity and PCE of both proposed rectifier and total system over process corners and temperature variations have been done and the results are illustrated in Fig. 16 and summarized in Table 2. According to Fig. 16 and Table 2, the results are very well matched and meet expectations. Therefore, the circuit is less sensitive to temperature changes and technology corner cases.

The main load of the circuit has a value of 100 kΩ. The reason for selecting this load is its suitability for IoT applications and radio wave identification systems. However, to demonstrate the versatility and superior performance of the proposed rectifier circuit

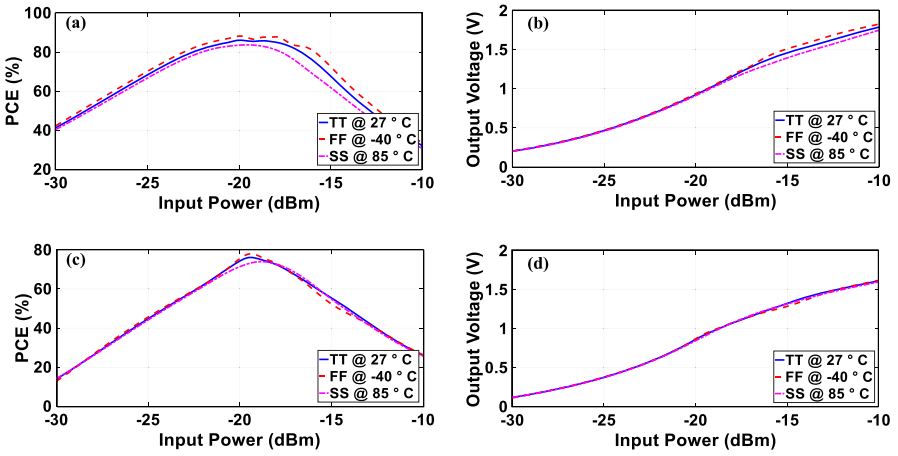


Fig. 16 The rectifier's **a** power PCE and **b** the output voltage and the total system's **c** PCE and **d** the output voltage in different process corner cases and temperature variations

Table 2 Simulation results at different process corner cases and temperature variations

Parameter	TT @ 27 °C	SS @ 85 °C	FF @ − 40 °C
Peak PCE (%)	86.03	83.66	88.14
Sensitivity (dBm)	− 19.32	− 19.22	− 19.39
DR (dB)	9.76	9.24	10.14

across various loads (different applications), we also analyze it with loads of 30 kΩ and 80 kΩ. The results of these simulations are observed in Fig. 17.

Tables 3 and 4 are provided to compare both the proposed rectifier and total RF energy harvesting system, including antenna and balun with several other previous works. The proposed structure has higher sensitivity, better PCE, and a wider dynamic range than previous works. Reference [13] has the maximum efficiency between the references, but with low sensitivity and dynamic range. Reference [6] shows high efficiency, and has good sensitivity, but the proposed structure has better parameters and has created a wider dynamic range. Diode (diode-connected transistors) network

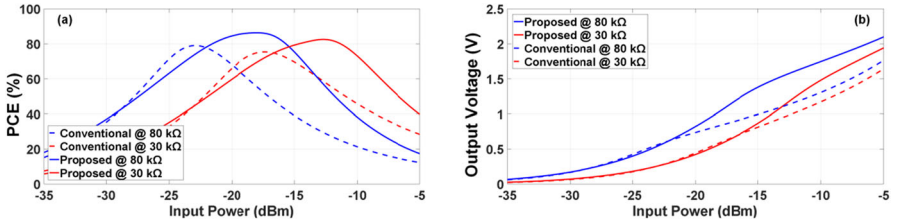


Fig. 17 The rectifier's **a** power PCE and **b** the output voltage with different loads

Table 3 Performance summary and comparison of the proposed rectifier with several previous similar works

Reference	Architecture	CMOS process (nm)	Freq. (MHz)	# of stages	Peak PCE (%)	Sensitivity (dBm)	DR (dB)	Area ($\times 10^3$ μm^2)	R_{Load} (kΩ)
Proposed rectifier*	Diode feedback and feedforward rectifier	180	900	1	86.03	− 19.32	9.76	7.69	100
Conventional rectifier*	Standard differential rectifier	180	900	1	81	− 14.29	6.3	3.52	100
JSSC'09 [13]	Standard differential rectifier	180	953	1	86.2**	− 13**	6**	13.44	100
MWCL'16 [21]	Adaptive rectifier	180	900	1	65	− 18	6.6	84.5	100
TCAS II'17 [22]	Self-biased	180	433	1	51.5	− 17	7.9	16.9	100
MTT'18 [2]	Double-sided	180	900	1	66	− 18.2	6.8**	8.8	100
TCAS II'21 [6]	Shared-capacitor coupling	130	900	3	83.7	− 19.2	6.7**	46.8	100
ELL'19 [12]*	Using thick-oxide transistors	180	900	2	75.2	− 17	5.6**	13.8	100
WPTC'17 [14]*	DC-boosted biasing	65	2450	2	59.6	− 17***	8.2**	89	29

*Post-layout simulation results
**Estimated from the figure

Table 4 Performance summary and comparison of the proposed RF energy harvesting system with several previous similar works

Reference	Architecture	CMOS process (nm)	Freq. (MHz)	# of stages	Peak PCE (%)	Sensitivity (dBm)	DR (dB)	R_{Load} (kΩ)
Proposed*	Diode feedback and feedforward rectifier	180	900	1	76.13	− 18.75	6.3	100
Conventional*	Standard differential rectifier	180	900	1	71.6	− 11	5.7	100
TCAS I'19 [25]	optimum compensation	130	896	4	43	− 20.5	–	1000
TCAS II'17 [18]	Dual path	65	900	5	36.5	− 17.7***	5.3**	147
ISCAS'18 [20]*	New self-compensated	130	915	10	42.8	− 30.5	–	500
IEEE Access'20 [11]	Reconfigurable stages	180	902	Rec	33	− 20.2****	8.5**	200
TCAS I'23 [28]	Main and auxiliary differential rectifier	65	900	6 + 7	42.8	− 20*****	–	100
JSSC'16 [1]	Reconfigurable Self-Startup	180	915	Rec.	25	− 14.8	–	1000
Sensors'22 [8]	Rectifier stacking, Charge pump	180	2400	3 × 3 + 6 CP	21.15	− 14.1	–	3.3

*Post-layout simulation results
**Estimated from the figure
***$R_{Load} = \infty$
****$R_{Load} = 1$ MΩ
*****$R_{Load} = 800$ kΩ

techniques have been used in [2] and [6]. Due to balun and antenna losses, the results of the entire system are slightly lower than the results of the rectifier and the matching network. Usually, systems with differential rectifiers are not systematically compared to other energy harvesting systems. However, in this paper, in addition to comparing the designed rectifier with similar works, we compare the total system with other systems. As shown in Table 4, in terms of PCE, it has achieved better results than all previous works. The sensitivity of the proposed circuit is less than [20, 25], and [11]. The reason is the high load of these references when calculating the sensitivity.

4 Conclusion

This paper introduces a rectifier structure that decreases the return current at high input power levels and enhances the forward current at low input power levels. The performance of diode-connected transistors, acting as feedback and feedforward paths, enhances the rectifier's PCE and DR. According to the detailed post-layout simulations in a 180 nm CMOS process, the proposed rectifier's PCE and DR are 86.03% and 9.76 dB, respectively, with a sensitivity of − 19.3 dBm at 900 MHz at 1 V output voltage across a 100 kΩ resistive load. Also, because of this improvement at the rectifier, the total system's results are 76.13% and 6.3 dB for PCE and DR with a sensitivity of − 18.75 dBm for the same condition with the rectifier.

Data availability Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Declarations

Conflict of interests The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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