SHORT PAPER

On the Boundaries of the Realization of Single Input Single Element-Controlled Universal Memelement Emulator

Kapil Bhardwaj[1] · Mayank Srivastava[1]

Abstract
The paper discusses in detail the inability of a circuit designer to design a single input single element-controlled universal memelement emulator. A Single input Single element-controlled universal memelement emulator would be such a configuration that can provide the realization of any of the three memelements (Memristor/Memcapacitor/Meminductor) by taking a circuit element as inductor (L), Capacitor (C) or Resistor (R) with the same input port. The analysis shows that no such circuit configuration can be built to realize such a highly flexible universal memelement emulator. It is found that by using such structures, only two ideal memelements can be realized at maximum. If these circuit structures are used to realize the remaining third memelement, then, the resulting element comes out to be a non-ideal memelement. Two circuit configurations to demonstrate this theory are also included for both charge-controlled and flux-controlled memelement emulation based on the approaches shown in this paper.

Keywords Memristor · Meminductor · Memcapacitor · Universal emulator

1 Introduction

The emulation circuits for memelements are attracting interest due to their use in nonlinear circuit memristive applications [4, 14, 20, 31]. As compared to the other two memelements, the memristor realization has been a well-established domain since the last decade. From the use of Op-Amp (Operational Amplifier) to the employment of OTAs (Operational Transconductance Amplifiers), the memristor emulators have

✉ Mayank Srivastava
   mayank2780@gmail.com

   Kapil Bhardwaj
   kapilec143@gmail.com

[1] Department of Electronics and Communication Engineering, National Institute of Technology Jamshedpur, Jamshedpur 831014, India

been built using several kinds of active elements so far [1, 3, 5, 12, 15, 19, 21, 22, 27, 32]. Also, some other kinds of circuit structures based on diode-bridge networks have been reported to emulate the memristor characteristics [13, 30]. Unlike the memristor which became popular, other memelements, memcapacitor and meminductor, are not well studied. There are some circuit implementations of these memelement emulators, which are reported in [2, 10, 17, 23–26, 28, 34, 35].

Apart from the memelement emulators that can realize only single memelement functions [1–3, 5, 10, 12, 13, 15, 17, 19, 21–28, 30, 32, 34, 35], the multi-(universal/dual) memelement emulators are also gaining importance among circuit theorists [6, 7, 9, 11, 29, 33, 36]. The aim of a circuit designer always remains the emulation of maximum numbers memelement functions using a single circuit configuration based on a minimum number of circuit resources possible. And also, flexibility is a very desirable feature (freedom to have all the desired emulated memelement functions by executing the least number of changes in the circuit). The universal memelement emulators present in the existing literature [33, 36] cannot be considered easily reconfigurable, as they require multiple changes in the circuit design to switch from one memelement function to another. However, it can be proven by simple circuit logic that the realization of such a highly flexible (which requires only a single change keeping the same input port) universal emulator is not a possibility. Only two of the three memelements can be realized at most keeping the same architecture (resulting in a very flexible dual memelement emulator), the realization of the third memelement requires a lot of alterations in the design of the circuit. In the existing literature, some dual memelement emulation circuits are available [6, 7, 9, 11, 29]. It is observed in these emulators that maintaining the same circuit design (except the change of one passive element) realization of only two memelements is possible; however, the third element comes out to be a non-ideal capacitor or inductor. The work first discusses the two approaches that can be followed to obtain the simplest design of a single input single element-controlled flux/charge dependent multi-memelement emulator. Then, the limitation of these circuit concepts is discussed in the realization of a single input single element-controlled universal memelement emulator. Further, validation of this argument is demonstrated through the OTA-CCII-based circuit structures following the discussed concepts.

2 Single Input Single Element-Controlled Multi-Memelement Emulators and Their Inability to Realize all Three Memelements

The use of linear functions of flux/charge/TIF (Time integral of Flux)/TIQ (Time integral of Charge) has been common among circuit designers to realize the corresponding memelement emulators. In almost every memelement emulators given previously [1–3, 5–7, 9–13, 15, 17, 19, 21–30, 32–36], the realizing memelement functions exhibit linear dependency on the time integral of the applied current/voltage/charge/flux signal, which has a relation in the time-domain as follows:

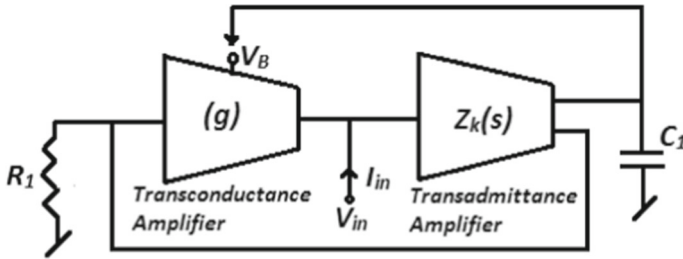$$y(t) = \left(a + b \int_0^t x(k)\, dk \right) x(t) \qquad (1)$$

Fig. 1 A simples realization approach for voltage-controlled memelement emulator using external multiplier-less configuration

where $x(t)$ and $y(t)$ represent the corresponding basic quantities of the memelements (which are voltage (v_{in}) and current (i_{in}) in the case of a memristor).

From Eq. (1), the memelement function becomes; $G_{M/memcap/memind} = \left(a + b \int_0^t x(k)dk\right)$, where **a** and **b** may be the coefficients depending upon the realization schemes.

Figure 1 shows possibly the simplest circuit structure to realize a voltage-controlled multi-memelement emulator with external multiplier-less architecture. This concept is based on a transconductance (with gain g) and a transadmittance amplifier (with a transfer function $Z_k(s)$) with two grounded passive elements. The second block (transadmittance amplifier) can be a type of filtering circuit, having a transfer function, Z_k that can be tuned to be; transconductive (g), transinductive (sg'') or transcapacitive $\left(\frac{g'}{s}\right)$.

Upon applying basic circuit principles, the i–v relation of the above-depicted circuit idea (in Fig. 1) is revealed as follows:

$$I_{in}(t) = \left(k + \frac{R_1}{C_1}\int_0^t Z_k V_{in}(k)dk\right) R_1 Z_k V_{in}(t) \tag{2}$$

The first term between the brackets denotes the transconductance of the first amplifier, biased by the voltage across C_1. The transient plot for Eq. (2) between I_{in} **(k)** and V_{in} **(k)** for the sinusoidal signal application is shown in Fig. 2.

By observing Figs. 1 and 2 and using Eq. (1), it can be deduced that by selecting the gain of the transadmittance amplifier as (g) and $\left(\frac{g'}{s}\right)$, the realization of memristor and meminductor can be achieved, respectively. If we select this amplifier gain as sg'' (transinductive), we can achieve the following kind of i–v relation:

$$i_{in}(t) = \left(k + \frac{R_1}{C_1}\int_0^t \left(\frac{dv_{in}(k)}{dk}\right)dk\right) R_1 \frac{dv_{in}(t)}{dt} \tag{3}$$

Therefore, in this case, Eq. (1) *cannot* realize the ideal memcapacitor function. Due to this, it can be concluded that no such circuit configuration can be designed, which can be used to realize all three voltage-controlled memelement functions by executing
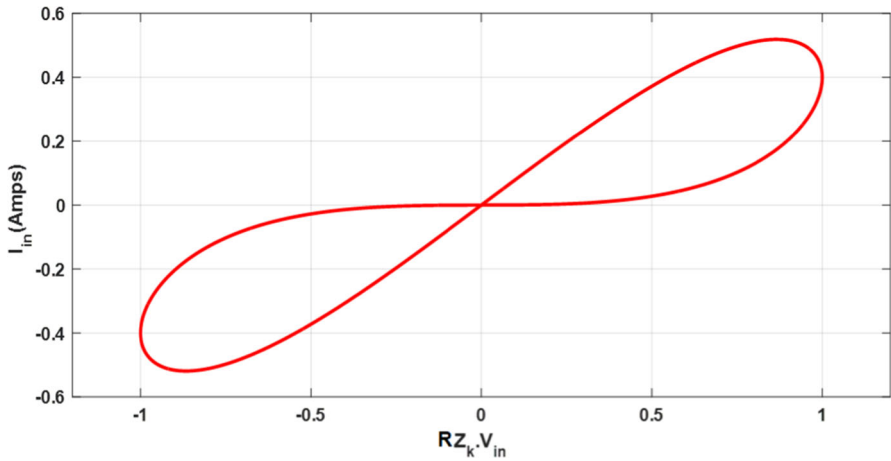
Fig. 2 Transient i–v response for Eq. (2) [between I_{in} and V_R (voltage across resistance R_1 in Fig. 1)] by employing Eq. (1), plotted for the memelements realized employing the approach depicted in Fig. 1

only a single change and maintaining the same input connections. Some existing universal emulators provide the realization of the three popular memelements, but they require the employment of three or more passive and active components (like those reported in [6, 7, 9, 11, 29]) and need multiple changes.

On comparing with the conventional capacitive relationship ($i = c\mathrm{d}v/\mathrm{d}t$), we can understand that Eq. (3) is representing the time-domain relationship of a nonlinear voltage-controlled capacitor.

Now, Fig. 3 depicts a simple realization concept that is single input single element-controlled architecture. However, it can be proved using similar logic that it cannot be used to realize all three memelements.

For this circuit configuration, the i-v relation is found as follows:

$$V_{in}(t) = \left(k + g_2 \frac{1}{C_1} \int_t^t Zi_{in}(k)\mathrm{d}k \right) R_1 Zi_{in}(t) \tag{4}$$
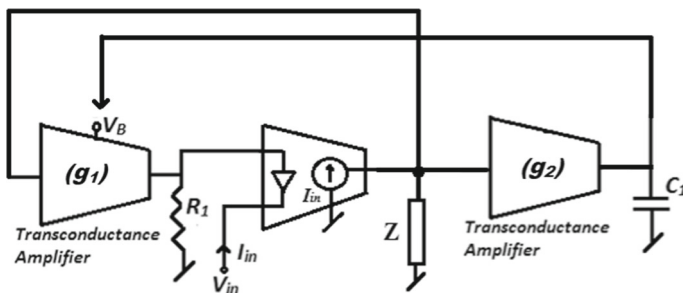

Fig. 3 A simplest realization approach of multi-memelement current-controlled memelement emulation using external multiplier-less configuration

Equation (4) suggests that selecting the impedance Z as R results in the realization of a memristor and taking it as the capacitance C provides the emulation of memcapacitor. Interestingly, the selection of the impedance Z as an inductor L does not provide the function of meminductor rather it realizes only the nonlinear inductor (current controlled).

Therefore, using the basic circuit structure of Fig. 3, we can only realize the current-controlled memristor and memcapacitor and hoping for the realization of a meminductor, the third element comes out to be a non-ideal inductor. So, even for the current-controlled elements, all three types of memelement functions cannot be realized employing such single input single element structures. At most, these compact architectures can only be used to realize two memelement functions. Nevertheless, the possibility can be explored to design such a true universal memelement emulator by using a very versatile block with several input/output ports (resulting in complex internal structures based on a large number of transistors). The realization of such a block and its use in the designing of a universal memelement emulator can be investigated in the future.

The discussed arguments in this section have been validated by implementing the above-mentioned circuit concepts (in Figs. 1 and 3) by using OTA and CCII-based configurations.

3 Implementations of the Multi-Memelement Emulators Using OTA and CCII

The employed OTA has a single current output (I_O) related to its voltage inputs by the relationship:

$$I_O = g_m(V_+ - V_-) \tag{5}$$

Here, g_m denotes the transconductance of OTA given by $g_m = k(V_B - V_{SS} - V_t)$, in which bias voltage is V_B, and V_{SS} is the power supply value, V_t is the transistors' threshold voltage value depending upon the technology, and k is the process parameter.

And the CCII is chosen with dual current outputs with port relationships given as follows:

$$V_X = V_Y, I_{Z+} = -I_{Z-} = I_X \quad \text{and} \quad I_Y = 0 \tag{6}$$

3.1 Flux-Controlled Single Input Single Element-Controlled Multi-Memelement Emulator

The designed proposed circuit configuration of the designed Flux-dependent multi-memelement emulator is depicted in Fig. 4. The circuit comprises one OTA along with CCII and three passive elements in the grounded state.

At the X port of the CCII, the connected impedance Z can be selected as: Resistor (R), Capacitor (C), and inductor (L), for the realization of the different element functions. It can be noticed from Fig. 4 that $I_{Z+} = I_X = \frac{V_X}{Z}$, $I_{Z-} = -I_X = -V_X/Z$,
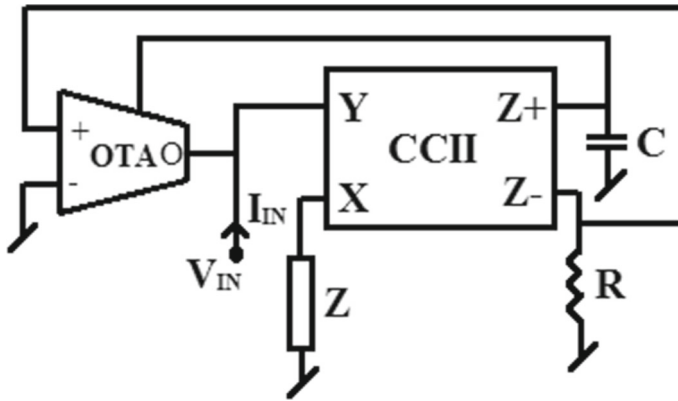
Fig. 4 Flux-controlled multi-memelement emulator using OTA and CCII [8]

where Z_X is the impedance present at the X terminal of the CCII. It suggests that $1/Z$ is acting like a transadmittance from port X to port Z. It is equivalent to the transadmittance amplifier, and the second stage of the circuit idea is depicted in Fig. 1.

By using Eqs. (5) and (6), the current I_{in} can be evaluated as follows:

$$I_{in} = k\left(\frac{1}{C}\int_0^t \frac{V_{in}}{Z}dt - V_t - V_{SS}\right)\frac{V_{in}}{Z}R \tag{7}$$

3.1.1 Case 1: Replacing Impedance Z with Resistance R_1

On putting $Z = R_1$, Eq. (7) is modified as follows:

$$I_{IN} = k\frac{R}{R_1}\left(\frac{1}{R_1C}\int_0^t V_{in}dt - V_{SS} - V_t\right)V_{in} \tag{8}$$

By using Eq. (8), it is clear that after connecting R_1, the circuit depicted in Fig. 4 emulates the behavior of a Flux-dependent memristor with memristance G_M equals to:

$$G_M = k\frac{R}{R_1}\left(\frac{1}{R_1C}\int_0^t V_{in}dt - V_{SS} - V_t\right) \tag{9}$$

The PSPICE simulations are performed to test the working of this circuit as a memristor emulator. The employed CMOS implementations of the used CCII and OTA are taken from the works reported in [16, 18]. The emulated memristor (realized using Eq. 8) using the designed emulator is simulated by selecting $R_1 = 8$ K, $C_1 = 0.036$ nF, and $R = 5$ K. Figure 5 demonstrates the memristor PHL curves for three operating frequencies, and it plotted between transient input voltage and current. According to the well-known memristor fingerprints, the memristor i–v contour should
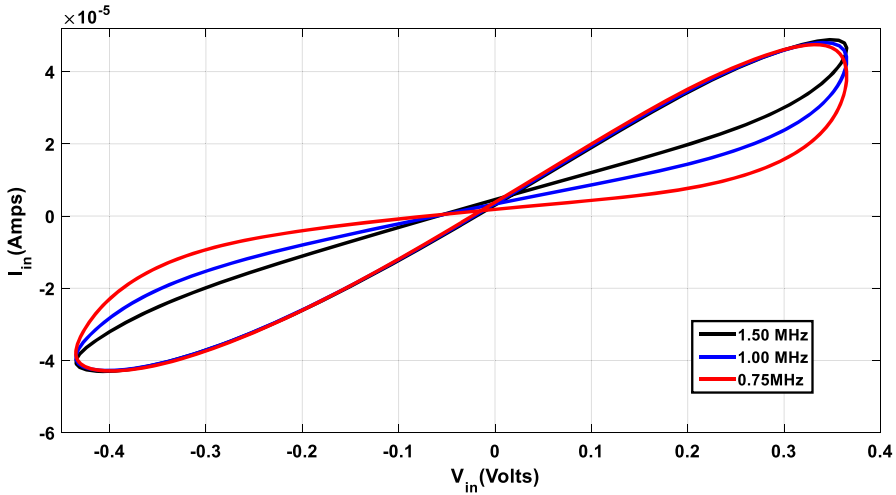
Fig. 5 Plotted PHL curves of the emulated memristive behavior

intersect itself at the origin, and its enclosed area should diminish upon raising the operating frequency of the applied signal.

3.1.2 Case 2: Replacing Impedance *Z* by Inductor *L*₁

On putting $Z = sL$, Eq. (7) can be written as follows:

$$I_{in} = k\frac{R}{L_1}\left(\frac{1}{L_1 C}\int_0^t \int_0^{t'} V_{in} \mathrm{d}k\mathrm{d}t' - V_{SS} - V_t\right)\int_0^t V_{in}\mathrm{d}t \qquad (10)$$

Equation (10) suggests the realization of a flux-controlled meminductor if an inductor is connected at the *X* port of the CCII. The realized inverse meminductance $L_M{}^{-1}$ can be found as follows:

$$L_M^{-1} = k\frac{R}{L_1}\left(\frac{1}{L_1 C}\int_0^t \int_0^{t'} V_{in}\mathrm{d}k\mathrm{d}t' - V_{SS} - V_t\right) \qquad (11)$$

To simulate the emulated meminductor, the simulation parameters are selected as: $R = 2\,\mathrm{K}$, $C = 0.075\,\mathrm{nF}$, and $L_1 = 0.01\,\mathrm{mH}$. The simulation results illustrated in Fig. 6 exhibit the ϕ–i (*flux-current*) plots of the emulated flux-controlled meminductor traced at three frequencies.

3.1.3 Case 3: Replacing Impedance *Z* with Capacitor *C*₁

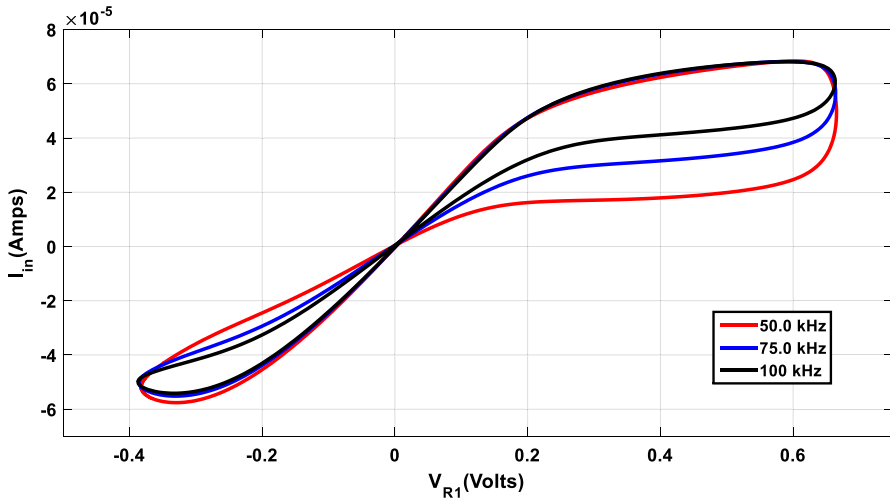In this case, the Eq. (7) should be written as follows:

Fig. 6 PHL plots of the realized meminductor (V_{R1} is proportional to $(-\phi)$, and the x-axis is chosen as-V_{R1}))

$$I_{\text{in}} = kRC_1\left(\frac{C_1}{C}(V_{\text{in}}) - V_{\text{SS}} - V_{\text{t}}\right)\frac{\mathrm{d}}{\mathrm{d}t}(V_{\text{in}}) \tag{12}$$

On comparing Eq. (12) with the commonly used capacitive current relation $I_{\text{in}} = C\mathrm{d}v/\mathrm{d}t$, the emulated nonlinear capacitance C_M by the circuit depicted in Fig. 4 is found as follows:

$$C_{\text{M}} = kRC_1\left(\frac{C_1}{C}(V_{\text{in}}) - V_{\text{SS}} - V_{\text{t}}\right) \tag{13}$$

Similarly, the realized nonlinear capacitance is tested by applying a sinusoidal signal with amplitude $V_{\text{P}} = 0.01$ V with operating parameters chosen as: $C = 0.01$ nF, $C_1 = 0.075$ nF, and $R = 5$ K. Equation (13) suggests that the characteristics of this nonlinear capacitor must be traced between I_{in} and $\mathrm{d}v/\mathrm{d}t$. For a sinusoidal input with a voltage signal as: $v = v_{\text{p}}\sin 2\pi F_{\text{in}}t$, the x-axis variation will be controlled by $\mathrm{d}v/\mathrm{d}t = 2\pi F_{\text{in}}v_{\text{p}}\sin 2\pi F_{\text{in}}t$. It clearly suggests that span of the PHL curve along the x-axis should depend upon the input signal frequency. It can also be observed in the plots demonstrated in Fig. 7. The nonlinear capacitors have also been called dual of memcapacitor.

3.2 Charge-Controlled Single Input Single Element-Controlled Memelement Emulator

The circuit described in Fig. 8 is the implementation of the circuit block diagram discussed in Fig. 3 for current-controlled multi-memelement emulators. The depicted schematic consists of two OTAs and a CCII along with three grounded passive elements.
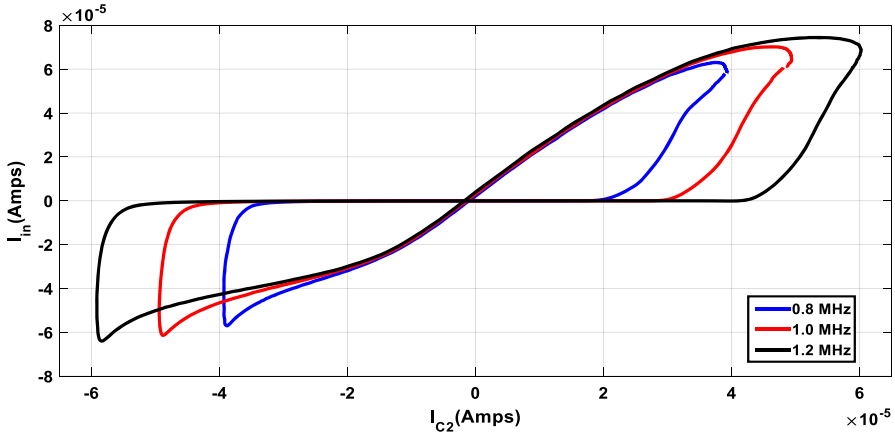
Fig. 7 Transient characteristics of the realized nonlinear capacitor traced in the $(i\text{--}dv/dt)$ plane (I_{C1} is directly proportional to the dv/dt)
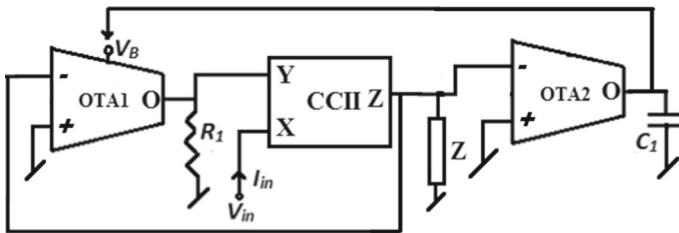

Fig. 8 Charge-controlled multi-memelement emulator using OTA and CCII

On performing circuital analysis by using Eqs. (4) and (5), the input current I_{in} is obtained as follows:

$$V_{\text{in}} = k\left(g_{\text{m2}}\frac{Z}{C_1}\int_0^t I_{\text{in}}dt - V_{\text{th}} - V_{\text{SS}}\right)I_{\text{in}}ZR_1 \qquad (14)$$

In Eq. (14), the first product term is the transconductance gain of OTA1, while g_{m2} represents the transconductance amplifier of OTA2.

Now, on selecting the different types of impedance Z, three different cases can be studied.

3.2.1 Case 1: When Z is Selected as Resistance R

In this case, Eq. (14) can be modified as follows:

$$V_{\text{in}} = k\left(g_{\text{m2}}\frac{R}{C_1}\int_0^t I_{\text{in}}dt' - V_{\text{th}} - V_{\text{SS}}\right)I_{\text{in}}RR_1 \qquad (15)$$

It can be deduced from Eq. (15) that by choosing Z as resistance R, the circuit of Fig. 8 realizes the function of a charge-controlled memristor.

3.2.2 Case 2: When Z is Selected as Capacitance C

For the use of the capacitance, the i–v relationship of the circuit can be computed from Eq. (14) as follows:

$$V_{\text{in}} = k \left(g_{\text{m2}} \frac{1}{CC_1} \int_0^t \int_0^{t'} I_{\text{in}} \mathrm{d}k \mathrm{d}t' - V_{\text{th}} - V_{\text{SS}} \right) \frac{1}{C_1} \int_0^t I_{\text{in}} \mathrm{d}t' R_1 \qquad (16)$$

On comparing Eq. (16) with the standard charge-controlled capacitance equation, we can understand that Eq. (16) is realizing the function of a charge-controlled memcapacitor.

3.2.3 Case 3: When Z is Selected as Inductance L

In this case, the input i–v relationship of the designed circuit is obtained as follows:

$$V_{\text{in}} = k \left(g_{\text{m2}} \frac{L}{C_1} I_{\text{in}} - V_{\text{th}} - V_{\text{SS}} \right) Z R_1 L \frac{\mathrm{d}}{\mathrm{d}t} (I_{\text{in}}) \qquad (17)$$

Equation (17) suggests the realization of only a nonlinear current-controlled inductor. Therefore, selecting the impedance Z as inductance L does not provide the emulation of a charge-controlled meminductor.

Therefore, the circuit concept of Fig. 3 is unable to realize all three memelements with a single input single element-controlled structure.

4 Conclusion

The paper discusses that a single input single element-controlled Flux-dependent multi-memelement emulator provides the realization of only the ideal memristor and ideal meminductor, and the other case results in a nonlinear voltage-controlled capacitor. Similarly, in the case of the current-controlled emulator, the ideal memristor and memcapacitor are realized but the third one is obtained as a nonlinear inductor. There is no possibility to modify these circuit configurations by executing any change in the emulator circuits into a perfect universal memelement emulator without losing the various advantages of the emulator related to flexibility. Therefore, it is proved in this article that such universal memelement emulators cannot be designed whose behavior can be switched only by executing a single change in the circuit configuration.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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