Circuits, Systems, and Signal Processing (2023) 42:5108–5120
https://doi.org/10.1007/s00034-023-02375-6

An Energy-efficient and High-speed Dynamic Comparator for Low-noise Applications

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Received: 27 December 2022 / Revised: 28 March 2023 / Accepted: 29 March 2023 /
Published online: 25 April 2023

Abstract

An energy-efficient, low-noise, and high-speed dynamic comparator is proposed in this work. The comparator uses two pre-amplifiers to have a two-stage operation for reduced kickback noise. It also incorporates the adaptive current reuse (ACR) technique for reduced latency and high-speed operation. The proposed comparator is designed and simulated in a 65-nm UMC CMOS process using a 1.2-V power supply. The performance of the design is verified using post-layout simulation and also through Monte Carlo simulations. The resultant offset standard deviation of 8 mV is observed, which is 3 times less compared to the conventional design. The maximum operating frequency of the comparator is 1 GHz. The worst-case energy consumption is 67 fJ with an average latency of 70 ps. The kickback noise of 5.5 mV is observed for the entire working range, which is almost 10 times less compared to the conventional dynamic comparator at 500 MHz clock frequency.

Keywords Dynamic comparator · ACR technique · Energy efficient · Low noise

1 Introduction

The advancements in IoT technology have increased the requirements of the number of sensors, wherein each sensor requires the corresponding high-precision, high-speed, low-power, and low-noise readout circuit. In recent times, the focus of IoT-based systems is towards device portability, which requires the readout circuits to be designed with low power for improved battery life. The other major challenge being faced by IoT

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systems is the latency introduced by different sensors, which varies with temperature and voltage. Therefore, it becomes absolutely necessary to reduce the latency up to the tolerable limit.

Analog-to-digital converter (ADC) is the key component of all the readout circuits being used in application areas like communication receivers, CMOS image sensors, health care, and others. ADC converts the analogue output of sensors to digital form for further processing. Among various possible data converters, successive-approximation register (SAR) ADC is popular for low power as it requires a minimal number of analogue elements compared to other ADCs. SAR ADC inherently consists of a comparator, SAR register, and a digital-to-analogue converter (DAC). The power of SAR ADC is limited by the comparators.

In general, dynamic comparators are preferred over static comparators for high-speed and high-resolution applications. In the literature, various techniques to increase the speed and to reduce power consumption are reported. In the comparator design reported in [18], high speed is achieved by adding parallel paths to the output node. The two-stage dynamic comparator presented in [10] uses a pre-defined clocking pattern to reduce power consumption. The high-speed comparator with a transconductance-enhanced latching stage is reported in [19]. The latching stage uses separated gate-biasing cross-coupled transistors instead of a standard cross-coupled inverter structure. In [16], a current recycling approach is used for lower energy and high-speed applications. The comparator presented in [9] uses the concept of adaptive current-biasing technique to increase the speed of the comparator. In [15], high speed is achieved by directly connecting the pre-amplifier output to the regenerative latch, which reduces the effective capacitive load. In [5], high-speed and low-power consumption in a double-tail comparator are achieved by using a charge-steering approach. In [22], A comparator with a wide input range is reported by using a variable current source. The work reported in [8] implements a fully differential double-tail structure to improve the dynamic range. A wide input range comparator for LVDS receiver is presented in [12]. Moreover, [3, 4, 11] techniques are also reported to increase the energy efficiency of the dynamic comparators. In [6, 21] VCO-based comparators are reported, whereas in [13] inverter-based pre-amplifier comparator is proposed. In [2], dynamic bias pre-amplifier in which the nodes are partially discharged to save energy consumption at a cost of higher kickback noise. All the above-discussed techniques suffer from high kickback noise, which becomes more prominent at high frequency and scaled technology nodes.

The kickback noise is introduced due to coupling of large voltage variations or perturbations at the regenerative nodes through parasitic capacitances, to the comparator input, due to nonzero output impedance of the preceding circuit. In [14], kickback noise is reduced by providing a pre-amplifier before the latching stage; however, the technique is less effective during high-frequency operation. In [7], a neutralization technique with few sampling switches is used to reduce the kickback noise at the cost of speed and area. In [20], binary-weighted gate capacitance is used to reduce the kickback noise, which is very complex to design and also reduces the speed. In [23], three stages are used to enlarge the gain of the pre-amplifier, and in [17], two techniques are proposed and compared to reduce the kickback noise at a low frequency of operation. Moreover, a double-tail technique is also reported in [1] to mitigate the

kickback noise at low-power consumption. In all the above-discussed techniques, the observed values of kickback noise are large, which affects the comparator decision. Hence, it is necessary to either reduce the amplitude of noise or to reduce the transient duration of kickback noise in order to improve the design accuracy and resolution.

In this work, a low-latency, low-noise, and energy-efficient comparator are proposed. The comparator consists of three stages, wherein the first two stages are used to reduce the effect of kickback noise. Further, an adaptive current recycling (ACR) technique through a *P*-type pre-amplifier is used to provide additional strength to PMOS pairs of the regenerative latch. Both the conventional and proposed comparator are designed and simulated in a 65-nm CMOS process using a 1.2-V power supply at 500 MHz operating frequency. The rest of the paper is organized as follows: section II discusses the proposed comparator. Section III presents the simulation results, and also compares the performance of the proposed comparator with state-of-the-art, and section IV discusses input-referred noise. The conclusion and future scope of the work are discussed in section IV.

2 Proposed Comparator

A comparator circuit mainly consists of a pre-amplifier and a regenerative latch. As an example, a conventional comparator with a pre-amplifier formed by transistors MN_0–MN_2, MP_0–MP_1, and a regenerative latch formed by transistors MP_2–MP_6, MN_3–MN_6 is shown in Fig. 1. The input voltage is applied to the transistors MN_0–MN_1, and the output of preamplifier ($V_{c\ \mathrm{outn}}+$, $V_{c\ \mathrm{outn}}-$) is directly coupled to the input of the latch through transistors MP_2–MP_3. During the rising edge of *CLK*, output nodes of the pre-amplifier are reset to *V DD,* and the output nodes of latch ($V_{c\ \mathrm{outn}}+$, $V_{c\ \mathrm{outn}}$)

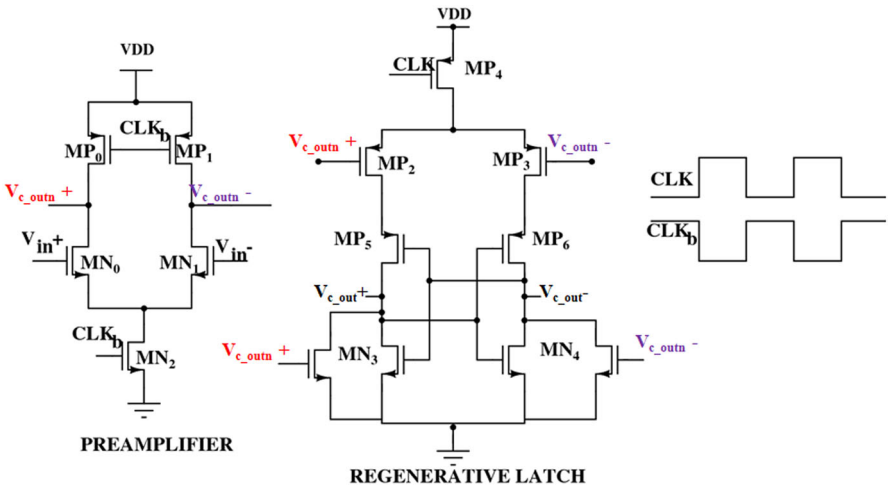

Fig. 1 Conventional dynamic comparator with timing diagram. The identical colour indicates the interconnected nodes

are reset to *GND*. During the falling edge of *CLK* or in the decision-making phase, the parasitic capacitance at the output nodes of pre-amplifier starts discharging at a different rate, which is sensed by the latch through transistors MP_2–MP_3. The positive feedback formed by MP_5–MP_6, MN_3–MN_4 results in high-voltage swing. Compared to the conventional design, the proposed dynamic comparator core consists of N-type pre-amplifier (PA1), *P*-type pre-amplifier (PA2), regenerative latch (RL), and an adaptive current recycling (ACR) technique (highlighted in the grey shade) as shown in Fig. 2. In addition to conventional design, the PA2 is formed by transistors MN_3–MN_4 and MP_6–$MP_{8,}$ whereas MP_2–MP_5 and MP_9–MP_{12} used to implement the ACR technique. The W/L ratio of all the devices are listed in the Table 1.

The operation of the proposed dynamic comparator is explained in two phases: the reset phase and the decision-making/regenerative phase. During the rising edge of *CLK*

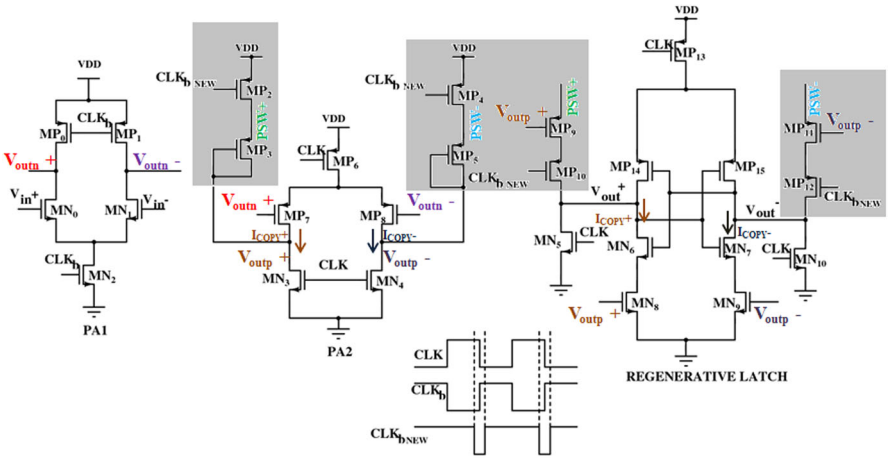

Fig. 2 Proposed dynamic comparator with the timing diagram. The identical colour indicates the respective interconnected node

Table 1 Aspect ratio of devices

Device	Aspect ratio
MN_0–MN_1	$\frac{2\mu}{60n}$
MN_2–MN_{10}	$\frac{1\mu}{60n}$
MP_0–MP_6	$\frac{1\mu}{60n}$
MP_7–MP_8	$\frac{2\mu}{60n}$
MP_9–MP_{15}	$\frac{1\mu}{60n}$

or falling edge of CLK_b, outputs of PA1 ($V_{\text{outn+}}$,$V_{\text{outn}-}$) and PA2 ($V_{\text{outp+}}$, $V_{\text{outp}-}$) are reset to *V DD* and *GND*, respectively. In the same phase, the regenerative nodes of RL ($V_{\text{out}}+$, $V_{\text{out}}-$) are reset to *GND* using MN_5 and MN_{10} by discharging any unwanted accumulated charge. During the falling edge or in the decision-making phase, the parasitic capacitance on the output nodes of the PA1 start discharging with different rates through the tail transistors $MN_{2,}$ which is determined by appliedinput voltage ($V_{\text{in}}+$, $V_{\text{in}}-$). The outputs of PA1 are fed to the input of PA2 and the instance when ($V_{\text{outn+}}$, $V_{\text{outn}-}$) discharge to the minimum threshold requirement of MP_7/MP_8, the PA2 turns on and output nodes of PA2 ($V_{\text{outp+}}$, V_{outp-}) start charging towards *VDD* with a different rate. The difference in the charging rate of parasitic capacitance at the output node of PA2 is sensed by the input transistors MN_8–MN_9 of RL. The sensed difference in voltage is amplified by the positive feedback of RL formed by transistors MN_6–MN_7 and MP_{14}–MP_{15} to achieve rail-to-rail voltage swing. One of the major advantages of using two pre-amplifiers is to increase the effective parasitic capacitances between the regenerative nodes and pre-amplifier inputs to suppress the kickback noise. It can be seen from the circuit operation that the decision by the latch is being made during the later part of CLK_b (edge) when the second preamplifier is turned ON, which reduces the overall kickback noise of the comparator. The increase in coupling capacitance between the output nodes ($V_{\text{out}}+$, V_{out}), and the input of comparator ($V_{\text{in}}+$, V_{in}) affects the comparator speed. To compensate for the degradation of speed, an adaptive current recycle technique is implemented in this work. There are three control signals: *CLK* and CLK_b are complementary and $CLK_{b\text{NEW}}$ is synchronized with the edges of the *CLK* with a duty cycle of 90% with respect to *CLK* as shown in the Fig. 2 used to implement the technique.

2.1 ACR Technique

In order to match the driving strength of PMOS devices of RL with NMOS devices, the proposed comparator uses the ACR technique highlighted in Fig. 2 with grey colour. In the ACR technique, the current from the PA2 is copied and reused in the regenerative nodes of RL during the falling edge of CLK_b for a faster decision compared to the conventional comparator. To copy the current, two *P*-type dynamic current mirrors are implemented to maintain the same source potential, which is labelled as *PSW+, PSW*− using transistor MP_3–MP_9 and MP_5–MP_{11}, respectively, as shown in Fig. 2. Moreover, four switches labelled as MP_2–MP_4, and MP_{10}–MP_{12} are used to synchronize the operation in the decision-making phase only, which are controlled by the signal CLK_{bNEW}. In the decision-making phase, the parasitic capacitance at the output nodes of PA2 ($V_{\text{outp+}}$, $V_{\text{outp}-}$) is charged towards *V DD* at a different rate, wherein the rate of charge of capacitors depends on the applied input difference. The resulting current flowing through these capacitances is ($I_{\text{copy}}+$), (I_{copy}), and acts as a current source for both the current mirrors. This current is reused in the RL by applying it to the drain terminal of transistors MP_{14}, MP_{15} by the switches MP_{10}, MP_{12}. Simulations are performed to find out the region where the transistors are in saturation region for the entire range of the comparator, and based on the observation, the duty cycle of

the control signal $CLK_{b\mathrm{NEW}}$ is decided, which operates all four switches, ensuring the current reuse.

3 Simulation Results and Analysis

The conventional as well as the proposed comparator is designed and simulated in 65 nm CMOS process using 1.2-V power supply, which is shown in Figs. 1 and 2. Both the comparator operates at a clock frequency of 500 MHz, and the maximum operating frequency of 1 GHz can be achieved. The layout of the proposed comparator is shown in Fig. 3, and it occupies an area of 20 µm 8 µm. To check the robustness of the proposed comparator, different post-layout simulations are performed including transient, Monte Carlo, and corner analysis as discussed in the below subsections.

3.1 Transient Analysis

The transient analysis of the comparator is shown in Fig. 4, wherein a ramp signal varying in the input range of 500 mV to 1.2 V and step size of 1 mV, is applied to the one input, say $V_{\mathrm{in}-}$ of the comparator and a fixed DC signal of 801 mV is applied to the other input, $V_{\mathrm{in}+}$. The plot is shown with a double Y-axis, wherein the output signals ($V_{\mathrm{out}+}$, $V_{\mathrm{out}-}$) and CLK_b are plotted with respect to the left Y-axis, and

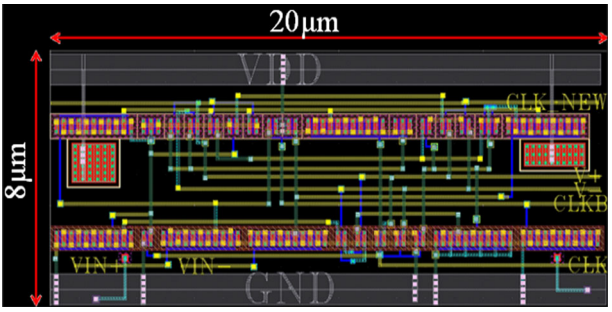

Fig. 3 Layout of the proposed comparator

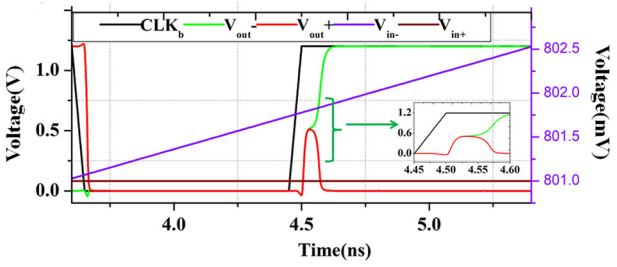

Fig. 4 Transient response of the proposed comparator

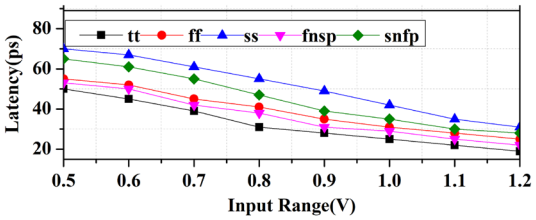

Fig. 5 Post-layout simulations representing latency for entire input voltage at various process corners

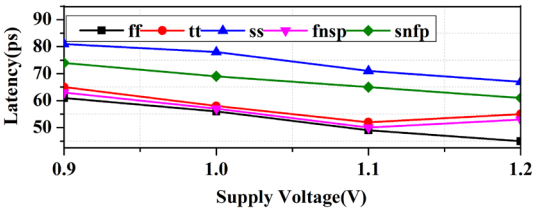

Fig. 6 Post-layout simulations representing variations in latency at different supply voltages plotted for all the process corners

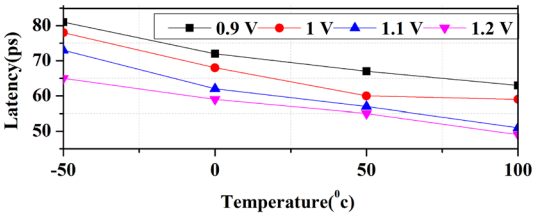

Fig. 7 Post-layout simulations representing variations in latency with respect to temperature for different supply voltages

the input signals (V_{in+}, V_{in-}) are plotted with respect to right Y-axis. The switching of comparator output can be shown in Fig. 4. The region representing comparator switching is zoomed in and shown as an inset graph. The switching in output voltages is observed at 0.802 V in the duration of 4.52 ns and 4.55 ns. The proposed comparator, therefore, has a resolution of 1 mV and latency of 30 ps.

3.2 Effect of Process Corners, Temperature, and Supply Voltage on Comparator Latency

The variation in comparator latency as a function of different corners including process, supply voltage, and temperature is analyzed to check the design's robustness. It is observed from Fig. 5 that for the entire input range, the latency of the proposed comparator for different process corners is within 70 ps. It is noted that the maximum variation in the latency is observed in the slowN and slowP (SS) corner as the threshold voltage of the devices is increased. Similarly, the effect of variations in supply voltage on latency for different process corners is observed as shown in Fig 6. It is observed that the worst-case latency is 81 ps below 1 V power supply at SS corner. The latency is decreased with an increase in the input voltage range due to an increase in the driving strength of the device. Further, the effect of varying temperature at different supply voltages on latency is analyzed in Fig. 7 and the latency of the comparator is varied

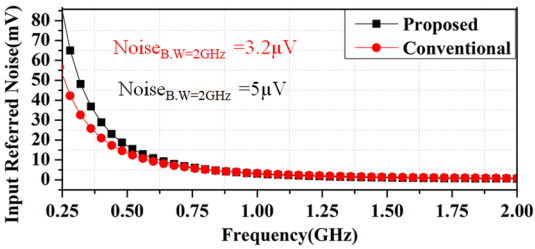

Fig. 8 The input-referred noise plotted with respect to frequency for the conventional and proposed design

from -5% to 12% with respect to the room temperature. All these simulations are performed for a fixed test bench wherein Vin− is applied with a ramp signal covering the comparator input range and other input is fixed at 600 mV.

3.3 Input-Referred Noise

The input-referred noise of the comparator is a summation of flicker noise and thermal noise introduced due to device components. Flicker noise is mainly dominated at low frequencies, whereas thermal noise is introduced due to change in the operating region of the devices. To estimate the total input-referred noise, noise analysis is performed both for conventional and proposed comparator. The observed noise over a bandwidth of 2 GHz for the conventional comparator is found to be 3.2 μV, whereas, for the proposed design, it is 5 μV as shown in Fig. 8.

3.4 Kickback Noise Analysis

The equivalent model for evaluating kickback noise is shown in Fig. 9, wherein the Thevenin equivalent of the preceding circuit is modelled with an output resistance of 1 $k\Omega$. The input signal with a difference of 1 mV(ΔV_{in}) is applied and the variations in the regenerating nodes coupled back to the comparator input are observed. In Fig. 10, the input signals are plotted with respect to the left y-axis (green colour), and the clock, as well as output signals, are plotted with respect to the right y-axis (purple colour). For better visualization, an inset representing the reduced effect of kickback noise at the comparator inputs is also shown. It is observed that when the CLK_b is making a transition from low to high state, at the first half of the edge, the effect of kickback noise is prominent on the input signal $V_{\text{in}}+$ and V_{in} with a maximum error of 40 mV. However, during this period, latch is still in *off* condition as output of the

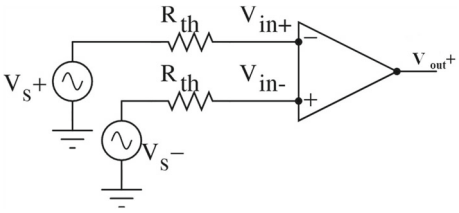

Fig. 9 Thevenin equivalent model for evaluation of kickback noise

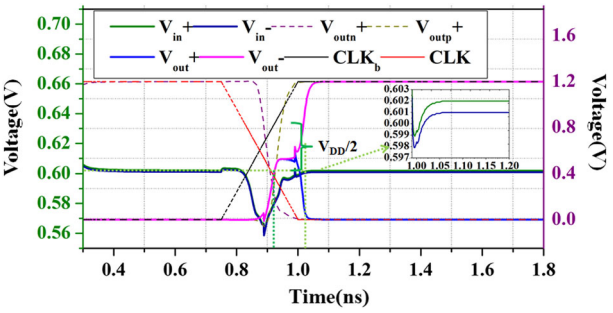

Fig. 10 Transient simulation where the variations in input voltages are plotted during the clock edges

second stage ($V_{\text{outp+}}$, $V_{\text{outp−}}$) is still at ground potential making MN_8–MN_9 in cutoff state. When the rate of discharge with respect to the input difference of the first stage ($V_{\text{outn+}}$, $V_{\text{outn−}}$) is enough to maintain the minimum threshold voltage requirements of the second stage, the outputs of PA2 ($V_{\text{outp+}}$, $V_{\text{outp−}}$) start charging at a different rate compared to the outputs of the first stage. As the RL becomes active based on the signals received from PA2, the additional delay introduced due to PA2 helped in reducing the effect of kickback noise from the regenerative nodes to the PA1 or comparator input. It can also be shown in Fig. 10 that the RL turns *ON* during the latter half of the falling edge of *CLK* and at the same time the differential inputs $V_{\text{in}}+$ and V_{in} are less affected by the kickback noise, and the peak error is reduced from 40 mV to 3 mV (with pre-layout simulations). The inset is also added to show a reduction in kickback noise with more clarity. In Fig. 11, kickback noise is evaluated considering post-layout simulations for the entire input range of the comparator. The worst-case noise of 5.5 mV is observed at 1.2 V power supply for post-layout design. However, the same analysis when performed for conventional comparator results in a worst-case noise of 55 mV. Therefore, the proposed design reduces the worst-case kickback noise by a factor of 10 compared to the conventionally designed comparator. As kickback noise is a frequency-dependent parameter, the noise is plotted for a different set of frequencies as shown in Fig. 12. It is known that the kickback noise increases with frequency, an increment in noise by approximately 5 times is observed for the wide input frequency range. However, the observed kickback noise is low compared to the comparators designed for 500 MHz–1 GHz operating frequency range [16, 18] due to the two-stage operation of pre-amplifiers.

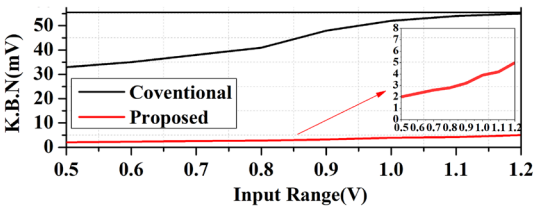

Fig. 11 Post-layout simulations of kickback noise with respect to the entire input range for conventional and proposed comparator for 1 mV differential input

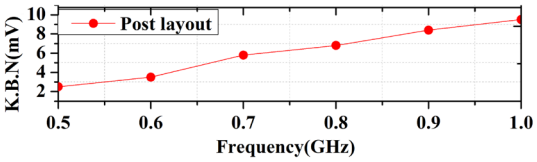

Fig. 12 Kickback noise with respect to varying frequency for 1 mV differential input

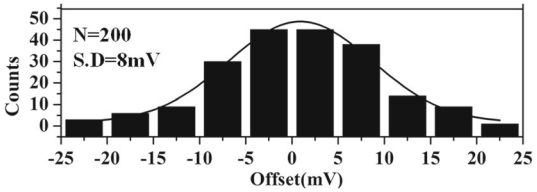

Fig. 13 Monte Carlo simulation of the proposed comparator for 200 samples post layout when V_{in+} is at 600 mV DC, and V_{in-} is ramp signal with a step size of 1 mV

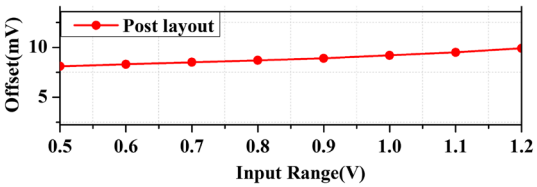

Fig. 14 Offset voltage of proposed comparator with respect to entire input range plotted for 200 Monte Carlo runs

3.5 Monte Carlo Analysis

The Monte-Carlo simulations are performed to analyze the effect of process and device mismatch in the proposed comparator. The simulations are performed for 200 samples keeping one input signal fixed to 600 mV and the other input is a ramp signal. The histogram shown in Fig. 13 represents the offset voltage of 8 mV. Further, the variations in offset for the entire working range of the comparator are also observed and the results are plotted in Fig. 14. It is seen that offset voltage increases with an increase in input voltage and worst case offset is 10 mV for an input voltage of 1.2 V.

As discussed earlier, the proposed comparator implements an additional ACR technique for high speed. Therefore, it becomes apparent to estimate total energy consumed by the proposed comparator. The total energy consumed by the comparator for different operating frequencies is evaluated and plotted in Fig. 15. It can be seen that at the operating frequency of 500 MHz, the energy consumed by the comparator is 67 fJ, which gets reduced to 30 fJ at 1 GHz operating frequency.

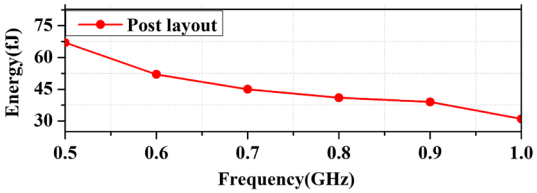

Fig. 15 The energy of the proposed comparator at different *CLK* frequencies for post-layout design of proposed comparator

Table 2 Performance comparison

Parameters	[18] [2021]	[4] [2020]	[3] [2017]	[2] [2018]	[23] [2021]	[1] [2014]	Conv	Prop
Technology [nm]	65	65	65	65	130	180	65	**65**
Supply [V]	1	1		1.2	1.2	0.8	1.2	**1.2**
Offset [mV]	2.05	-	6.2	–	–	7.8	24	**8**
Input range [V]	0.4–1	–	0.5-0.8	0.45-0.8	–	1	0.7	**0.7**
Energy [pJ]	0.108	0.192	0.03	0.034	0.215	0.24	0.034	**0.067**
Frequency [MHz]	3000	25	25	25	–	2400	500	**500**
Latency [ns]	0.167	–		–	0.211	0.294	0.5	**0.07**
Resolution [mV]	2	5		100	1	1	1	**1**
Area [μm^2]	603	1025	125	125	216	392	125	**160**
Kickback Noise [mV]	190	–	–	–	19.78	13	55	**5.5**

*Conv. and Prop. represents Conventional and proposed design parameters

The performance of the proposed comparator is compared with the state-of-the-art as shown in Table 2. Compared to [17], the proposed design has almost 1.5 times less kickback noise and energy consumption per conversion cycle compared to [7]. On comparing with the work mentioning the similar technology node of 65 nm [18], it is observed that the proposed design reduces the kickback noise by 35 times and energy by 1.2 times making the proposed comparator suitable for low noise and energy-efficient applications.

4 Conclusion and Future Scope

An energy-efficient, low-noise, and high-speed dynamic comparator is presented in this paper. The proposed comparator uses two pre-amplifiers having N-type and P-type input pairs for the two-stage operation to reduce the effect of kickback noise. It further incorporates an adaptive current reuse technique to increase the driving strength of the pull-up network of the regenerative latch, which ensures low latency for the entire working range. The comparator is designed in UMC 65 nm CMOS technology using a 1.2-V power supply. The performance of the comparator is observed for post-layout simulations. It operates at 500 MHz frequency and can reach the maximum operating frequency of 1 GHz. The proposed comparator occupies an area of 20 μm–8 μm and consumes 67 fJ of energy at 500 MHz. The average latency of the comparator is 70 ps throughout the input range, and the input-referred noise is 2 mV at 1 GHz frequency. The worst-case kickback noise for the entire working range is 5.5 mV, which is verified through simulations, and it is 10 times less compared to the conventionally designed comparator. The future work includes the integration of the designed comparator into SAR ADC followed by design tape-out.

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