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A Bi/Tri-level Self-Adaptive Two-Step DAC Switching Scheme for High-Power Efficiency SAR-Based ADCs

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Abstract

A high energy-efficient and reference voltage self-adaptive switching scheme for a triple-capacitive array successive approximation register analog-to-digital converters is proposed. The proposed switching time scheme includes Bi-level and Tri-level modes. The operating mode can be automatically switched by the reference voltage self-adaptive module according to the number of reference voltages of the peripheral circuits. The proposed timing scheme has the advantage of automatic compatibility with Bi/Tri-level reference voltage, which can be better adapted to the requirements of different hybrid ADC architectures. In Bi/Tri-level mode, two-step method, and monotonic switching scheme, floating capacitor technology is used to achieving 99.6% and 99.9% savings in average switching energy and a 73.4% reduction in total capacitance compared to the conventional scheme when applied to a 10-bit SAR ADC. The INL and DNL for both the Bi-level reference mode and the Tri-level reference mode are 0.350, 0.347 and 0.177, 0.172, respectively. In addition, the scheme eliminates to reset energy while regulating M to achieve a compromise between energy, area, and linearity. The post-simulation results show that the 10-bit SAR ADC with the proposed switching scheme can achieve a signal-to-noise distortion ratio (SNDR) of 60.53 dB and a spurious-free dynamic range (SFDR) of 68 dB at a sampling rate of 20 MS/s in a 65 nm CMOS process. The area of this ADC is only 0.2392 mm^2.

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1 Introduction

The development of analog-to-digital converters (ADCs) has changed from the traditional design ideas of low-power successive approximation registers (SARs), high-speed Pipelined SARs, and high-accuracy Delta-Sigma ADCs to a high power-efficiency development, resulting in ADCs such as high-accuracy time-to-digital converters (TDCs) and VCO-SARs. DAC capacitive switching circuits are one of the main energy consuming components of many ADCs, such as VCO-SAR [2], Pipelined-SAR [6, 14], and MASH ADC [13]. For example, reference [15] presented a switched-capacitor array applied to an SAR ADC in which the comparator, digital logic control circuit, and DAC capacitor array account for 8.9%, 8.6%, and 53%, respectively.

SAR-based architectures are gaining importance because they do not require high-energy consumption amplifiers and are being adopted in new types of MASH ADC, VCO-SAR [31], and Pipeline SAR ADCs [14]. The key to high power-efficiency designed of SAR ADCs is in the switching strategy of the DAC array. The DAC timing strategy from the traditional monotonic structure is gradually researched. In addition to power consumption, the linearity, the number of DAC capacitors, and other issues are gradually given attention. A number of switching solutions have been proposed to address power consumption, linearity, and area issues.

Low-power consumption Digital-to-analog converters have been the focus on attention, with the key points being energy-efficient switching technology and reduced capacitor count [1, 10, 12, 18, 20, 22, 23]. The two-level reference voltage switching scheme is not ideal for energy saving [12, 23]. So, the third level reference voltage V_{cm} ($1/2V_{ref}$) is introduced [3, 12, 21, 27, 30, 33, 34, 36]. Compared to traditional switching energy consumption can be saved by more than 80%. To further to reduce the switching energy, several switching methods are used, including floating capacitor techniques [7, 11, 29], the introduction of a fourth reference voltage V_{aq} ($1/4V_{ref}$) [24], monotonic structure [17], and two-step structure schemes [3, 4, 8, 9]. However, each method has its disadvantages. Higher DAC logic complexity is required [5, 32], more than enough reference voltage is needed [16, 26], excessive common-mode voltage swing [27].

In terms of the number of external reference voltages, there are two common switching strategies with Bi-level and Tri-level reference voltages. Although increasing the number of reference voltages can effectively reduce power consumption and improve linearity, the problem is that adding an additional number of references adds a burden on the peripheral circuitry and additional circuit overhead.

The idea of considering only the harsh conditions of increasing reference levels in many switching scheme papers without compatibility with external applications can make it difficult for these switching strategies to be more widely used. Thus, it is not only necessary to consider how to optimize the structure of the switching scheme, but

also the external conditions to improve the compatibility of the timing scheme against the external reference level.

Therefore, a switch structure that can be adjusted according to the number of external levels is proposed. This increases the compatibility of DAC switching technology and allows it to be freely selected in different external configurations. The proposed reference voltage self-adaptive switching structure has good linearity and very low power consumption in Tri-level mode and excellent compatibility in Bi-level mode with only two reference levels. In addition, there is no reset energy consumption of both modes in the proposed switching strategy.

The rest of the paper is structured as follows: Section 2 describes the proposed reference voltage self-adaptive switching scheme. Sect. 3 discusses the proposed switching strategy of common-mode voltage variation. Section 4 and Sect. 5 mainly compare and analyze the energy consumption of the switching mode in this paper with various previous switching schemes. Section 6 analyzes and compares the advantages and disadvantages of the linearity of Bi-level reference mode and Tri-level reference mode switch technology. Section 7 draws conclusions.

2 Proposed Switching Strategy

Although the proposed timing technique can support a minimum of a 4-bit SAR structure, to reflect the scalability of the structure, a 10-bit SAR is used as an example in this paper. This technique has a two-step structure divided into two stages of coarse quantization and fine quantization. The proposed novel switch array is a reference voltage self-adaptive structure of the option to adopt Bi-level reference voltage modes and Tri-level reference voltage modes. The proposed switching scheme adds a balancing capacitor to the finely quantized capacitor array so that each bit of the finely quantized capacitor can match the corresponding conversion bit inversion voltage.

In the proposed structure, M controls the length of the coarsely and finely quantized capacitor arrays of both capacitor arrays. Different values of M can be set from 2 to 7, and different values of M have various energy consumption and linearity. Figure 1 shows the architecture of the proposed 10-bit SAR ADC, where C is the unit capacitor. The ADC includes a coarse quantization capacitor array (CCA), two fine quantization capacitor arrays (FCA), a four-input comparator, and SAR logic control circuitry. These include Tri-level reference voltages, V_{cm} (1/2 of V_{ref}), V_{aq} (1/4 of V_{ref}), and gnd. The number of three references is kept constant when the Tri-level reference switching mode is adopted, and the V_{aq} reference voltage is turned off when the Bi-level reference mode is chosen, as shown in Fig. 2.

2.1 Switching Mode for Bi-Level

Figure 2 shows the structure of the proposed Bi-level voltage mode of the reference voltage self-adaptive switching scheme. When only two external reference voltages are available, the DAC array can use the proposed "Bi-level" switching mode, increasing the adaptability of the overall structure. The Bi-level reference mode uses two reference

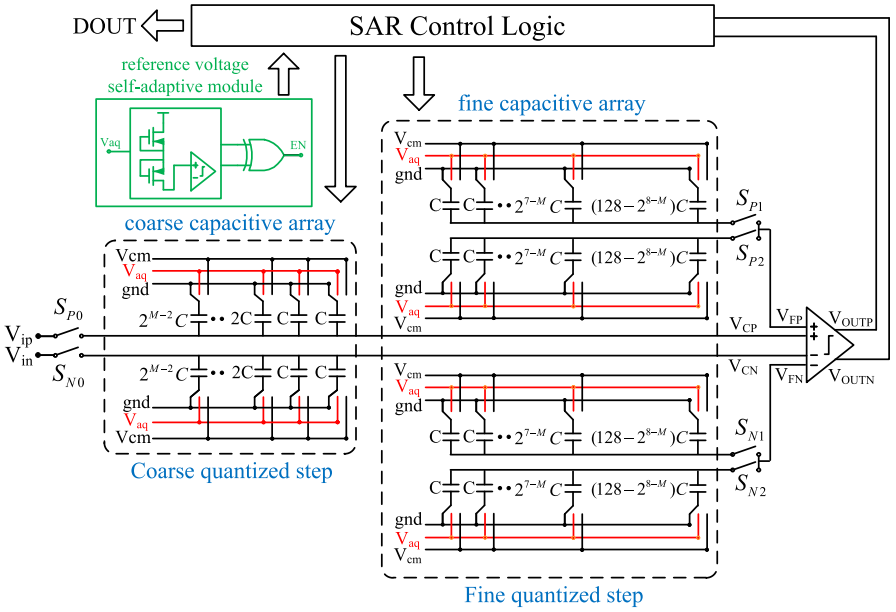

Fig. 1 Illustrated reference voltage self-adaptive structure of the proposed 10-bit SAR ADC

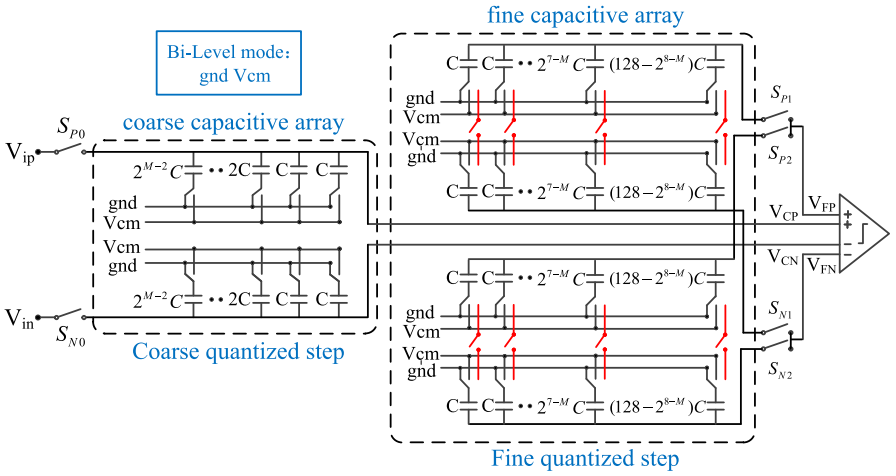

Fig. 2 Illustrated Bi-level reference voltage structure of the proposed 10-bit SAR ADC

levels, V_{cm} and gnd, and disables the dependence on an additional reference voltage (V_{aq}). The Bi-level switching scheme combines partial floating capacitor technology with single-ended capacitor floating technology to implement the conversion process.

The proposed Bi-level reference mode consists of three phases: input sampling, coarse quantization, and fine quantization. During the sampling phase, the top plates

of the capacitors in the CCA are connected to the input signal, and the bottom plates of all capacitors in the CCA are connected to V_{cm}. At the same time, the bottom plates of the S_{P1} and S_{N2} capacitors in the FCA are reset to V_{cm} and the bottom plates of the S_{P2} and S_{N1} capacitors are reset to gnd.

Figures 3 and 4 show the voltage reversal of the proposed five-bit Bi-level voltage capacitor switching scheme. At the end of the first comparison, if $V_{ip} > V_{in}$, the S_{P1} and S_{N1} capacitor bottoms in the FCA are interconnected at this time, realizing that

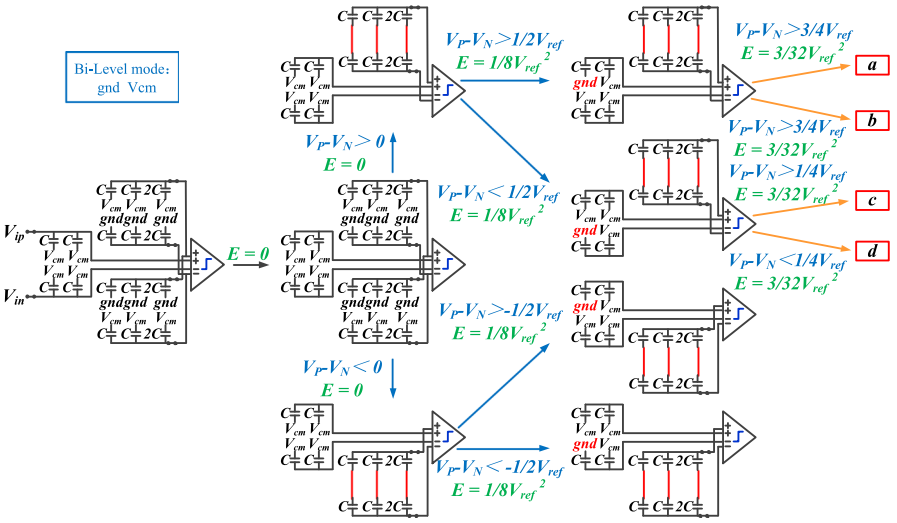

Fig. 3 Proposed Bi-level reference mode switching scheme for the first three DACs

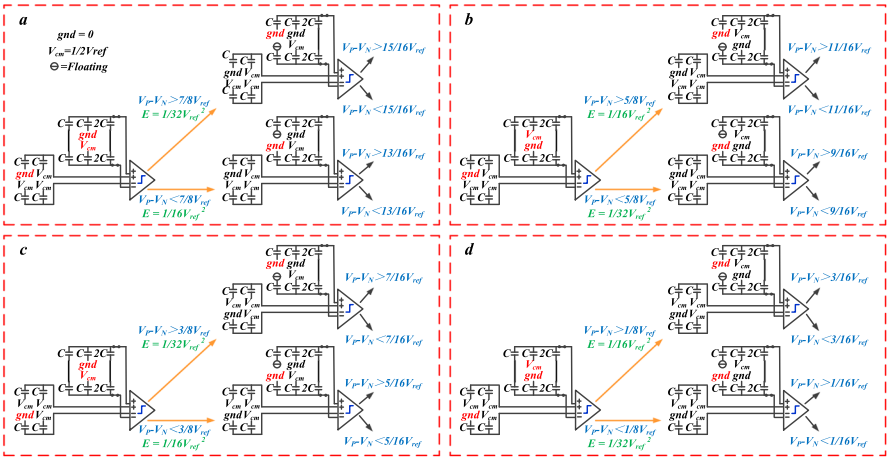

Fig. 4 Proposed Bi-level reference mode switching scheme for the fourth and fifth DACs

the voltage at the positive end of the comparator drops by 1/4 and the voltage at the negative end of the comparator rises by 1/4.

When D [1] = 1, the energy consumed by the voltage flipped is zero, as the following equation proves:

$$E_{\mathrm{FP}} = C_{\mathrm{FP\_tot}}(-V_{\mathrm{aq}})[(V_{\mathrm{FP2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - V_{\mathrm{cm}})] = 0 \tag{1}$$

$$E_{\mathrm{FN}} = C_{\mathrm{FN\_tot}}(-V_{\mathrm{aq}})[(V_{\mathrm{FN2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - 0)] = 0 \tag{2}$$

$$E_{\mathrm{FP}} + E_{\mathrm{FN}} = 0 \tag{3}$$

The coarse quantization of the capacitor array single-ended flip is performed next, and when $V_{\mathrm{cp}} > V_{\mathrm{cn}}$, the high capacitance bottom base plate voltage of the capacitor array at V_{cn} will be connected from V_{cm} to gnd.

As D [2] = 1 consumes $1/8CV_{\mathrm{ref}}{}^2$switching energy, it is proven in the following equations:

$$E_{\mathrm{CP}} = C_{\mathrm{CP\_vcm}}(-V_{\mathrm{cm}})[(V_{\mathrm{CP2}} - V_{\mathrm{cm}}) - (V_{\mathrm{CP1}} - V_{\mathrm{cm}})] = \frac{1}{8}C{V_{\mathrm{ref}}}^2 \tag{4}$$

The N-terminal capacitor array has no energy consumption, and the total power consumption is:

$$E_{\mathrm{CP}} + E_{\mathrm{CN}} = \frac{1}{8}C{V_{\mathrm{ref}}}^2 \tag{5}$$

The capacitor array of the fine quantization stage uses a double-ended capacitor flip. When $V_{\mathrm{CP}} > V_{\mathrm{CN}}$, D [3] = 1 capacitor array using a double-ended capacitance flip results in the flip as shown in Fig. 4 'a,' consuming energy as follows:

$$E_{\mathrm{FP}} = C_{\mathrm{FP\_vaq}}(-V_{\mathrm{aq}})[(V_{\mathrm{FP2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - V_{\mathrm{aq}})] = \frac{3}{64}C{V_{\mathrm{ref}}}^2 \tag{6}$$

$$\begin{aligned} E_{\mathrm{FN}} =& C_{\mathrm{FN\_vcm}}(-V_{\mathrm{cm}})[(V_{\mathrm{FN2}} - V_{\mathrm{cm}}) - (V_{\mathrm{FN1}} - V_{\mathrm{aq}})] \\ &+ C_{\mathrm{FN\_vaq}}(-V_{\mathrm{aq}})[(V_{\mathrm{FN2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FN1}} - V_{\mathrm{aq}})] = \frac{3}{64}V_{\mathrm{ref}}^2 \end{aligned} \tag{7}$$

$$E_{\mathrm{FP}} + E_{\mathrm{FN}} = \frac{3}{32}CV_{\mathrm{ref}}^2 \tag{8}$$

The last bit uses a floating capacitor technique where the voltage at one end is reduced to gnd and the other end is held. The above equation proves that the total energy consumption is smaller. The energy consumption of the proposed Bi-level reference voltage model is reduced by 99.6% compared to the conventional structure.

2.2 Switching Mode for Tri-level

When an external reference voltage is sufficiently provided, the DAC array can use the proposed Tri-level reference voltage technique to further to improve linearity and switching power consumption. Figure 5 shows the overall structure of the Tri-level reference voltage.

During the sampling phase, the top plates of the capacitors in the CCA are connected to the input signal, and the bottom plates of all capacitors in the CCA are connected to V_{aq}. Meanwhile, the bottom plates of the S_{P1} and S_{N2} capacitors in the FCA are reset to V_{cm} and the bottom plates of the S_{P2} and S_{N1} capacitors are reset to gnd.

Figures 6 and 7 show the voltage reversal of the proposed five-bit Tri-level reference voltage capacitor switching scheme. At the end of the first comparison, if $V_{\mathrm{ip}} > V_{\mathrm{in}}$, the S_{P1} and S_{N1} capacitor bottoms in the FCA are reset to V_{aq} at this time, thus achieved a 1/4 drop in the voltage at the positive side of the comparator and a 1/4 rises in the voltage at the negative side of the comparator.

In the first comparison cycle, when D [1] = 1, the consumed switching energy is calculated by:

$$E_{\mathrm{FP}} = C_{\mathrm{FP\_tot}}(-V_{\mathrm{aq}})[(V_{\mathrm{FP2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - V_{\mathrm{cm}})] = 0 \tag{9}$$

$$E_{\mathrm{FN}} = C_{\mathrm{FN\_tot}}(-V_{\mathrm{aq}})[(V_{\mathrm{FN2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - 0)] = 0 \tag{10}$$

$$E_{\mathrm{FP}} + E_{\mathrm{FN}} = 0 \tag{11}$$

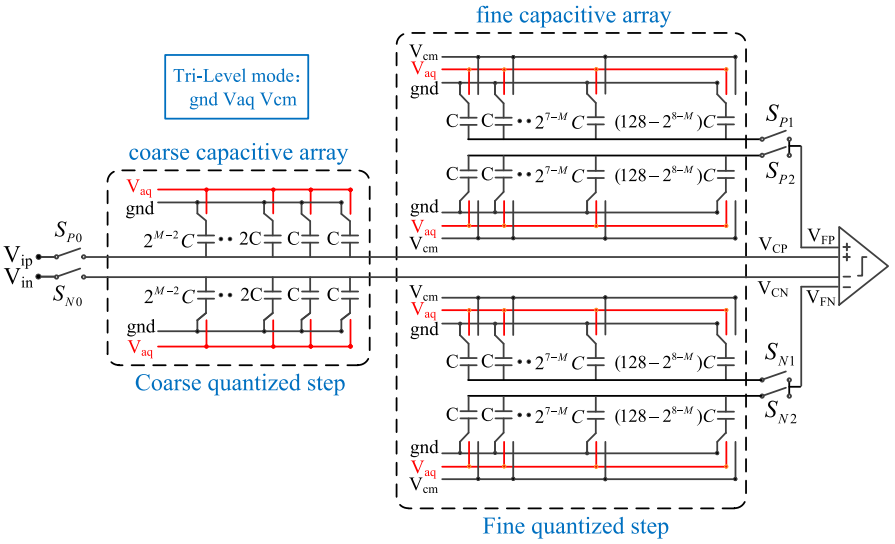

Fig. 5 Illustrated Tri-level reference voltage structure of the proposed 10-bit SAR ADC

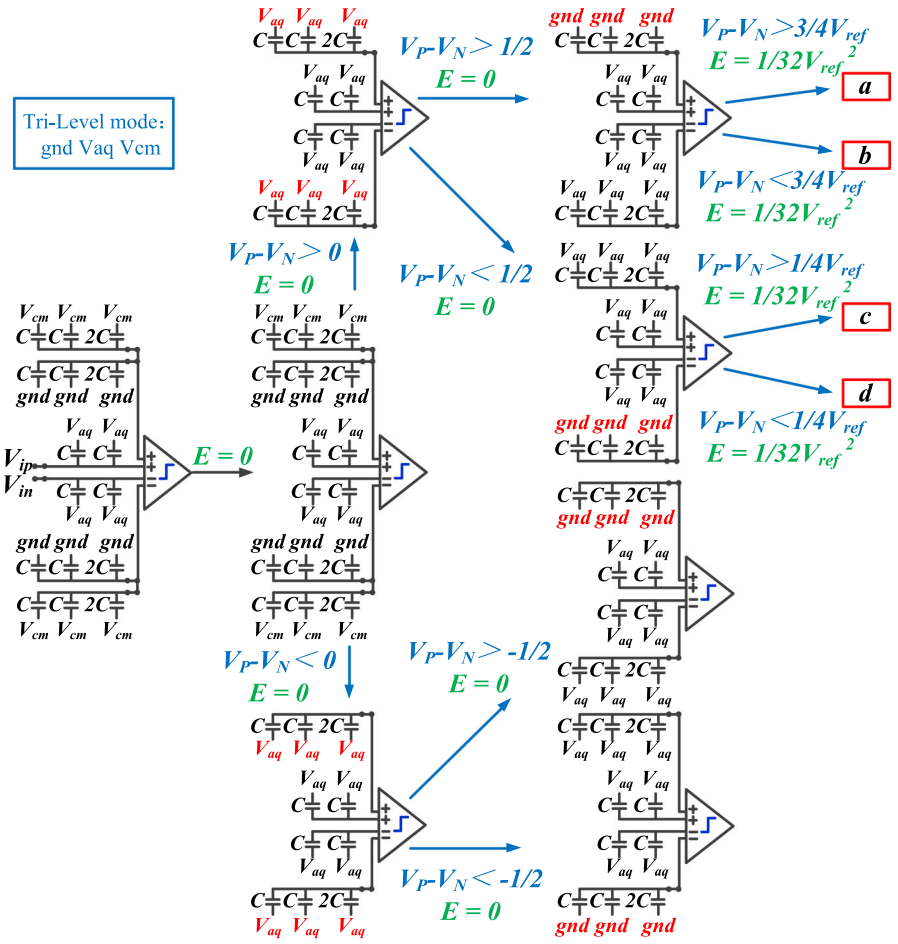

Fig. 6 Conversion in Tri-level reference mode for the first three times

The second capacitor array flip, D [2] = 1, is performed next when $V_{CP} > V_{CN}$, at which point the S_{P1} capacitor base in the FCA is reset to gnd, achieving a voltage drop of 1/4 on the positive side of the comparator. This process has no energy consumption. Total power consumption is zero.

When $V_{CP} > V_{CN}$, D [3] = 1, the coarse quantization capacitor array uses single-ended capacitance flipping, and the high capacitance voltage is flipped from V_{aq} to gnd. The result of the way flip is shown as 'a' in Fig. 5. In this bit-cycle, the switching energy is consumed by:

$$E_{FP} = C_{CP\_\,vaq}(-V_{aq})[(V_{CP2} - V_{aq}) - (V_{CP1} - V_{aq})] = \frac{1}{32} C V_{ref}{}^2 \qquad (12)$$

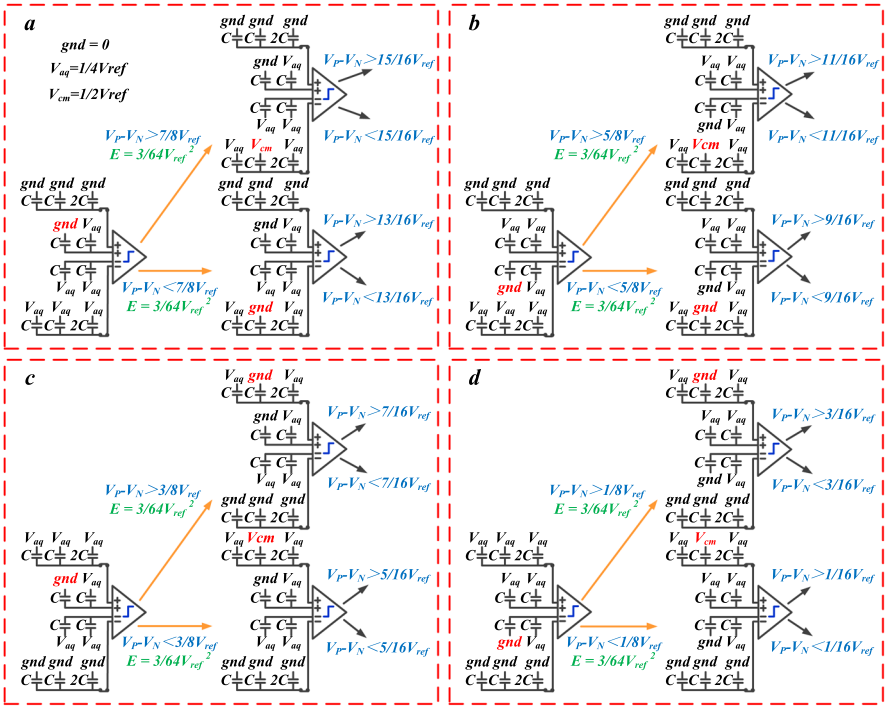

Fig. 7 In Tri-level reference mode, the fourth, and fifth conversions

The N-terminal capacitor array consumes zero energy. Total energy consumption is:

$$E_{\mathrm{FP}} + E_{\mathrm{FN}} = \frac{1}{32} C {V_{\mathrm{ref}}}^2 \tag{13}$$

When $V_{\mathrm{CP}} > V_{\mathrm{CN}}$ and D [4] = 1, the capacitor array uses a single-ended capacitance float. The voltage at the high side of the capacitor array bottom plate at the V_{CN} end will be connected to V_{cm} by V_{aq}. Similarly, the energy of this process is calculated as follows:

$$\begin{aligned} E_{\mathrm{FP}} =& C_{\mathrm{FN\_vcm}}(-V_{\mathrm{cm}})[(V_{\mathrm{FP2}} - V_{\mathrm{cm}}) - (V_{\mathrm{FP1}} - V_{\mathrm{aq}})] \\ &+ C_{\mathrm{FN\_vaq}}(-V_{\mathrm{aq}})[(V_{\mathrm{FP2}} - V_{\mathrm{aq}}) - (V_{\mathrm{FP1}} - V_{\mathrm{aq}})] = \frac{3}{64} C {V_{\mathrm{ref}}}^2 \end{aligned} \tag{14}$$

The P-terminal capacitor array consumes zero energy. So, the energy consumption expression is:

$$E_{\mathrm{FP}} + E_{\mathrm{FN}} = \frac{3}{64} C {V_{\mathrm{ref}}}^2 \tag{15}$$

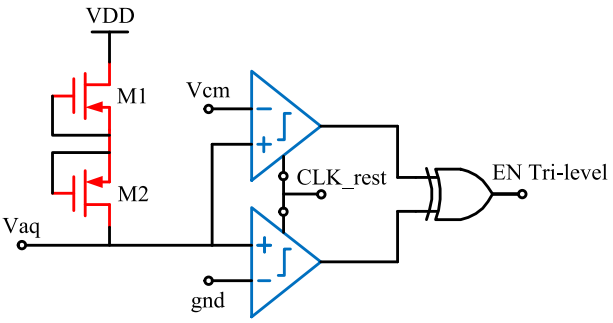

Fig. 8 Reference voltage self-adaptive module

The proposed Tri-level reference voltage mode consumes 99.9% less energy than the conventional structure. The Tri-level voltage mode has higher energy efficiency compared to the Bi-level voltage mode.

2.3 Reference Voltage Self-Adaptive Scheme

Figure 8 illustrates the reference voltage self-adaptive judgment module. The two dynamic comparators start operating when the ADC resets clock signals to arriving. V_{aq} is connected to the judgment module and to VDD through a pull-up resistor. The static power consumption can be greatly reduced since the pull-up resistor is a PMOS pseudo-resistor (resistance of GΩ level). When V_{aq} is overhung, the pull-up resistor causes the voltage at the comparator input to be VDD, and both comparators compare to 1. The judgment result returned through to the XOR gate is 0, which means that no additional external reference level is determined, and Bi-level reference mode is used. When V_{aq} is connected to the ADC, the upper and lower comparator outputs result in 0 and 1, and the judgment result returned through the XOR gate is 1, using Tri-level reference mode. Therefore, the proposed periphery level judgment module can self-adapt to the external reference situation for the timing strategy change. In addition, since a coarse dynamic comparator and a pseudo-resistor are used and compared only once during the reset phase, the power consumption is basically negligible compared to the DAC switching energy consumption.

2.4 DAC Control Logic Complexity Analysis

The control circuit of the overall circuit structure includes a Tri-level reference mode control circuit and a Bi-level reference mode control circuit. The reference voltage self-adaptive module is highly adaptable because it selects either the Bi-level voltage mode or the Tri-level voltage mode based on the voltage reference provided by the external circuit.

The control circuit of the Bi-level voltage switching mode uses a single-ended flip switching scheme to lower the bottom plate of the switching array of the low voltage end to V_{cm} to gnd in the coarse quantization stage. A double-ended flip technique is

used in the fine quantization stage, and for the last bit, a single-ended flip other end hold is used.

The coarse quantization staged and the fine quantization stage of the control circuit of the Tri-level switching mode both use single-ended flipped conversion. The difference is that in the coarse quantization stage, the switch array bottom plate at the low voltage end is lowered from V_{aq} to gnd. The fine quantization stage will fix one end of the capacitor array voltage either up or down. The control logic of the proposed switching structure is not complex compared to many recent ideas, e.g., TSDC [3], TSMS [9].

2.5 The Proposed Four-Input Comparator

Traditional four-input comparators have only one stage structure with large offset and delay, so this paper proposes a novel type of two-stage four-input comparator. The proposed four-input comparator is designed as shown in Fig. 9. The proposed comparator consists of a pre-amplification stage, a comparison stage and a latching stage. The pre-amplification stage sets the bias voltage to keep the Vgs voltage of the differential input pair the same as the common-mode variation and to reduce the effect of V_{cm} and V_{aq} on gain and offset [8].

Figure 10 shows 500-run Monte Carlo simulations for the coarsely quantized port. It can be seen that the offset at the coarse quantization port is 665 μV, and this offset is a fixed offset due to the design while the dynamic offset is $3\sigma = 3*19\ \mu V = 57\ \mu V$ (process & mismatch).

Figure 11 shows 500-run Monte Carlo simulations for the finely quantized port. It can be seen that the fixed offset is 137.6 μV, and the dynamic offset is $3\sigma = 3*3.67\ \mu V = 11.01\ \mu V$.

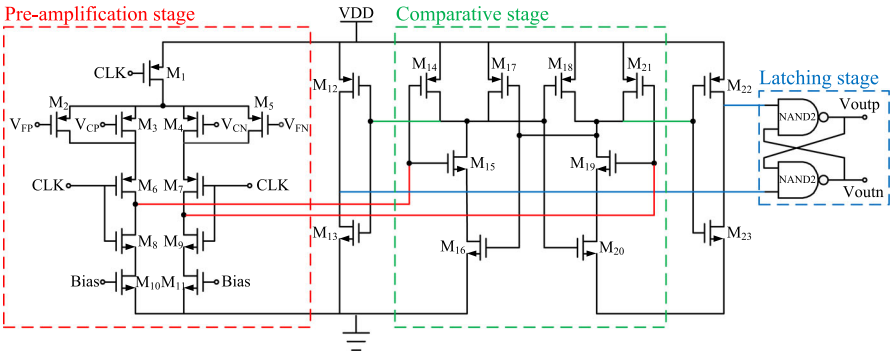

Fig. 9 Proposed four-input comparator

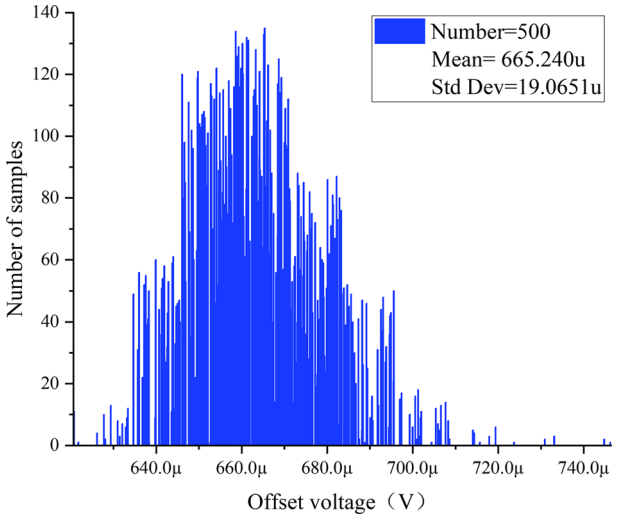

Fig. 10 Monte Carlo simulations of input Vcp, Vcn

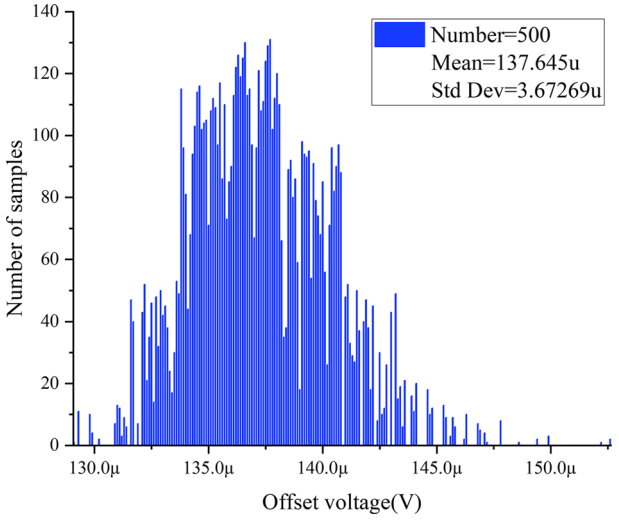

Fig. 11 Monte Carlo simulations of input Vfp, Vfn

3 Analysis of Common-Mode Voltage in Timing Switches

The input common-mode voltage range puts demand on the comparator performance, and a large range of common-mode voltage swing can lead to increased comparator noise. Figure 12 shows the 10-bit DAC output waveform of the proposed Bi-level reference voltage capacitor switching scheme in M = 5. At the end of the first comparison, since $V_{ip} > V_{in}$, all capacitor arrays of fine quantization are connected to each

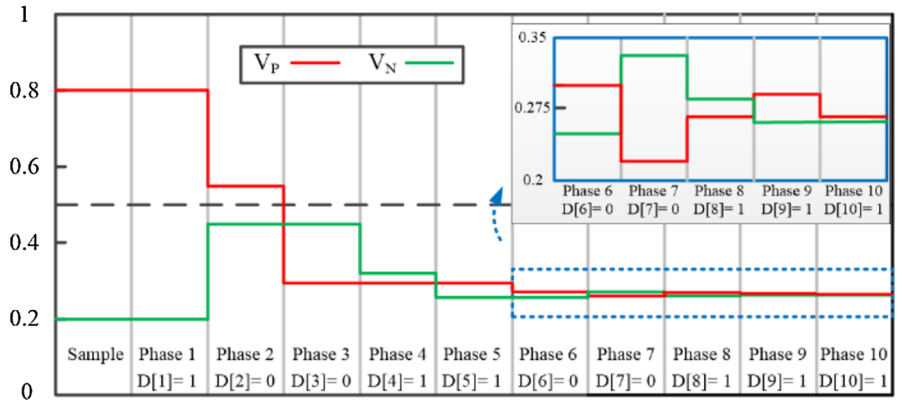

Fig. 12 Voltage conversion of Bi-level reference voltage modes

other at this point, and the voltage at the positive side of the comparator achieves a 1/4 V_{ref} voltage dropped and the voltage at the negative side of the comparator achieves a 1/4 V_{ref} voltage rise. At the end of the second comparison, the voltage at the positive end of the comparator achieves a voltage drop of 1/4 V_{ref} due to $V_{\text{ip}} > V_{\text{in}}$ when the bottom plate of the capacitor array of the positive end of the comparator is connected to gnd. The D [2:5] digital code is implemented by inverting the CCA. The D [6:10] digital code is implemented by inverting the with FCA.

Figure 13 shows the 10-bit DAC output waveform of the proposed Tri-level reference voltage capacitor switching scheme in M = 5. At the end of the first comparison, since $V_{\text{ip}} > V_{\text{in}}$, S_{P2}, S_{N2} turn off, and FCA bottom voltage are connected to V_{aq}, the voltage at the positive side of the comparator achieves a 1/4 V_{ref} voltage drop, and the voltage at the negative side of the comparator achieves a 1/4 V_{ref} voltage rise. At the end of the second comparison, since $V_{\text{ip}} > V_{\text{in}}$, the array of capacitors with fine quantization at the positive side of the comparator is connected to gnd at this time, and

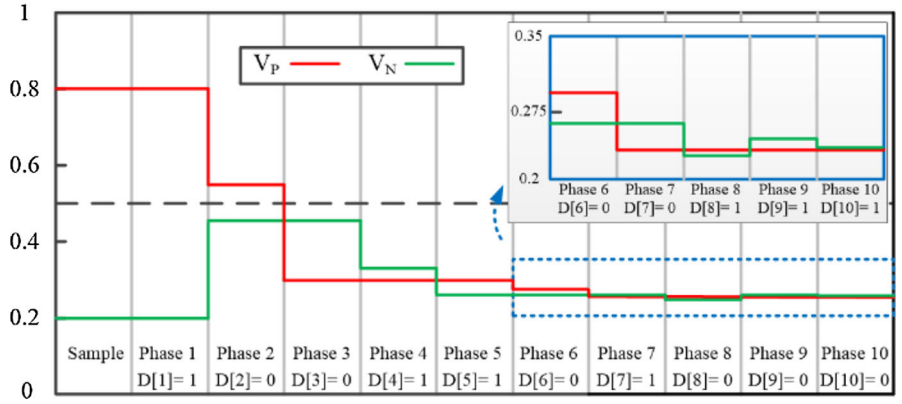

Fig. 13 Voltage conversion of Tri-level reference voltage modes

the voltage at the positive side of the comparator achieves a voltage drop of 1/4 V_{ref}. The D [3:6] digital code is implemented by inverting the capacitor array of CCA. The D [7:10] digital code is implemented by inverting the code with FCA. The pressure on the common-mode offset is less for the comparator, and comparators with high common-mode range requirements can be used in our approach.

Figures 12 and 13 show each voltage inversion for both Bi-level and Tri-level modes. Both proposed structures have a maximum common-mode offset of less than 0.25 V_{ref} due to the first double-ended inversion mode. The structure in references [1, 27] uses a single-ended inversion case; therefore, the maximum common-mode voltage offset is less than 0.5 V_{ref}. Therefore, the proposed technique requires less comparators, reduces the difficulty of circuit designed, and improves compatibility.

4 Dynamic Performance Analysis

4.1 Effects of Capacitor Mismatch

The dynamic performance of the ADC is influenced by the accuracy per unit capacitance. Figures 14 and 15 show the FFT analysis after 500-run Monte Carlo simulations of a 10-bit SAR ADC with Tri-level and Bi-level in the capacitance mismatch range of 0–1%. Figure 15 illustrates that the dynamic performance decreases with increasing capacitance mismatch. When the capacitance mismatch is 1%, the SFDR and SNDR are reduced by 12.1 and 3.1 dB for the Bi-level switching scheme and 9.4 and 0.7 dB for the Tri-level switching scheme, respectively.

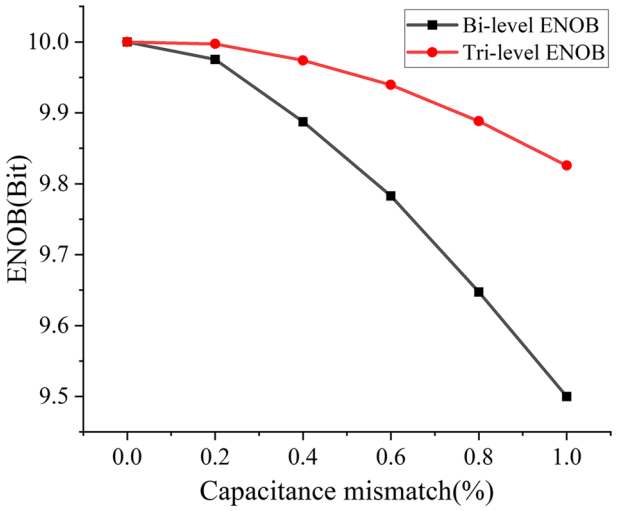

Fig. 14 Effect of capacitive mismatch on ENOB

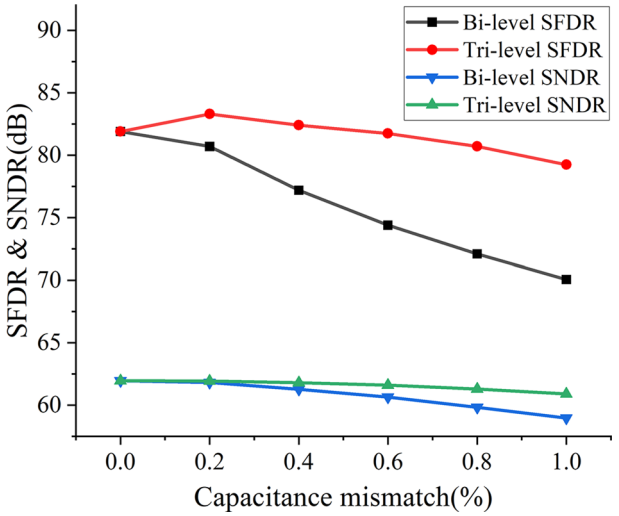

Fig. 15 Effect of mismatch on SNDR and SFDR

4.2 Effects of Voltage Mismatch

The dynamic performance of the ADC is also affected by the accuracy of the reference voltages V_{cm} and V_{aq}. Figures 16 and 17 show the FFT analysis after 500-run Monte Carlo simulations of a 10-bit SAR ADC with Tri-level and Bi-level in the voltage mismatch range of 0–0.5%. Figure 17 illustrates that the dynamic performance decreases with increasing capacitance mismatch. When the capacitance mismatch is

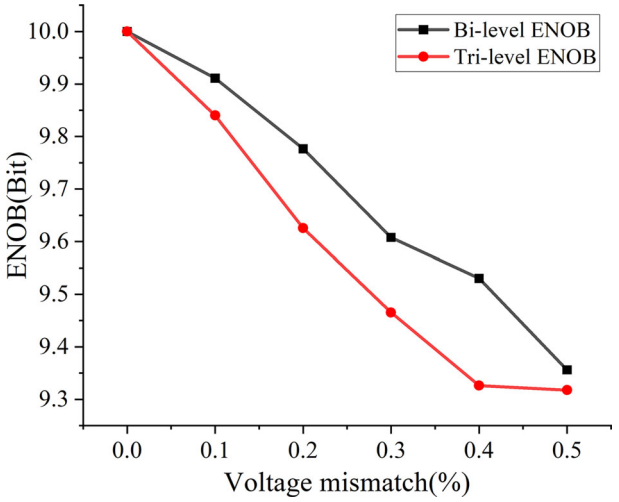

Fig. 16 Effect of voltage mismatch on ENOB

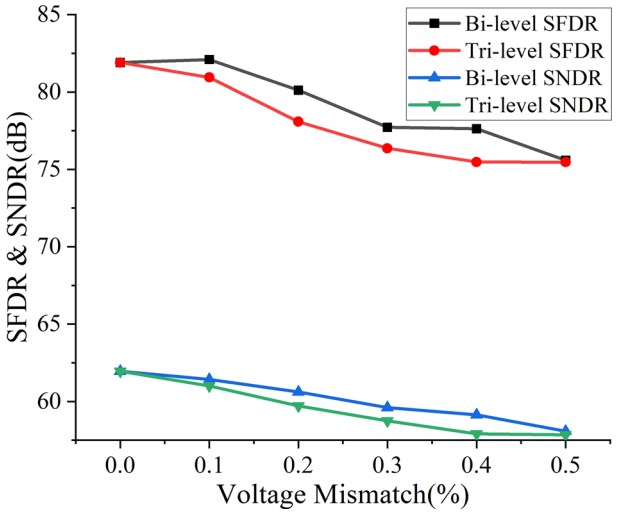

Fig. 17 Effect of mismatch on SNDR & SFDR

0.5%, the SFDR and SNDR decreased by 9.8 and 3.02 dB, respectively, for the Bi-level switching scheme, and by 13.4 and 4.29 dB, respectively, for the Tri-level switching scheme.

4.3 The Effect of Mismatch on FFT

The proposed switched-capacitor array introduces CCA and FCA to establish a two-step structure framework, and the energy consumption of the two-step switching scheme is $37.5CV_{ref}{}^2$, which is 97.2% saving compared to the conventional switching scheme. To verify the effect of non-ideal factors, a 10-bit SAR ADC model was built in MATLAB.

Figures 18 and 19 show 500 points of SFDR, SNDR, and ENOB for the proposed switching scheme in Bi-level mode and Tri-level mode at a sampling rate of 1 MS/s and an input signal frequency of 243.652 kHz. The number of FFT points simulated in Figs. 18 and 19 is 2048. There is almost no spurious and harmonics in the Bi-level mode and the Tri-level mode proposed by the ideal model in Figs. 18a and 19a. The SNDR and SFDR dropped to 61.7 dB and 78.1 dB for adding the voltage mismatch Bi-level mode as seen in Fig. 18b. The SNDR and SFDR dropped to 59 dB and 73.5 dB for adding the capacitive mismatch Tri-level mode in Fig. 18c. Figure 18d shows that when capacitance mismatch (1%), V_{cm} and V_{aq} mismatch (0.1%) are added to the ideal model simultaneously, SNDR and SFDR decrease to 58.6 and 64.3 dB, respectively.

Figure 19d shows that the Tri-level model reduces the SNDR and SFDR to 58.5 dB and 67.2 dB, respectively; when capacitance mismatch (1%), V_{cm} and V_{aq} mismatch (0.1%) are added to the ideal model at the same time. The switched-capacitor scheme still has good stability when the noise increases.

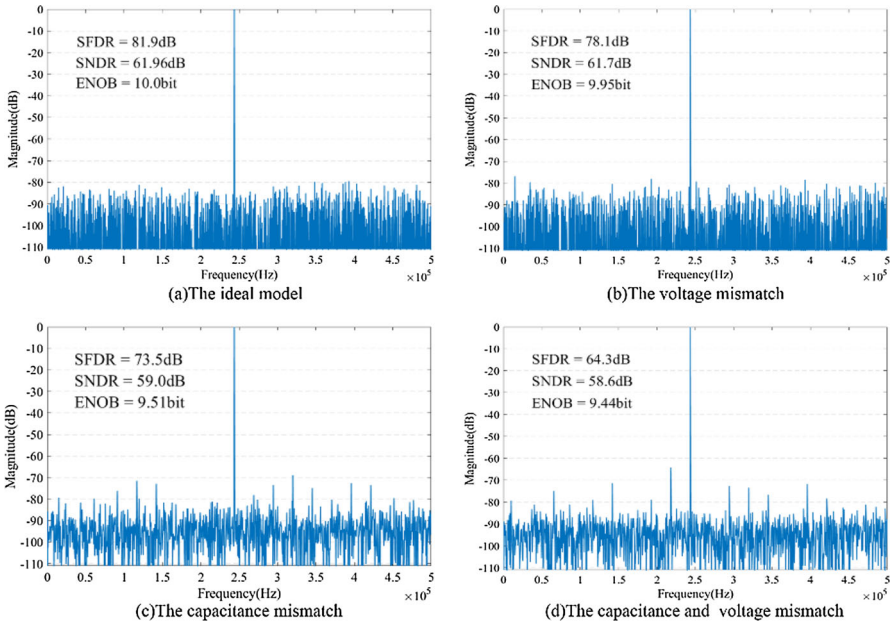

Fig. 18 FFT spectrum at a sampling rate of 1 MS/s in Bi-level mode

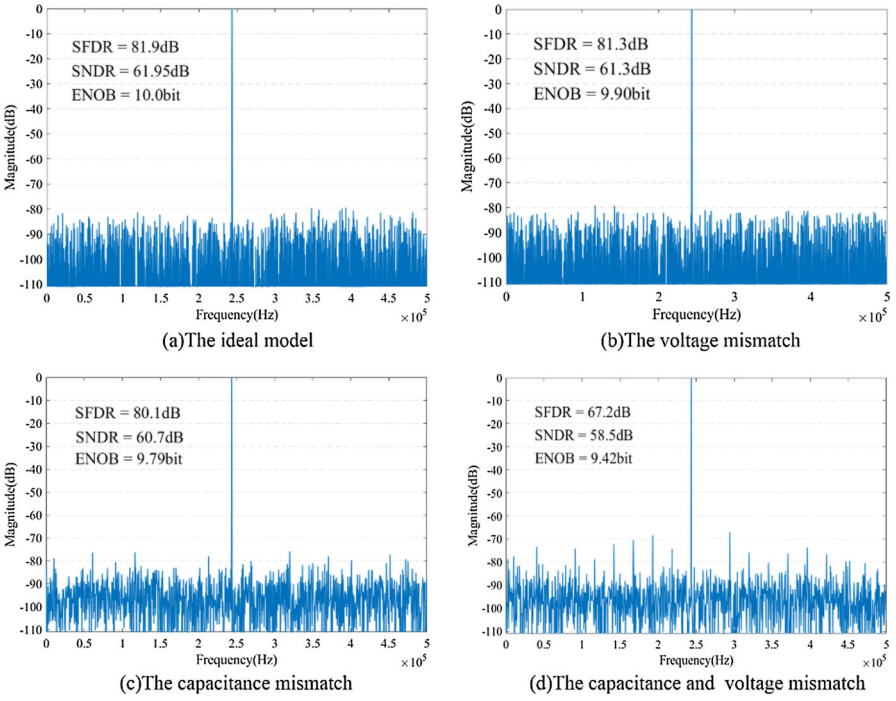

Fig. 19 FFT spectrum at a sampling rate of 1 MS/s in Tri-level mode

4.4 Post-Simulation Results

To verify the implementation of the proposed switched-capacitor array, we designed a 10-bit 10 MS/s SAR ADC with the proposed switching scheme. The SAR ADC with the proposed switching scheme is designed in a 65 nm CMOS process with a 1.2 V supply. Figure 20 shows the layout of the SAR ADC with an effective area of 0.2392 mm^2. The unit capacitance size is 20 fF.

Figure 21 shows the power consumption of each module of the proposed SAR ADC. The total power is 548.5 μW, of which clock circuit, CDAC, S/H, Dynamic SAR

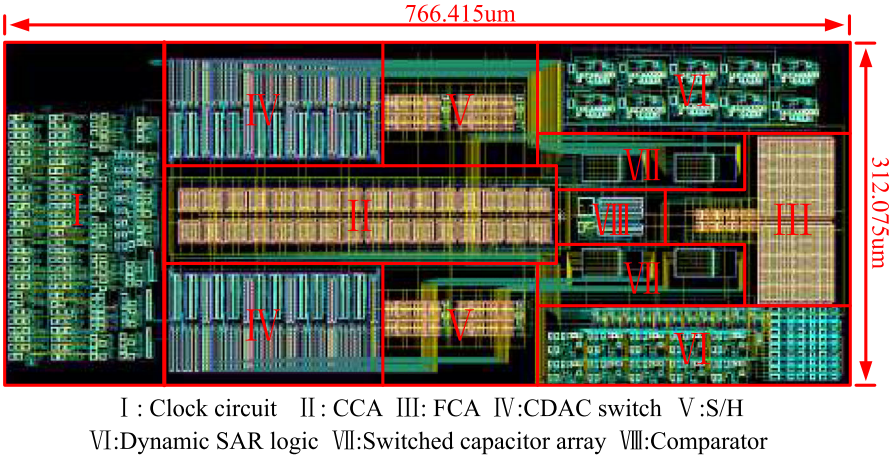

Fig. 20 Layout of the proposed SAR ADC

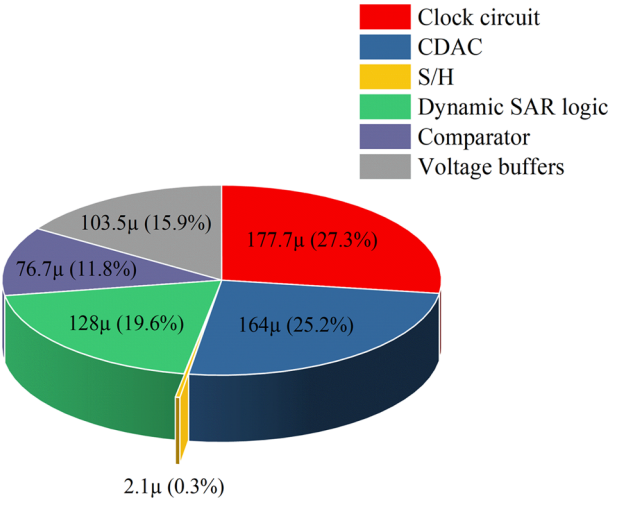

Fig. 21 Percentage of energy consumption

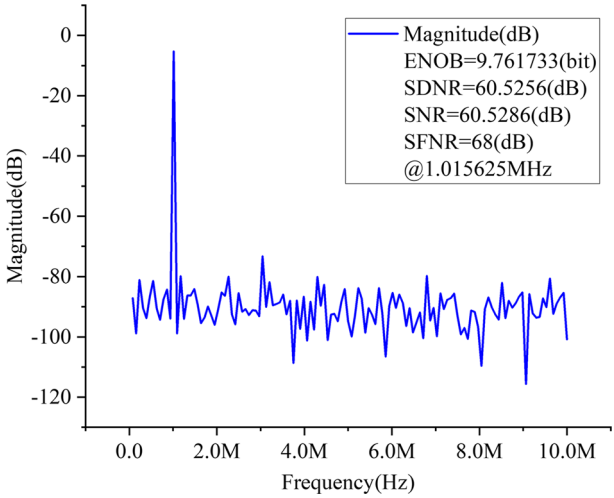

Fig. 22 FFT spectrum at the sampling rate of 20 MS/s

logic, comparator, and voltage buffers are 177.7, 164, 2.1, 128, 76.7, and 103.5 μW, respectively. It is proved that the switching scheme has very low power consumption. Figure 22 shows the post-simulation results of the SAR ADC with SND, SFDR, SNDR, and ENOB of 60.528 dB, 68 dB, 60.525 dB, and 9.76 bits, respectively, at 1.015625 MHz input frequency. The number of FFT points simulated in Fig. 22 is 256. Through the SNDR and SFDR of the post-simulation results, it can be seen that the switching scheme has good linearity.

5 Analysis of Energy Consumption in Timing Switches

In order to facilitate the analysis and comparison, this section presents the energy consumption analysis in both the Bi-level reference mode and Tri-level reference mode cases, respectively. The proposed two-step structure is divided into a coarse quantization stage and a fine quantization stage, each of which implements a portion of the digital code conversion. M determines the number of bits in each of the two quantization segments. In the theoretical analysis, M can be set to 2 to 7, but considering the noise, the sampling array cannot be too short, so M cannot be too small. Therefore, only the cases of "M = 4, 5, 6" are analyzed in this section. The behavioral simulation of the proposed switching method is carried out in MATLAB and proposed to this paper for the case of a 10-bit SAR ADC with different M values. In order to simplify the analysis, the modeling analysis here does not have the influence of non-ideal factors caused by the parasitic capacitance, and the analysis of the non-ideal influence of parasitic capacitance is discussed in later section.

Figure 23 shows the switching energy consumption of the Bi-level reference mode for different M values. The conclusion is that the smaller the value of M, the lower the energy consumption of the switch. As shown in Table 1 below, Bi-level reference

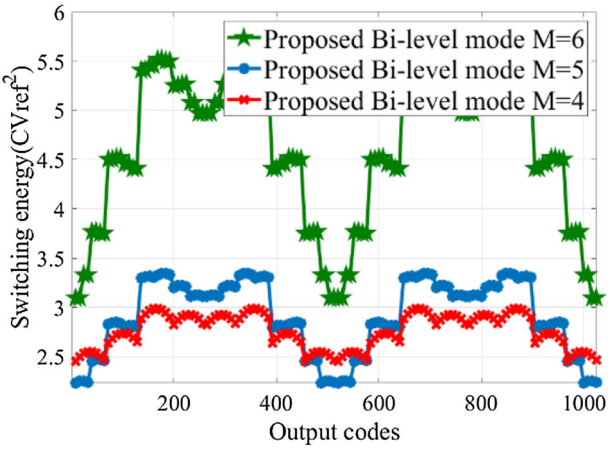

Fig. 23 Energy consumption of Bi-level reference voltage switching schemes at M = 4,5,6

Table 1 Analysis of Bi-level reference voltage switching scheme in the case of different values of M

M	4	5	6
Sampling capacitor (C)	8	16	32
Average switching energy (CV_{ref}^2)	2.76	2.91	4.63
DNL (LSB)	0.598	0.471	0.347
INL (LSB)	0.634	0.478	0.350

voltage switching schemes.

The energy consumption and linearity of the proposed Bi-level reference voltage switching scheme for M = 4, 5, and 6 are summarized in Table 1. It can be seen from the table that the energy consumption gradually increases as the value of M increases due to the increase in the capacitance array in the coarse quantization stage. The overall linearity gradually improves.

In Tri-level mode, the V_{aq} reference voltage is increased and a single-ended voltage flip technique is used with no energy consumption during the first three flip cycles. Figure 24 shows the energy consumption of the proposed Tri-level reference voltage switching strategy in the three cases of M = 4, 5, and 6.

Tri-level reference voltage switching schemes are shown in Table 2 below.

The energy consumption and linearity of the proposed Tri-level reference voltage switching scheme for M = 4, 5, and 6 are summarized in Table 2. From comparing Table 1, it can be seen that the energy consumption and linearity of the Tri-base are better than that of the reference voltage self-adaptive structure regardless of the value of M. Therefore, it is concluded that the linearity becomes progressively better as the value of M increases.

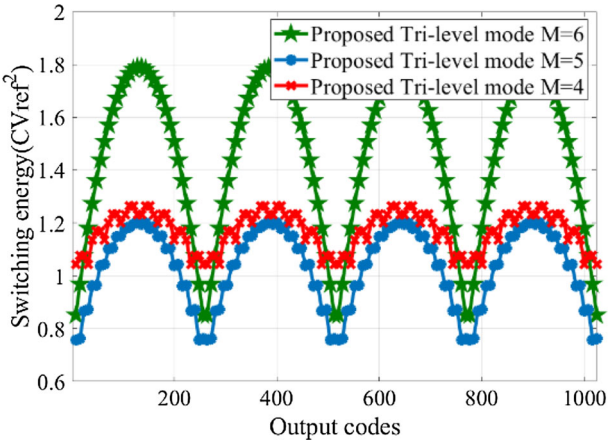

Fig. 24 Energy consumption of Tri-level reference voltage switching schemes at M = 4,5,6

Table 2 Analysis of Tri-level reference mode in the case of different values of M

M	4	5	6
Sampling capacitor (C)	8	16	32
Average switching energy (CV_{ref}^2)	1.17	1.03	1.47
DNL (LSB)	0.347	0.236	0.172
INL (LSB)	0.350	0.246	0.177

Therefore, at the cost of increased external level reference voltage, the proposed Tri-level reference mode is more suitable to save circuit power consumption and improve linearity.

Figure 25 shows the simulated energy consumption plots of the proposed 10-bit

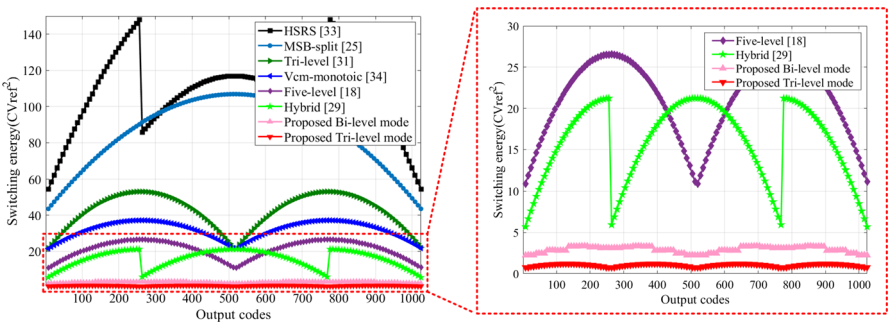

Fig. 25 Switching energy against output code

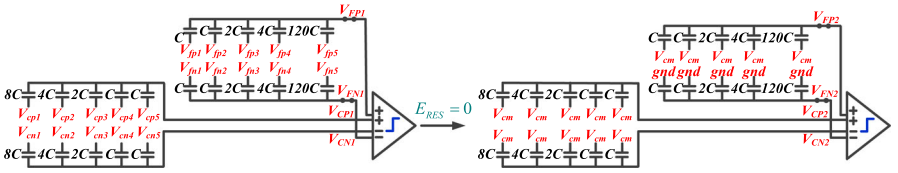

Fig. 26 Illustration of the reset scheme in the Bi-level reference mode

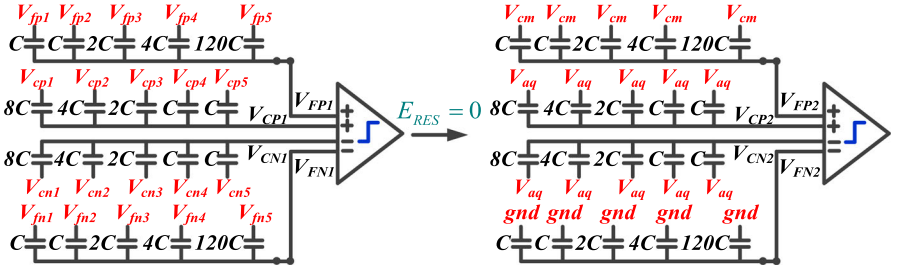

Fig. 27 Illustration of the reset scheme in the Tri-level references mode

SAR ADC switching method and several switching schemes with lower power consumption. A ramp signal is created under MATLAB simulation software, and the energy consumed by various capacitive switching schemes is calculated and compared by creating the inversion models of HSRS, MSB-split, Tri-level, V_{cm}-monotoic, Five-level, Hybrid, Proposed Bi-level mode, and Proposed Tri-level mode switching schemes for A/D conversion of the input signal. Figure 25 in the text shows the energy consumption of each switching scheme.

5.1 Reset Energy Consumption

Reset energy consumption is also one of the key points affecting the energy consumption of the switching strategy. Reset energy consumption is to change the final state of the flip of the capacitor array of the initial state. The reset voltage flipped when $V_{ip} > V_{in}$ using the Bi-level reference switch scheme is shown in Fig. 26.

The reset voltage flip when $V_{ip} > V_{in}$ using the Tri-level reference switching scheme is shown in Fig. 27.

It can be demonstrated by the equations in the Appendix that the proposed Bi-level reference voltage switching scheme and the Tri-level reference voltage switching scheme both have zero reset energy consumption. The proposed timing structure has a very high energy utilization.

5.2 Parasitic Capacitance

The presence of parasitic capacitance of the comparators and switches in the circuit also has a non-negligible impact on the energy consumption of the switching scheme.

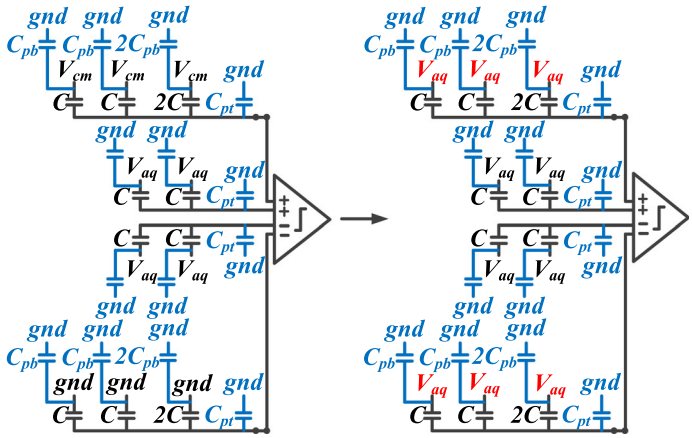

Fig. 28 Parasitic capacitance of the Tri-level reference mode

In order to simulate the actual capacitor array more accurately, the energy consumption of four switching schemes, V_{cm}-monotonic [36], Five-level [16], Hybrid [30], and the proposed reference voltage self-adaptive switching mode were simulated with parasitic capacitors, respectively.

Figure 28 illustrates the parasitic capacitance present in the capacitor array for the Tri-level reference switching scheme. Ideally, the average power consumption of the analyzed capacitor array is zero when the bottom plate voltage of all capacitors of the inefficient capacitor array is increased from gnd to V_{cm}. However, in the actual circuit, the power consumption is not zero because of the presence of the top board parasitic capacitor C_{pt} and the bottom board parasitic capacitor C_{pb}.

Figures 29 and 30 show the effect of parasitic capacitance on the switching energy. Compared to the four switching schemes, it can be seen that the energy consumption of the switch becomes larger after the addition of the parasitic capacitor. The addition of parasitic capacitors results in energy savings of 97.1%, 97.4%, 97.6%, 99.7%, and 99.8% for the V_{cm}-monotonic, Five-level, Hybrid, and novel reference voltage self-adaptive switching schemes, respectively, compared to conventional switching arrays. By observing Figs. 29 and 30, it can be concluded that the proposed novel switching scheme still has the best energy efficiency.

6 Linearity Analysis in Timing Switches

To improve energy utilization efficiency, the unit capacitance area is kept as small as possible, but the matching between capacitor arrays will greatly affect the overall conversion linearity. Figures 31, 32, 33, 34 depict behavioral simulation results of 500 Monte Carlo runs of the proposed reference voltage self-adaptive switching scheme for INL (Integral Nonlinearity) and DNL (Differential Nonlinearity) with $\sigma_{\mathrm{u}}/C_{\mathrm{u}} = 0.01$. Since the case of $\mathrm{M} = 5$ is an excess of the cases of $\mathrm{M} = 4$ and $\mathrm{M} = 6$, it will

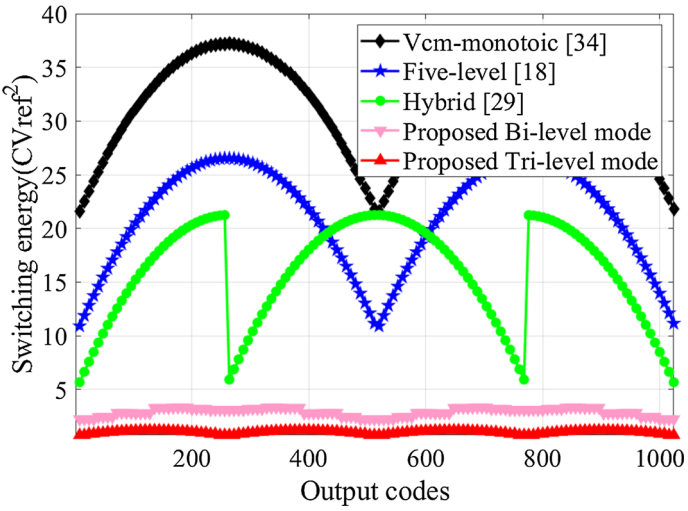

Fig. 29 Without parasitic capacitors

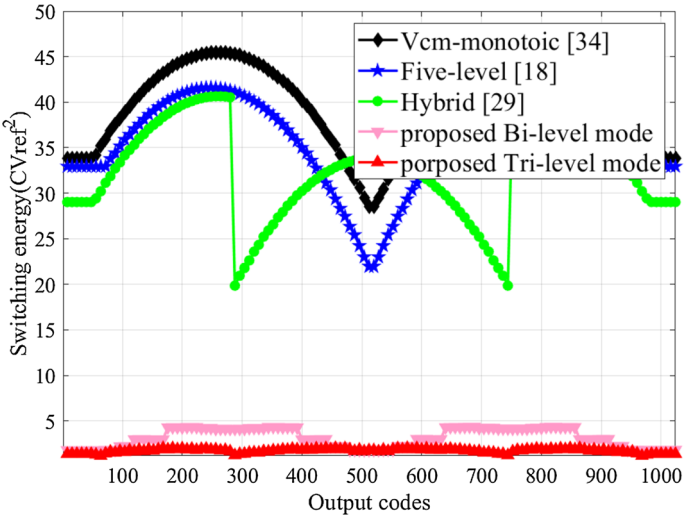

Fig. 30 Existence of parasitic capacitance

not be discussed in detail. The linearity of M = 5 is better than that of M = 4, but not as good as that of M = 6.

Figures 31 and 32 show the linearity simulation results for Bi-level reference voltages and Tri-level reference voltages for the case of M = 4. It can be seen from the plots that the INL and DNL of the tri-base switching scheme is 0.337 and 0.332, respectively, while the INL and DNL of the two-base switching scheme is 0.634 and

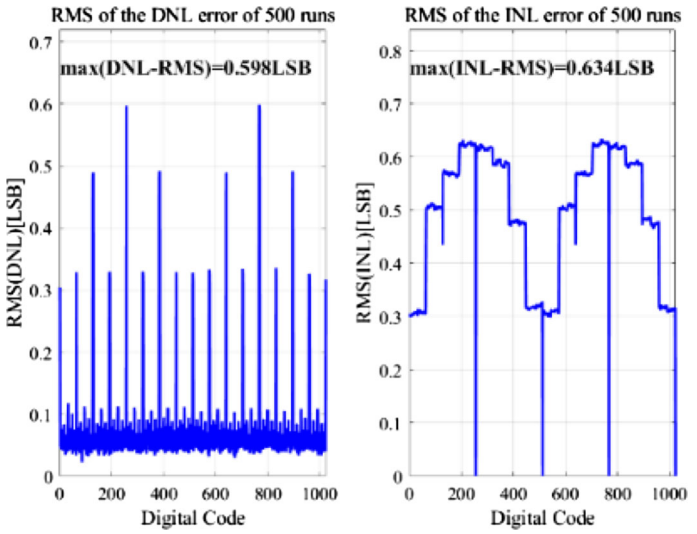

Fig. 31 DNL/INL versus Bi-level mode M = 4 output code

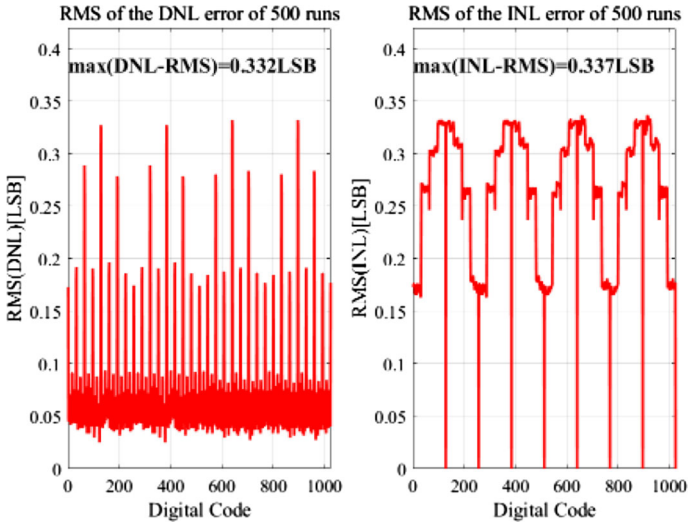

Fig. 32 DNL/INL versus Tri-level mode M = 4 output code

0.598, respectively. The linearity of the tri-base switching scheme is better than that of the two-base switching scheme.

Figures 33 and 34 show simulation results of the reference voltage self-adaptive switching method. The root mean square (RMS) INL and RMS DNL of the proposed architecture with Tri-level reference mode are only 0.177LSB and 0.172LSB, separately, while the RMS INL and RMS DNL of Bi-level reference mode are 0.350LSB

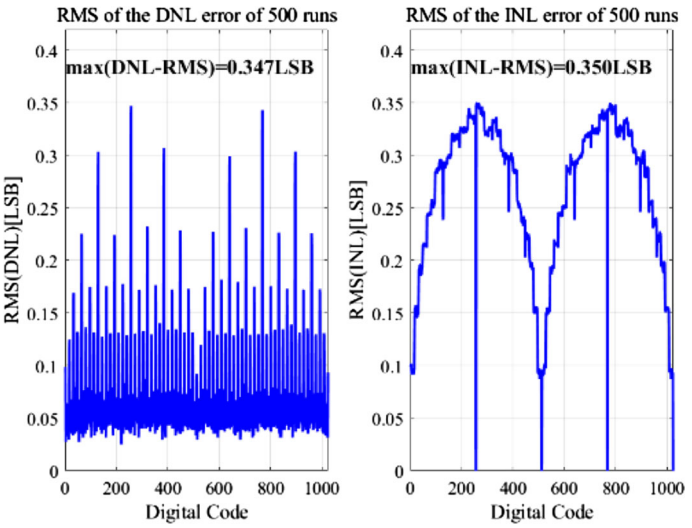

Fig. 33 DNL/INL versus Bi-level mode M = 6 output code

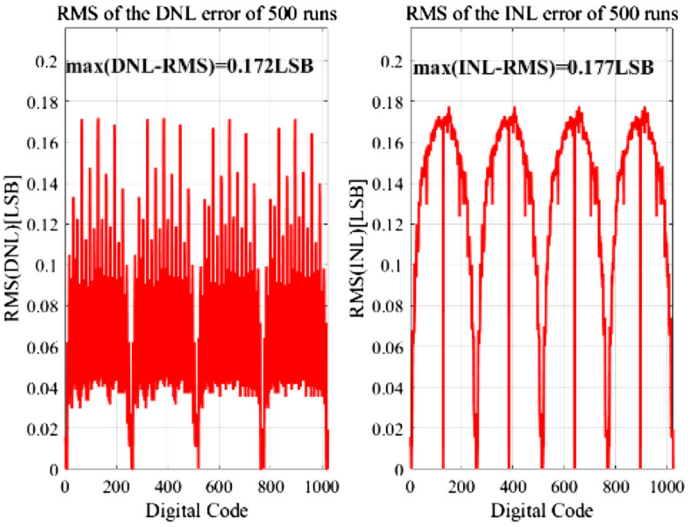

Fig. 34 DNL/INL versus Tri-level mode M = 6 output code

and 0.347LSB, respectively. The linearity of the Tri-level reference voltage switching scheme is better than that of the Bi-level reference voltage switching scheme.

From the analysis of the above three cases, it is concluded that the linearity of the overall structure becomes better and better due to the increase in the capacitance array of the coarse quantization stage caused by the increase in M.

Table 3 summarizes the average energy consumption, linearity, and capacitance

Table 3 Comparison of different switching schemes for 10-bit SAR ADC

Switching scheme	Switch energy (CV_{ref}^2)	Energy saving (%)	Number of unit capacitor	Area reduction (%)	Logic complexity	Reference voltages	Reset energy	Capacitive array	Linearity (INL/DNL)
Conventional	1363.3	0	2048	0	Low	gnd, V_{ref}	NO	Single	–
Set and down [17]	255.5	81.2	1024	50	Low	gnd,1/2V_{ref}, V_{ref}	NO	Single	0.192/0.181
Vcm-based [35]	170.2	87.5	1024	50	Low	gnd,1/2V_{ref}, V_{ref}	NO	Single	–
HSRS [34]	106.2	92.2	1024	50	Medium	gnd,1/2V_{ref}, V_{ref}	NO	Single	–
MSB-split V_{cm} [25]	85.08	93.7	512	75	Low	gnd,1/2V_{ref}, V_{ref}	NO	Single	–
Tri-level [33]	42.4	96.9	512	75	Low	gnd,1/2V_{ref}, V_{ref}	NO	Single	0.168/0.165
Vcm-monotonic [36]	31.9	97.7	512	75	Low	gnd,1/2V_{ref}, V_{ref}	NO	Single	–
Five-level [16]	21.2	98.4	512	75	Medium	gnd,1/4V_{ref}, 1/2V_{ref}, 3/4V_{ref}, V_{ref}	NO	Single	–
Hybrid [30]	15.88	98.8	512	75	Medium	gnd, 1/2V_{ref}, V_{ref}	Yes	Single	–
Wang [28]	10.61	99.2	256	87.5	Medium	gnd, 1/4 V_{ref}, 1/2V_{ref}, V_{ref}	Yes	Single	0.321/0.321
Zhao [27]	10.54	99.2	512	75	Medium	gnd, 1/2V_{ref}, V_{ref}	NO	Single	0.161/0.152
Lu [18]	6.35	99.5	544	73.4	Medium	1/2V_{ref}, V_{refn}, V_{refp}	Yes	Single	0.416/0.254

Table 3 (continued)

Switching scheme	Switch energy (CV_{ref}^2)	Energy saving (%)	Number of unit capacitor	Area reduction (%)	Logic complexity	Reference voltages	Reset energy	Capacitive array	Linearity (INL/DNL)
TSDC [3]	2.14	99.8	320	84.38	High	gnd, $1/2V_{ref}$, V_{ref}	NO	Double	0.281/0.234
Ding [5]	1.3	99.9	62	96.9	High	gnd, $1/2V_{ref}$, V_{ref}	NO	Double	0.627/0.727
TSMS [9]	1.38	99.9	390	80.96	High	gnd, $1/2V_{ref}$	NO	Double	0.426/0.446
Proposed Bi-level mode	4.63	99.6	544	73.4	Medium	gnd, $1/2V_{ref}$	NO	Triple	0.350/0.347
Proposed Tri-level mode	1.47	99.9	544	73.4	Medium	gnd, 1/4 V_{ref}, $1/2V_{ref}$	NO	Triple	0.177/0.172

Table 4 Post-simulation results comparison of different switching schemes for 10-bit SAR ADC

Parameter	Ref. [25]$^{+}$	Ref. [28]*	Ref. [27]*	Ref. [35]$^{+}$	Ref. [19]$^{+}$	This work*
Technology (nm)	180	180	180	90	130	65
Resolution (bit)	10	10	10	10	10	10
Power supply (V)	1	0.6	1	1.2	0.8	1.2
Active area (mm^2)	0.13	0.13	0.057	0.18	0.2	0.239
Sampling rate (MS/s)	0.12	0.02	1	100	14	20
Power (μW)	2.97	0.035	15.25	3000	175.8	548.5
SFDR (dB)	67.4	70.56	68.63	71	69.2	68
SNDR (dB)	58.26	59.41	57.81	56.6	54.3	60.5
ENOB (bit)	9.39	9.57	9.31	9.11	8.72	9.76
FoM (fJ/conv.-step)	36.9	2.31	24.03	77	29.76	31.6

*Simulation $^{+}$Measured

area of the different switching schemes in previous works. As can be seen from the table, the proposed structure has low energy consumption and good linearity in the Bi-level reference voltage mode. In the Tri-level reference voltage mode, the proposed structure has extremely low energy consumption and very good linearity compared with other switching structures. The structure can be adjusted to the reference to the periphery circuit to improve the overall circuit compatibility.

Table 4 summarizes performance indicators such as technology, power supply, sampling rate, and active area of different switching schemes in previous work. The figure-of-merit (FOM) is as below:

$$\mathrm{FoM} = \frac{\mathrm{Power}}{f_S \times 2^{\mathrm{ENOB}}} \tag{16}$$

where f_s is the Sampling rate, Power represents that the power consumption of the ADC and the ENOB is the effective number of bits at Nyquist frequency sampling rate. The proposed SAR ADC achieves an FOM of 31.6 fJ/conversion-step. It can be concluded that the proposed switching scheme has better FOM in medium and high-speed ADCs.

Figure 35 compares the three aspects of energy consumption, linearity, and the number of capacitors per unit, and it can be seen that the Tri-level mode is very good in terms of both energy consumption and linearity. The Bi-level reference voltage switching mode also consumes less energy than most switching schemes. Therefore, the proposed energy consumption timing technique has very good external compatibility and is suitable for energy-efficient SAR-based ADCs.

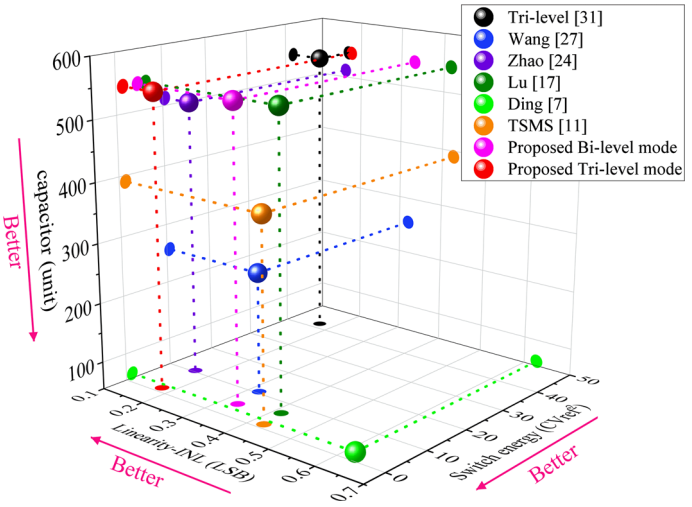

Fig. 35 About the comparison of energy consumption, linearity, and number of capacitors per unit

7 Conclusion

A high energy-efficient and reference voltage self-adaptive switching scheme for hybrid ADC is proposed. With the reference voltage self-adaptive module, the compatibility of the proposed switching timing scheme can be improved to a large extent. This is a better trade-off between energy efficiency, number of capacitors, common-mode voltage range, complexity of the logic control circuit, and linearity in our technique. The proposed reference voltage self-adaptive switching strategies achieved 99.7% and 99.9% savings in average switching energy and 73.4% reduction in total capacitance compared to the conventional scheme. The INL and DNL for both the Bi-level reference mode and the Tri-level reference mode are 0.350, 0.347 and 0.177, 0.172, respectively. The post-simulation results show that the 10-bit SAR ADC with the proposed switching scheme can achieve a signal-to-noise distortion ratio (SNDR) of 60.53 dB and a spurious-free dynamic range (SFDR) of 68 dB at a sampling rate of 20 MS/s in a 65 nm CMOS process. The area of this ADC is only 0.2392mm^2. Furthermore, the proposed two modes have no reset energy. Therefore, the proposed reference voltage self-adaptive switching scheme is suitable for realizing high energy-efficient and high area utilization VCO-SAR, Pipelined-SAR, or MASH ADC.

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Data availability Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Appendix: Without Reset Energy Consumption of Eqs. (16)–(33)

The reset energy consumption of the proposed Bi-level reference voltage capacitor switching structure is shown in the following mathematical derivation.

The value of the V_{FP2} voltage changed and the energy consumed by the voltage flip for this process is zero, as evidenced by the following equation:

$$V_{\mathrm{FP2}} = V_{\mathrm{FP1}} + \frac{\sum_{i=1}^{5} C_{\mathrm{fpi}} \times (V_{\mathrm{cm}} - V_{\mathrm{fpi}})}{\sum_{i=1}^{5} C_{\mathrm{fpi}}} \tag{17}$$

$$\begin{aligned} E_{\mathrm{RES\_FP}} &= \sum_{i=1}^{5} C_{\mathrm{fpi}} \times (-V_{\mathrm{cm}}) \times \left[(V_{\mathrm{FP2}} - V_{\mathrm{cm}}) - (V_{\mathrm{FP1}} - V_{\mathrm{fpi}})\right] \\ &= \sum_{i=1}^{5} C_{\mathrm{fpi}} \times (-V_{\mathrm{cm}}) \times \left[(V_{\mathrm{FP2}} - V_{\mathrm{FP1}}) - (V_{\mathrm{cm}} - V_{\mathrm{fpi}})\right] \\ &= V_{\mathrm{cm}} \times \left[\sum_{i=1}^{5} C_{\mathrm{fpi}}(V_{\mathrm{cm}} - V_{\mathrm{fpi}}) - \sum_{i=1}^{5} C_{\mathrm{fpi}}(V_{\mathrm{cm}} - V_{\mathrm{fpi}})\right] \\ &= 0 \end{aligned} \tag{18}$$

The value of the voltage changes of V_{CP2} and the energy consumed by the voltage flip as shown in (19):

$$V_{\mathrm{CP2}} = V_{\mathrm{CP1}} + \frac{\sum_{i=1}^{5} C_{\mathrm{cpi}} \times (V_{\mathrm{cm}} - V_{\mathrm{cpi}})}{\sum_{i=1}^{5} C_{\mathrm{cpi}}} \tag{19}$$

$$\begin{aligned} E_{\mathrm{RES\_CP}} &= \sum_{i=1}^{5} C_{\mathrm{pi}} \times (-V_{\mathrm{cm}}) \times \left[(V_{\mathrm{CP2}} - V_{\mathrm{cm}}) - (V_{\mathrm{CP1}} - V_{\mathrm{cpi}})\right] \\ &= \sum_{i=1}^{5} C_{\mathrm{cpi}} \times (-V_{\mathrm{cm}}) \times \left[(V_{\mathrm{CP2}} - V_{\mathrm{CP1}}) - (V_{\mathrm{cm}} - V_{\mathrm{cpi}})\right] \\ &= V_{\mathrm{cm}} \times \left[\sum_{i=1}^{5} C_{\mathrm{cpi}}(V_{\mathrm{cm}} - V_{\mathrm{cpi}}) - \sum_{i=1}^{5} C_{\mathrm{cpi}}(V_{\mathrm{cm}} - V_{\mathrm{cpi}})\right] \\ &= 0 \end{aligned} \tag{20}$$

The value of the voltage changes of V_{FN2} and the energy consumed is:

$$V_{FN2} = V_{FN1} + \frac{\sum_{i=1}^{5} C_{fpi} \times (gnd - V_{fpi})}{\sum_{i=1}^{5} C_{fpi}} \tag{21}$$

$$E_{RES\_FN} = 0 \tag{22}$$

The value of the voltage changes of V_{CN2} and the energy consumed by the voltage flip is proved and is calculated below:

$$V_{CN2} = V_{CN1} + \frac{\sum_{i=1}^{5} C_{cni} \times (V_{cm} - V_{cni})}{\sum_{i=1}^{5} C_{cni}} \tag{23}$$

$$\begin{aligned} E_{RES\_CN} &= \sum_{i=1}^{5} C_{cni} \times (-V_{cm}) \times [(V_{CN2} - V_{cm}) - (V_{CN1} - V_{fni})] \\ &= \sum_{i=1}^{5} C_{cni} \times (-V_{cm}) \times [(V_{CN2} - V_{CN1}) - (V_{cm} - V_{fni})] \\ &= V_{cm} \times \left[\sum_{i=1}^{5} C_{cni}(V_{cm} - V_{cni}) - \sum_{i=1}^{5} C_{cni}(V_{cm} - V_{cni}) \right] \\ &= 0 \end{aligned} \tag{24}$$

Thus, the total energy consumption of the Bi-level reference voltage scheme is:

$$E_{RES} = E_{RES\_CP} + E_{RES\_CN} + E_{RES\_FP} + E_{RES\_FN} = 0 \tag{25}$$

The reset energy consumption of the proposed Tri-level reference voltage capacitor switching structure is calculated by the following equation.

The value of the V_{FP2} voltage changed and the energy consumed by the voltage flip for this process is zero, as evidenced by the following mathematical derivation:

$$V_{FP2} = V_{FP1} + \frac{\sum_{i=1}^{5} C_{fpi} \times (V_{cm} - V_{fpi})}{\sum_{i=1}^{5} C_{fpi}} \tag{26}$$

$$E_{RES\_FP} = \sum_{i=1}^{5} C_{fpi} \times (-V_{cm}) \times \left[(V_{FP2} - V_{cm}) - (V_{FP1} - V_{fpi}) \right]$$

$$
\begin{aligned}
&= \sum_{i=1}^{5} C_{\mathrm{fpi}} \times (-V_{\mathrm{cm}}) \times \left[(V_{\mathrm{FP2}} - V_{\mathrm{FP1}}) - (V_{\mathrm{cm}} - V_{\mathrm{fpi}}) \right] \\
&= V_{\mathrm{cm}} \times \left[\sum_{i=1}^{5} C_{\mathrm{fpi}} (V_{\mathrm{cm}} - V_{\mathrm{fpi}}) - \sum_{i=1}^{5} C_{\mathrm{fpi}} (V_{\mathrm{cm}} - V_{\mathrm{fpi}}) \right] \\
&= 0
\end{aligned} \tag{27}
$$

The value of the voltage changes of V_{CP2} and the energy consumed by the voltage flip is proved by the following equation:

$$
V_{\mathrm{CP2}} = V_{\mathrm{CP1}} + \frac{\sum_{i=1}^{5} C_{\mathrm{cpi}} \times (V_{\mathrm{aq}} - V_{\mathrm{cpi}})}{\sum_{i=1}^{5} C_{\mathrm{cpi}}} \tag{28}
$$

$$
\begin{aligned}
E_{\mathrm{RES\_CP}} &= \sum_{i=1}^{5} C_{\mathrm{cpi}} \times (-V_{\mathrm{aq}}) \times \left[\left(V_{\mathrm{CP2}} - V_{\mathrm{aq}} \right) - (V_{\mathrm{CP1}} - V_{\mathrm{cpi}}) \right] \\
&= \sum_{i=1}^{5} C_{\mathrm{cpi}} \times (-V_{\mathrm{aq}}) \times \left[(V_{\mathrm{CP2}} - V_{\mathrm{CP1}}) - (V_{\mathrm{aq}} - V_{\mathrm{cpi}}) \right] \\
&= V_{\mathrm{aq}} \times \left[\sum_{i=1}^{5} C_{\mathrm{cpi}} (V_{\mathrm{aq}} - V_{\mathrm{cpi}}) - \sum_{i=1}^{5} C_{\mathrm{cpi}} (V_{\mathrm{aq}} - V_{\mathrm{cpi}}) \right] \\
&= 0
\end{aligned} \tag{29}
$$

The value of the voltage changes of V_{FN2} and the energy consumed by the voltage flipped is proved and calculated below:

$$
V_{\mathrm{FN2}} = V_{\mathrm{FN1}} + \frac{\sum_{i=1}^{5} C_{\mathrm{fpi}} \times (V_{\mathrm{cm}} - V_{\mathrm{fpi}})}{\sum_{i=1}^{5} C_{\mathrm{fpi}}} \tag{30}
$$

$$
E_{\mathrm{RES\_FN}} = 0 \tag{31}
$$

The value of the voltage changes of V_{CN2} and the energy consumed by the voltage flipped is proved by the following expression:

$$
V_{CN2} = V_{CN1} + \frac{\sum_{i=1}^{5} C_{cni} \times (V_{cm} - V_{cni})}{\sum_{i=1}^{5} C_{cni}} \tag{32}
$$

$$
\begin{aligned}
E_{\mathrm{RES\_CN}} &= \sum_{i=1}^{5} C_{\mathrm{cni}} \times (-V_{\mathrm{aq}}) \times \left[\left(V_{\mathrm{CN2}} - V_{\mathrm{aq}} \right) - \left(V_{\mathrm{CN1}} - V_{\mathrm{fni}} \right) \right] \\
&= \sum_{i=1}^{5} C_{\mathrm{cni}} \times (-V_{\mathrm{aq}}) \times \left[\left(V_{\mathrm{CN2}} - V_{\mathrm{CN1}} \right) - \left(V_{\mathrm{aq}} - V_{\mathrm{fni}} \right) \right] \\
&= V_{\mathrm{aq}} \times \left[\sum_{i=1}^{5} C_{\mathrm{cni}} (V_{\mathrm{aq}} - V_{\mathrm{cni}}) - \sum_{i=1}^{5} C_{\mathrm{cni}} (V_{\mathrm{aq}} - V_{\mathrm{cni}}) \right] \\
&= 0
\end{aligned} \tag{33}
$$

The total energy consumption of the Tri-level-based voltage scheme is:

$$
E_{\mathrm{RES}} = E_{\mathrm{RES\_CP}} + E_{\mathrm{RES\_CN}} + E_{\mathrm{RES\_FP}} + E_{\mathrm{RES\_FN}} = 0 \tag{34}
$$

Conclusion: The proposed Bi-level reference voltages and Tri-level reference voltages have no reset energy consumption. The analysis shows that there is no switch to the ports of the capacitor array and the comparator and that the voltage of each capacitor on the bottom plate of the capacitor array is not consistent. This will exist to reset the energy consumption.

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